RECOMMENDED FOR NEW DESIGNS

ATEK177P4

2 to 20 GHz High OIP2 LNA

Product Description

ATEK177P4 is a Wideband GaAs MMIC High Output IP2 Low Noise Amplifier (LNA) operating from 2 to 20 GHz.

The ATEK177P4 LNA provides a high gain of 25dB with a corresponding low noise figure of 2.5dB and a high OIP3 of +32dBm. The LNA has a high 2nd order intercept of +45dBm that results in 40dBc suppression of the second harmonic with an operating power of +6dBm output power. This allows users to easily realize a very high dynamic range for wideband receiver frontends.

The ATEK177P4 LNA is housed in a compact 4x4 mm SMD package with input and output matched to 50 ohms internally.

Evaluation Board, bare die, custom package, and module options are available upon request.

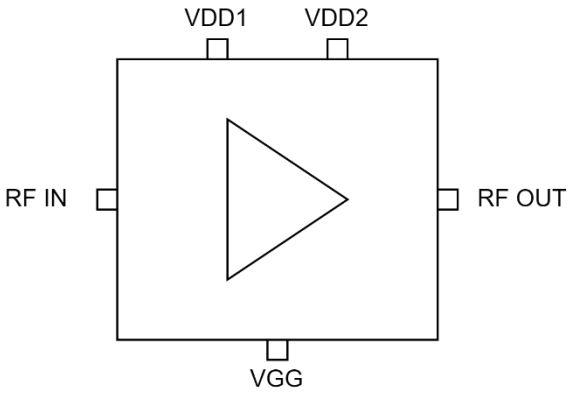
Product Features

- Frequency Range: 2 - 20 GHz
- OIP2: +45 dBm
- OIP3: +32dBm
- P1dB: +20dBm
- Gain: 25 dB
- Noise Figure: 2.3 dB
- VD BIAS: +4V @ 200mA
- 4x4 mm Compact Size

Applications

- Wideband Receivers, SDRs
- Microwave Radio
- Test and Measurement
- EW / ECM / C-UAS
- Military and Commercial Radar

Functional Block Diagram



Electrical Specifications

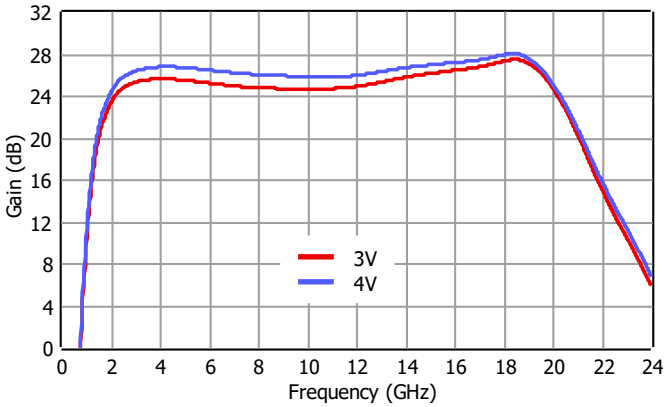
Conditions unless otherwise specified: $V_{DD1} = V_{DD2} = V_{GG}$ = 4 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		2		20	GHz
Gain	2 GHz		24.5		dB
	8 GHz		26		
	12 GHz		26		
	20 GHz		25		
IP2	2 GHz		42		dBm
	8 GHz		51		
	12 GHz		43		
	18 GHz		53		
Noise Figure	2 GHz		3.3		dB
	8 GHz		2.3		
	12 GHz		2.3		
	20 GHz		2.6		
Isolation	2 GHz		57		dB
	8 GHz		66		
	12 GHz		68		
	20 GHz		52		
Input Return Loss			-12		dB
Output Return Loss			-10		dB
Output IP3			32		dBm
Output P1dB			20		dBm
Psat			21		dBm
DC Supply Voltage (Vdd1 = Vdd2)			4		V
DC Supply Current (Idd1 + Idd2)			200		mA
DC Gate Voltage (Vgg)			4		V
DC Gate Current (Igg)			1		mA
Operating Temperature		-40		85	°C

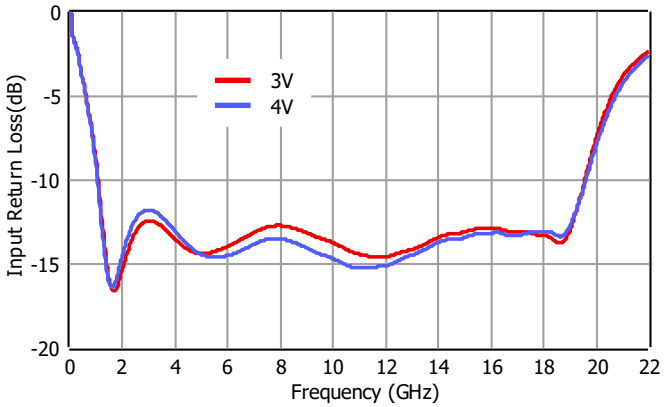
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD1} = V_{DD2} = V_{GG}$ = 4 V, Typical, T = 25 C, CW.

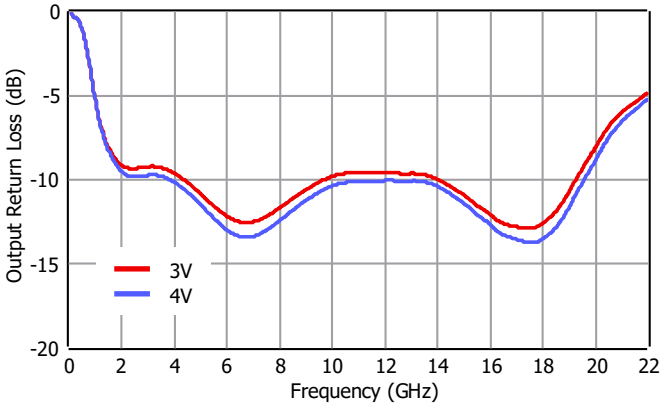
Gain



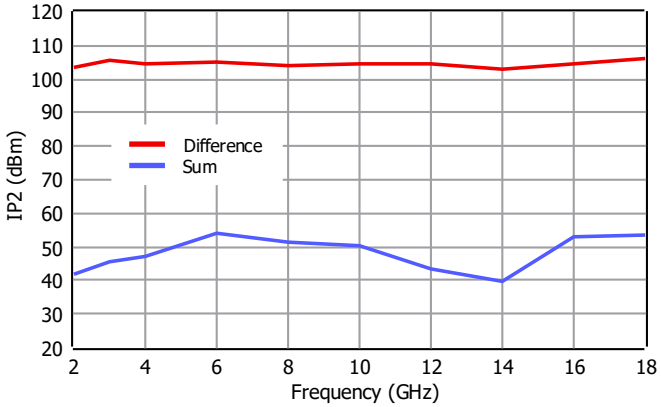
Input Return Loss



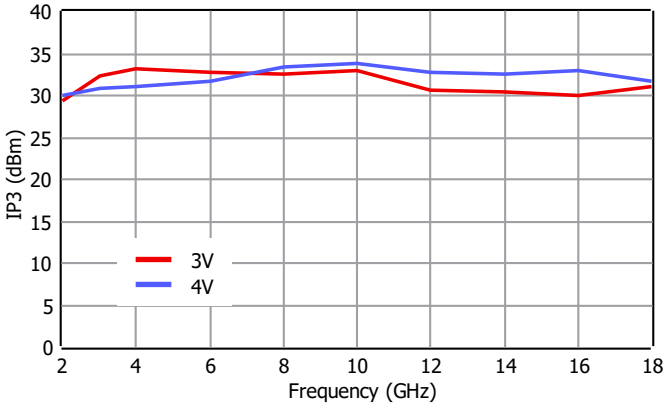
Output Return Loss



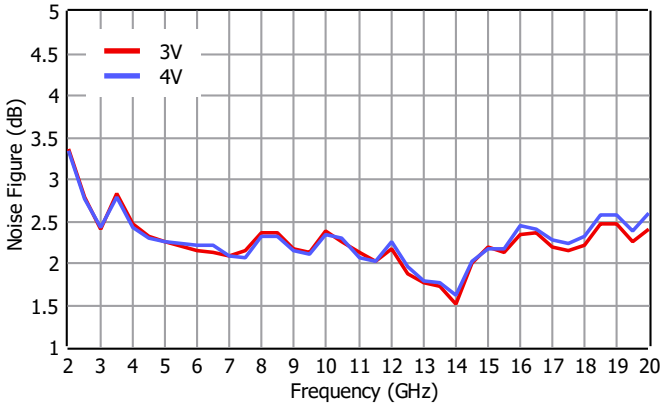
IP2 at Pout = +6 dBm/tone



IP3 at Pout = +6 dBm/tone



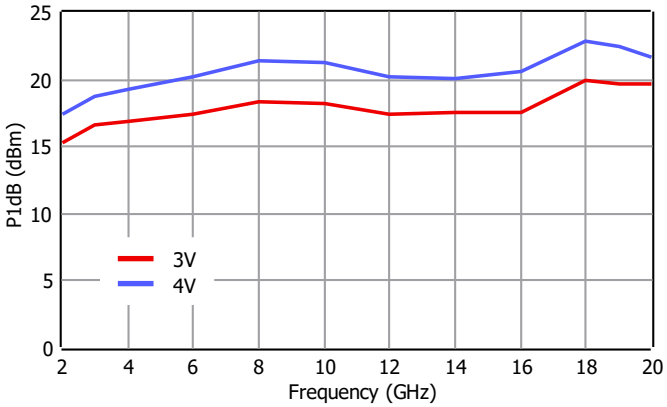
Noise Figure



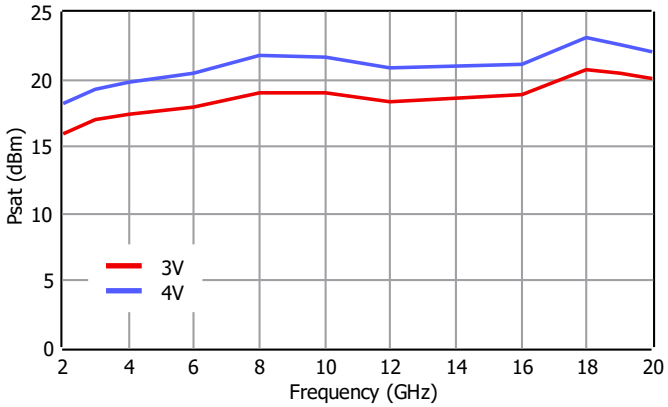
Typical Performance Plots

Conditions unless otherwise specified: V_{DD1} = V_{DD2} = V_{GG} = 4 V, Typical, T = 25 C, CW.

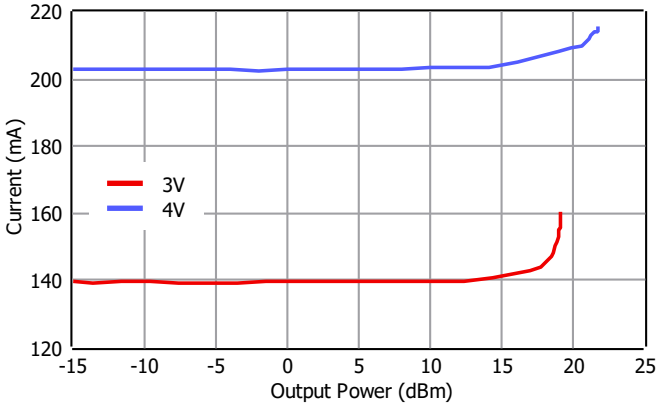
P1dB



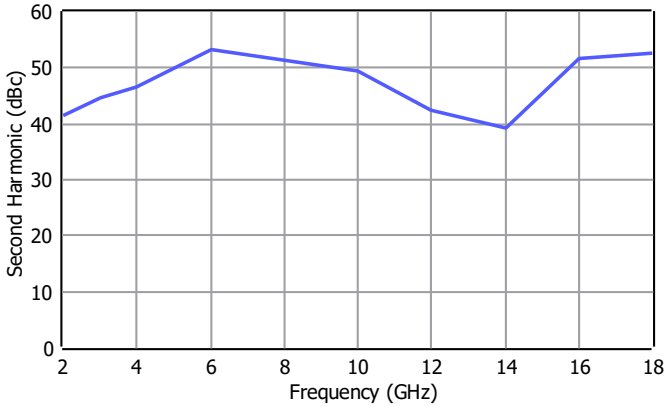
Psat



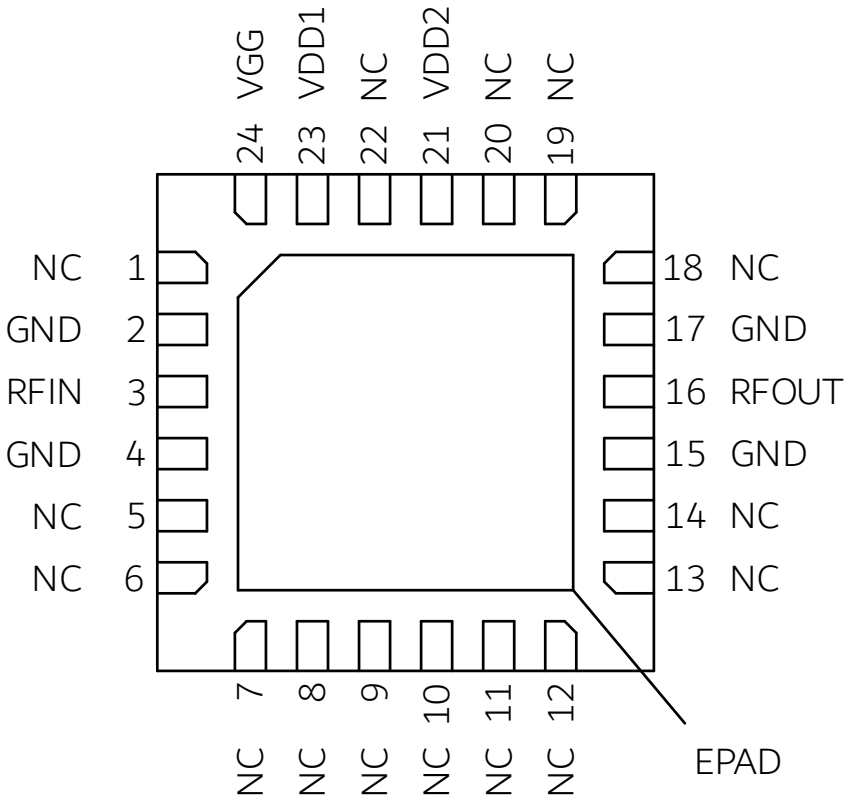
Current vs Output Power at 10 GHz



Second Harmonic at Pout = +6 dBm/tone



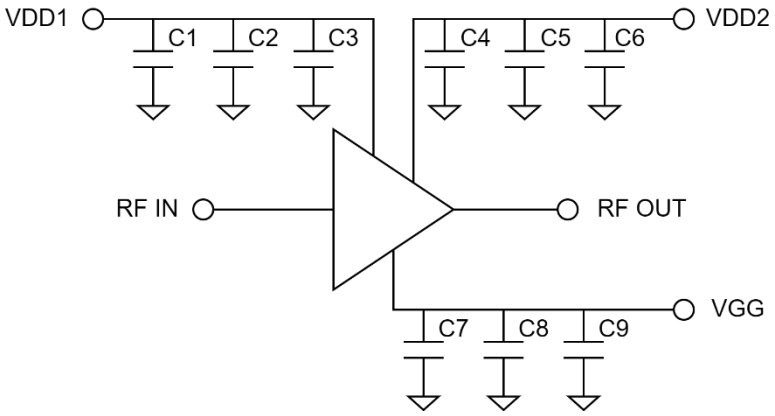
Pin Description



Pin Number	Pin Name	Description
3	RF IN	RF input pin. AC Coupled.
16	RF OUT	RF output pin. AC Coupled.
23	VDD1	Vdd bias pin.
21	VDD2	Vdd bias pin.
24	VGG	Vgg bias pin.
1, 5-14, 18-20, 22	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 15, 17	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Applications Information

Signal entering from RF IN goes to RF OUT with an amplification.
A typical application schematic to operate the amplifier is given below.



C1, C2, C3, C4, C5, C6, C7, C8 and C9 are used to filter out the ripples and unwanted signals coming from the Vdd supply and Vg supply. Using additional capacitors in parallel to C1, C2, C3, C4, C5, C6, C7, C8 and C9 will improve this filtering. If this filtering is of no concern, then the amplifier can be operated without C1, C2, C3, C4, C5, C6, C7, C8 and C9.

R1 is a gate resistor.

Small signal data plots are gathered with probe PCB measurements to generate plots shown in this document.

Large signal and noise figure data are generated with connectorized evaluation PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

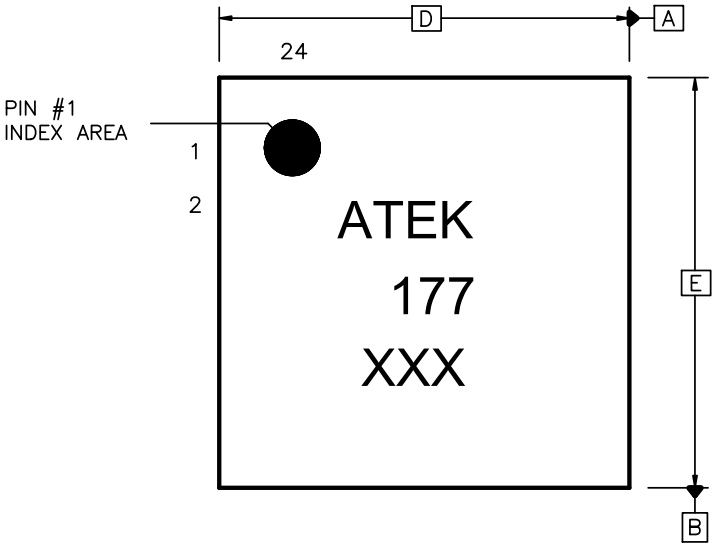
The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

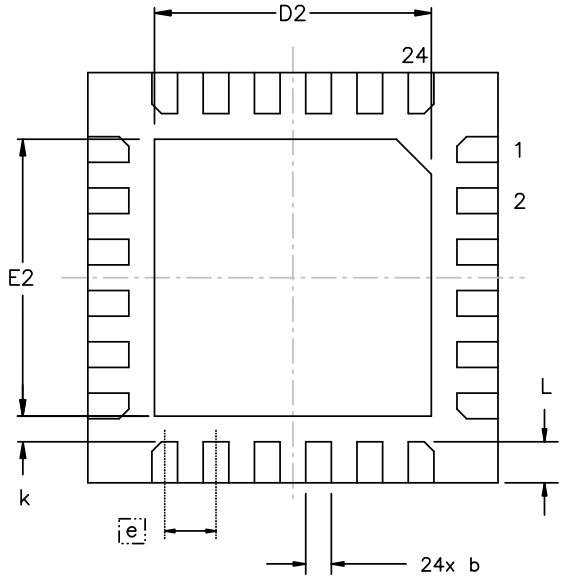
Parameter	Value/Range
Supply Voltage (Vdd)	+4.5V
RF Input Power (Vdd = +4.0V)	+6 dBm
Channel Temperature	+175 °C
Thermal Resistance	100°C/W
Power Dissipation (Ta=85 °C)	0.9 W
Storage Temperature	−55 to +125 °C
Operating Temperature	−40 to +85 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

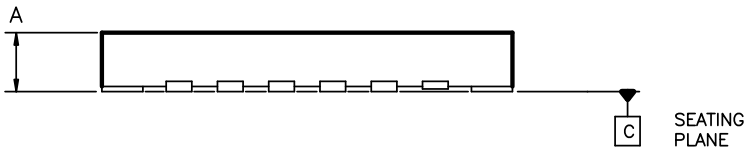
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM
2) MARKING XXX INDICATES INTERNAL LOT CODE

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
b	0.18	0.30	e	0.50 BSC	
D	4.00 BSC		k	0.20	–
D2	2.60	2.80	L	0.35	0.45
E	4.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Email: support@atekmidas.com

Notice

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
0.1	18.05.2026	Initial Release	
0.2	21.05.2026	Format and Content Fixed	
0.3	05.06.2026	Product Release, Format & Content Fixed	