ATEK563P5

0.2 to 24 GHz 0.5W Power Amplifier

Product Description

The ATEK563P5 is a 0.2 to 24 GHz wideband GaAs pHEMT MMIC power amplifier designed for radar, SATCOM, SDR, and Electronic Warfare transceivers. Operating from a +8V to +12V supply, it delivers 12 dB gain, +27 dBm P1dB, and an OIP3 of +40 dBm. For low-power applications, it can operate at +8V for increased gain at reduced output levels.

Supplied in a 5x5mm QFN SMT package, the device minimizes external components by integrating 50-ohm matched RF ports and a self-bias configuration that requires DC blocking capacitors, an external choke, and two external decoupling capacitors

The ATEK563P5 has outstanding drive/linearity for a wide range of radar, SATCOM, SDR, test instrument, & EW/ECM transceiver applications.

Evaluation Board, custom package, and module options are available upon request.

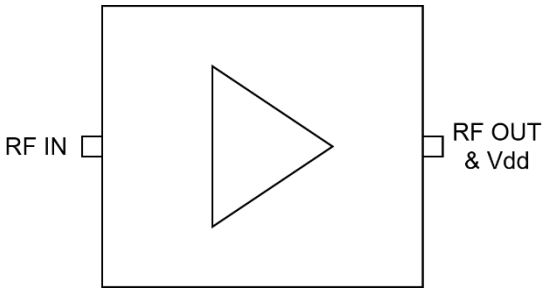
Product Features

- Frequency Range: 0.2 to 24 GHz
- Gain: 12 dB
- P1dB: +27 dBm
- Psat: +30 dBm, +12V, 24% PAE
- OIP3: +40 dBm
- +8 to +12V Single Supply
- 5x5 mm compact size

Applications

- Wideband Receivers, SDRs
- Telecommunication
- Test and Measurement
- SATCOM
- EW, ECM, & C-UAS

Functional Block Diagram



Electrical Specifications

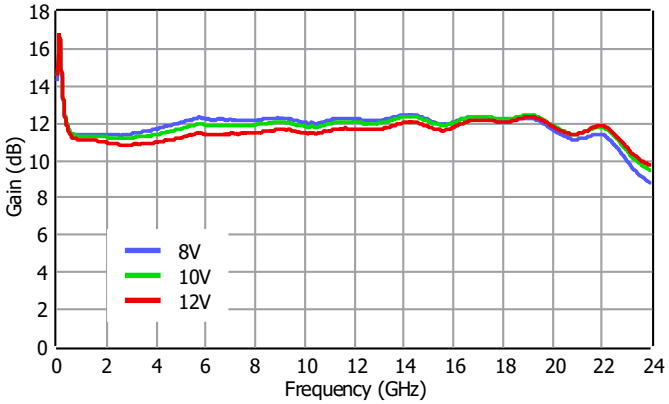
Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 360 mA, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.2		24	GHz
Gain	0.2 GHz		14.1		dB
	2 GHz		11.2		
	8 GHz		11.9		
	16 GHz		12		
	22 GHz		11.8		
Isolation	0.2 GHz		56		dB
	2 GHz		51		
	8 GHz		38		
	16 GHz		29		
	22 GHz		26		
Input Return Loss			-13		dB
Output Return Loss			-11		dB
Output IP3			39.5		dBm
Output P1dB			27		dBm
Psat			29		dBm
DC Supply Voltage (Vdd)		8.0	10.0 12.0	12.5	V
DC Supply Current			370 400		mA
Operating Temperature		-40		85	°C

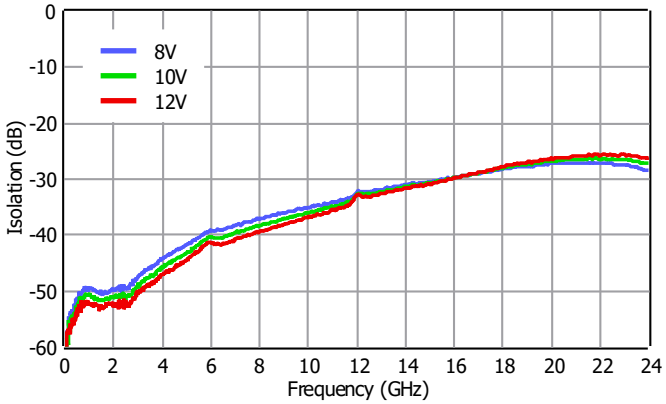
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 360 mA, Typical, T = 25 C, CW.

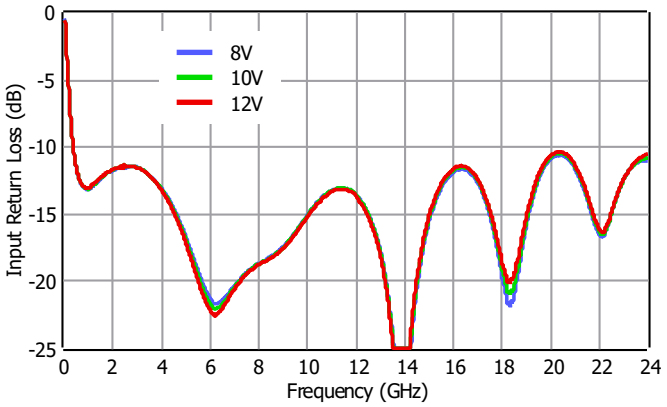
Gain



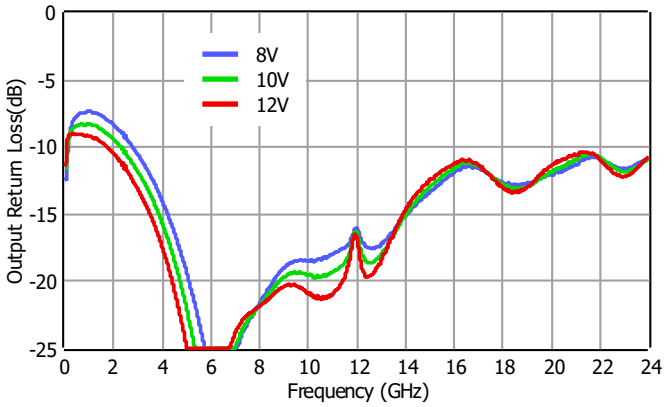
Isolation



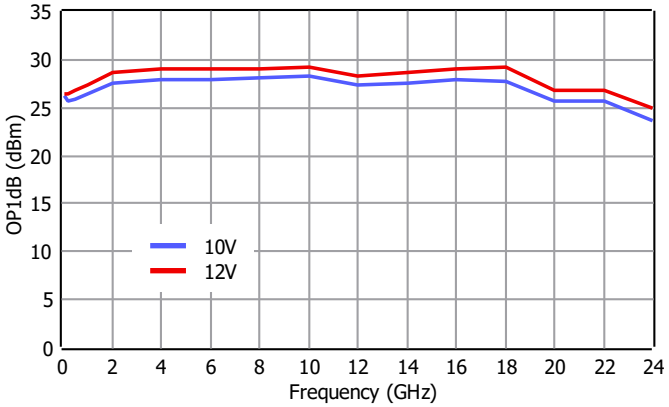
Input Return Loss



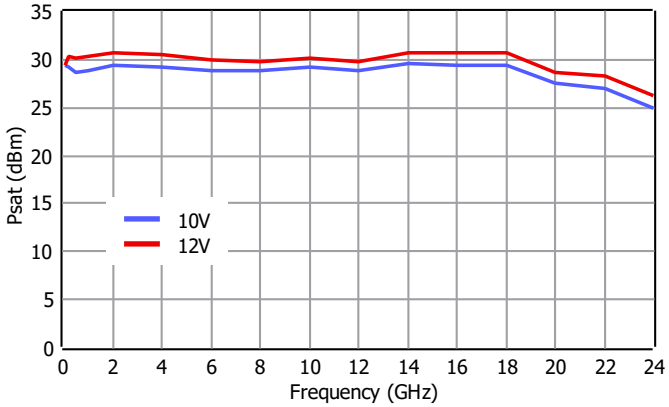
Output Return Loss



Output P1dB



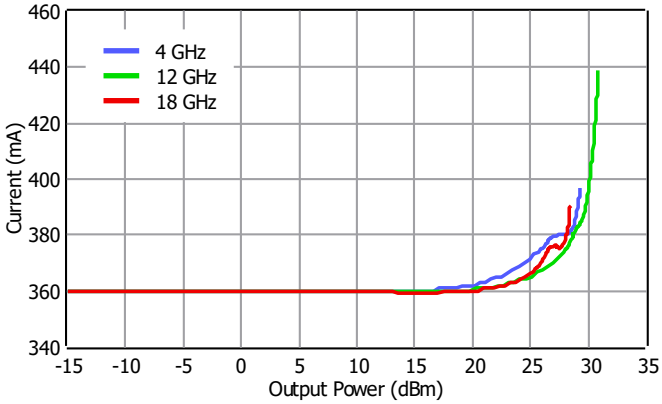
Psat



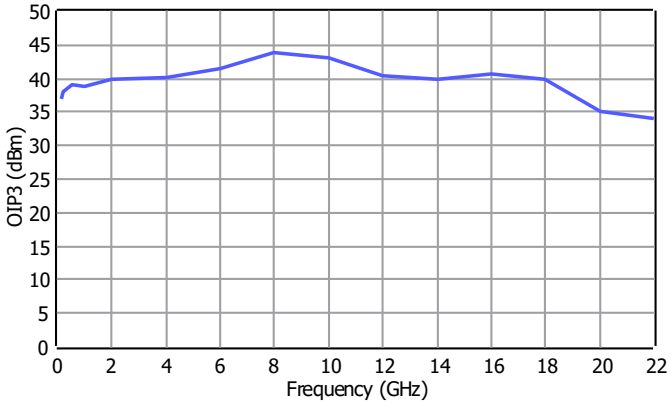
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 360 mA, Typical, T = 25 C, CW.

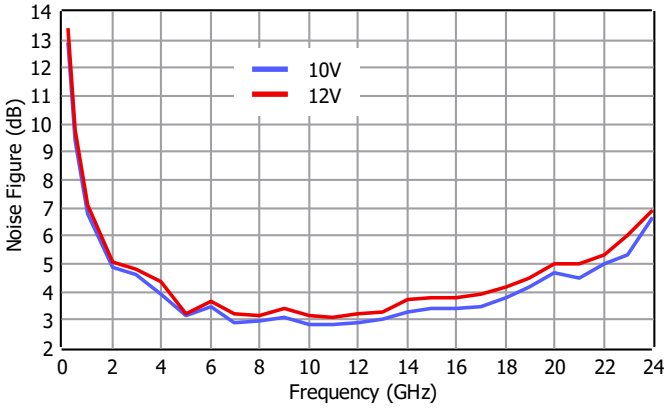
Current vs Output Power, Frequency



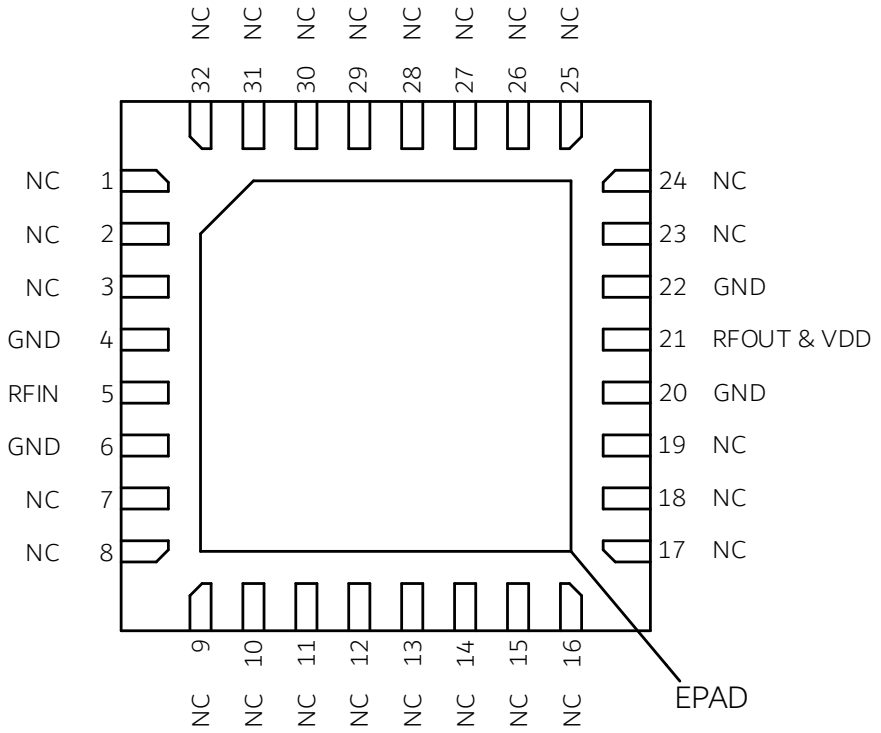
Output IP3



Noise Figure



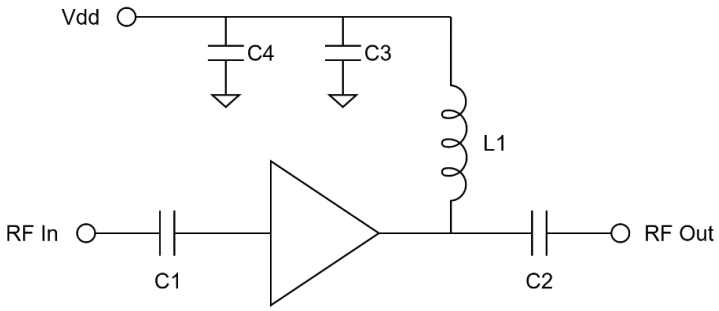
Pin Description



Pin Number	Pin Name	Description
5	RF IN	RF input pin. Wideband external DC block capacitor is required.
21	RF OUT & Vdd	RF output and Vdd supply pin. Wideband external DC block capacitor and choke inductor are required
1-3, 7-19, 23-32	NC	These pins are not internally connected. Can be grounded on the PCB.
4, 6, 20, 22	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Applications Information

Signal entering from RF IN goes to RF OUT with amplification.
A typical application schematic to operate the amplifier is given below.



C1 and C2 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

L1 is used as RF choke inductor. It is recommended to use wideband RF choke to achieve wideband performance.

To extend the low frequency cutoff of the amplifier from 10 MHz to lower frequencies, high value C1, C2 and L1 external components can be used. This will improve low frequency performance at the expense of flat wideband response, and high frequency response.

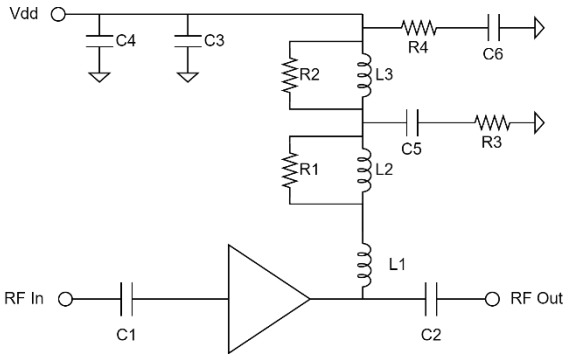
Choosing higher values for C1, C2 and L1 will allow amplifier to operate at lower frequencies, compared to the plots that is given in this datasheet. By increasing values of these components, low frequency operation can be extended below 200 MHz, at the expense of flat wideband, and high frequency response.

C3 and C4 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C3 and C4 will improve this filtering. If this filtering is of no concern, then amplifier can be operated without C3 and C4.

Small signal plots are gathered on probe PCB measurements with external connectorized Bias Tee and external connectorized DC Block, to generate data shown in this document. The calibration performed with external Bias Tee and external DC Block capacitor.

Large signal and noise figure data are generated with connectorized evaluation PCB measurements which have an external Bias Tee and external DC Block capacitors. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

When SMD Bias Tee and DC Block capacitors are used, the wideband performance will be affected. Typical application schematic to operate the amplifier with SMD Bias Tee and DC Block capacitors are given below.

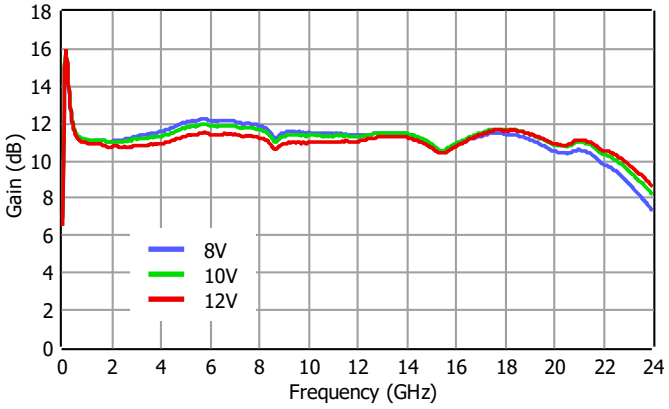


0.2 to 24 GHz 0.5W Power Amplifier

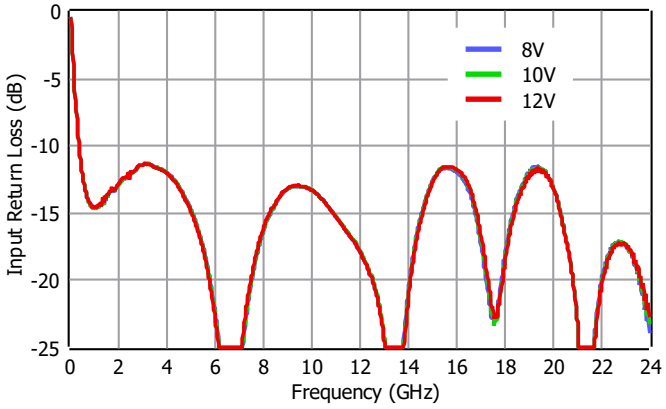
Typical Performance Plots with SMD Bias Tee and DC Block Capacitors

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 360 mA, Typical, T = 25 C, CW.

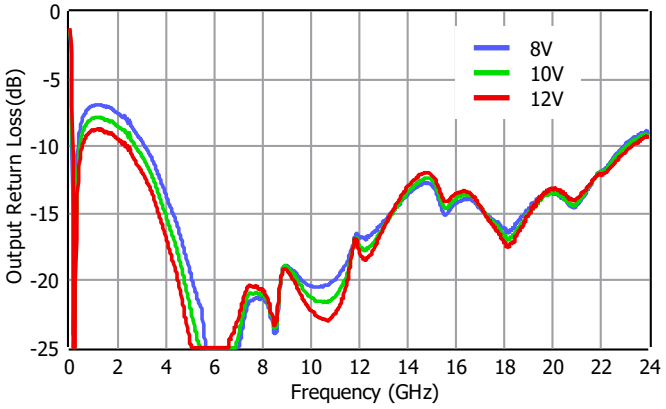
Gain



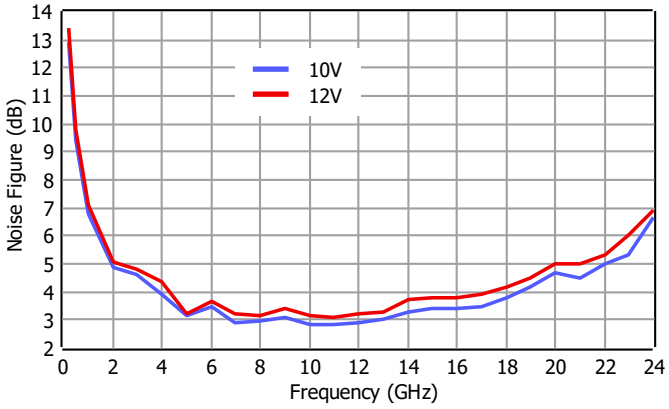
Input Return Loss



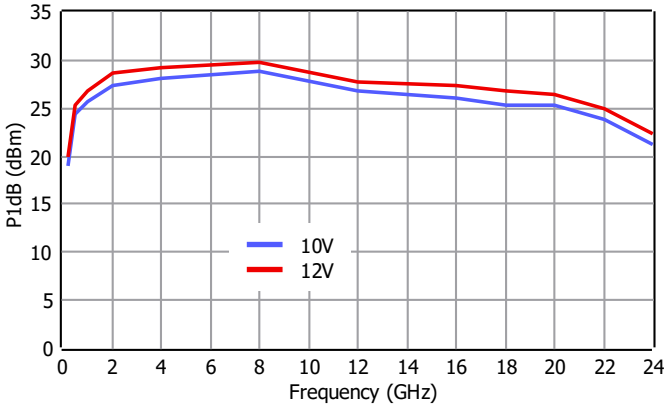
Output Return Loss



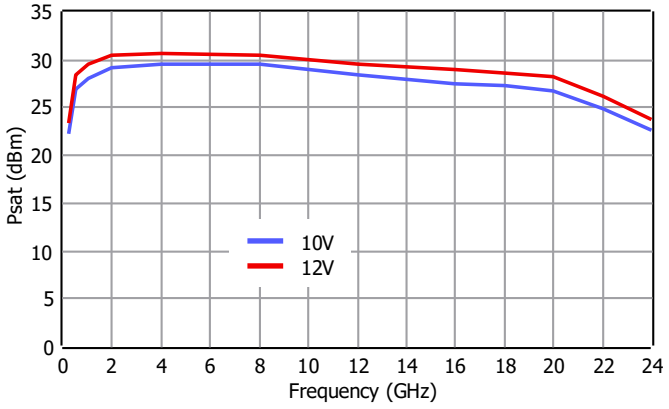
Noise Figure



Output P1dB



Psat



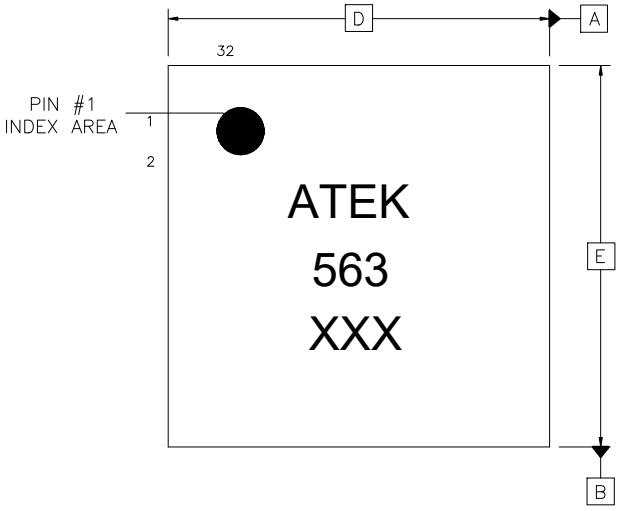
The NC pins of the Amplifier are connected to the GND on the PCBs. Vdd values shown on the datasheet correspond to the Vdd pins shown on the application schematic, not the output pin of the amplifier.

Absolute Maximum Ratings

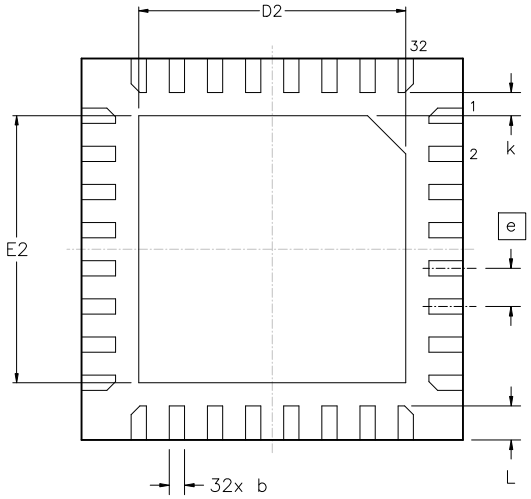
Parameter	Value/Range
Supply Voltage (Vdd)	+12.5 V
RF Input Power (Vdd = +10.0V)	+27 dBm
Channel Temperature	175 °C
Power Dissipation (Ta=85 °C)	4.56W
Thermal Resistance	19.73 °C/W
Storage Temperature	−55 to +125 °C
Operating Temperature	−40 to +85 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

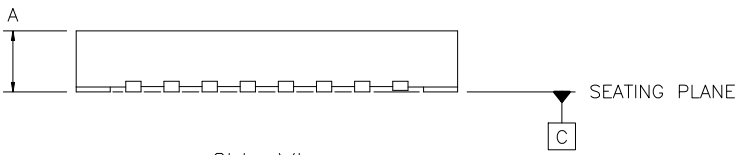
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	3.40	3.60
b	0.18	0.30	e	0.50 BSC	
D	5.00 BSC		k	0.20	–
D2	3.40	3.60	L	0.40	0.50
E	5.00 BSC				

Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

Notice

This document and its contents are property of ATEK MIDAS. ATEK MIDAS has carefully reviewed the product specification information herein, and it is believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or errors, and the information within may be changed at any time without prior notice. Use of this information and/or any of our products does not convey to the user any patent rights or licenses. ATEK MIDAS products are designed to be used only within the electrical and environmental limits published in their respective data sheets or custom quoted specifications. ATEK MIDAS does not authorize the use of any of its products beyond the current published data sheet limits. Such use beyond the currently published electrical and/or environmental data sheet limits voids all ATEK MIDAS warranties. ATEK MIDAS reserves the right to change component circuitry, package material, assembly/test/inspect processes, specifications or other information at any time without prior notice. ATEK MIDAS shall have no responsibility for the customer's products, customer applications, and actions of the customer related to this product.

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	16.09.2024	Initial Release	
1.1	06.11.2024	Application Section Revised, Large Signal Plots Added	
1.2	21.11.2024	Format and Content Fixed	
1.3	14.04.2024	Plots Updated	
1.4	29.04.2026	Format and Content Fixed	
1.5	05.06.2026	AMR Table Update, Format & Content Fixed	