ATEK MIDAS

RECOMMENDED FOR NEW DESIGNS

ATEK581N5

8 to 12 GHz 17W Power Amplifier

Product Description

ATEK581N5 is a GaN MMIC high-power 17W amplifier operating from 8 to 12 GHz while providing 32dB of small signal gain.

The ATEK581N5 delivers +42dBm output with 42% power added efficiency over the 8 to 12GHz band.

The power amplifier is housed in a compact 5x5mm SMD package with input and output matched to 50 ohms internally.

Evaluation Board, custom package, and module options are available upon request.

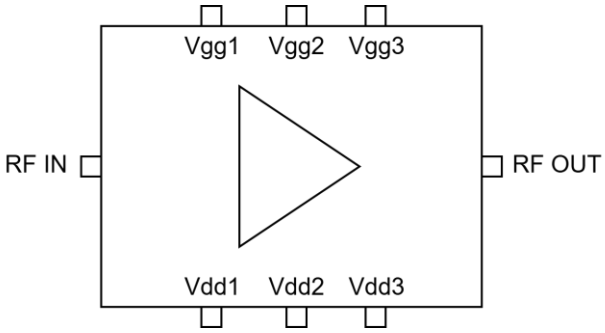
Product Features

- Internally matched GaN MMIC PA
- Frequency Range: 8 to 12 GHz
- Small Signal Gain: 32dB
- 21dB Power Gain with Pin = +22dBm
- PAE: 42% with +22dBm Pin
- Output Power: 17W
- Quiescent Bias: +28V @ 200mA
- 5x5 mm Compact Size

Applications

- Weather & Marine Radar
- Test & Measurement
- X-Band Transceivers
- EW / ECM / C-UAS

Functional Block Diagram



Electrical Specifications

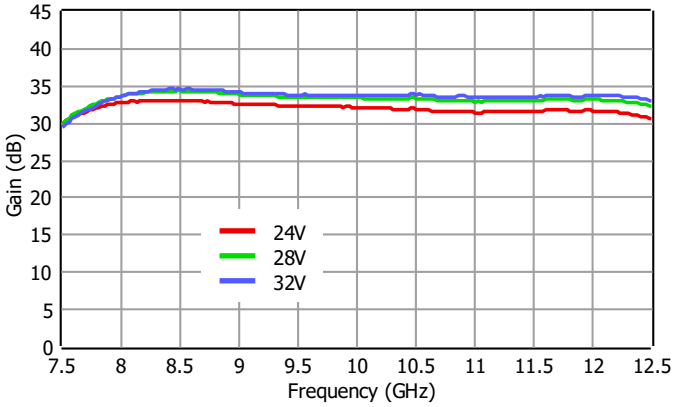
Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		8		12	GHz
Output Power at Pin: +22 dBm	8 GHz		42.9		dBm
	9 GHz		43		
	10 GHz		42.7		
	11 GHz		42.6		
	12 GHz		42.3		
Small Signal Gain	8 GHz		31.7		dB
	9 GHz		32.1		
	10 GHz		32.1		
	11 GHz		31.5		
	12 GHz		32.3		
Input Return Loss			-17		dB
Output Return Loss			-12		dB
Noise Figure			TBD		dB
Output IP3			TBD		dBm
Drain Voltage (Vdd1, Vdd2, Vdd3)		24	28	32	V
Gate Voltage (Vgg1, Vgg2, Vgg3) *Adjust the gate voltage between −4V and −1V to achieve an IDQ = 200mA typical*			-2.1		V
Quiescent Current (Idq1 + Idq2 + Idq3)			200		mA
PAE			42		%
Operating Temperature		-40		85	°C

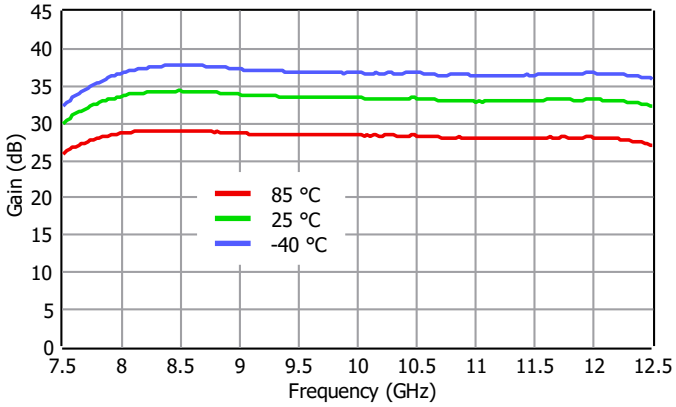
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

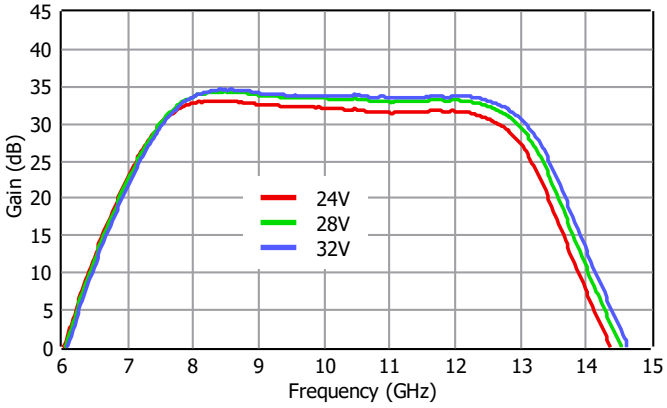
Gain vs Vdd



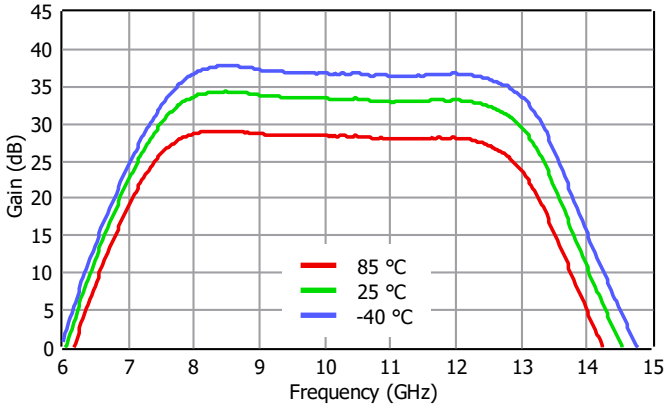
Gain vs Temperature



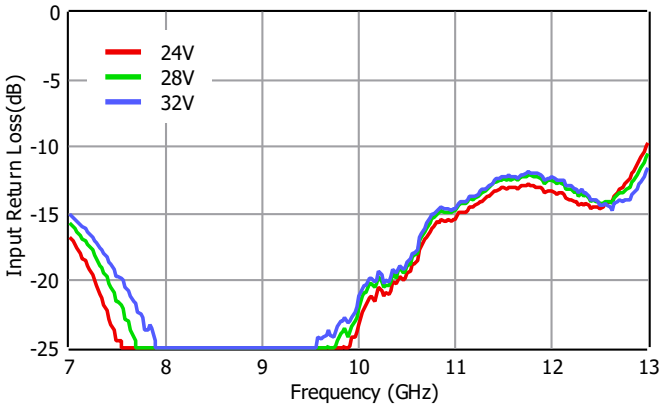
Wideband Gain vs Vdd



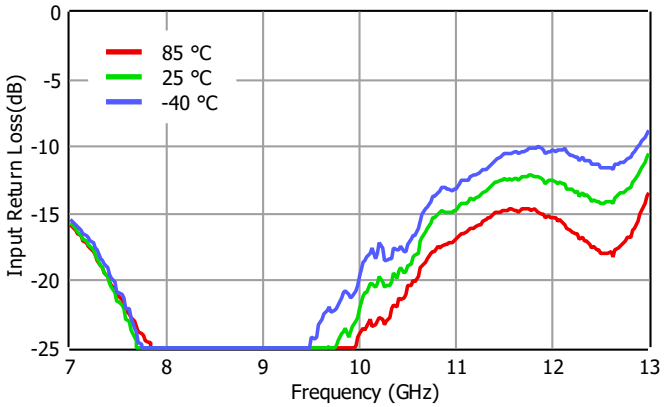
Wideband Gain vs Temperature



Input Return Loss vs Vdd



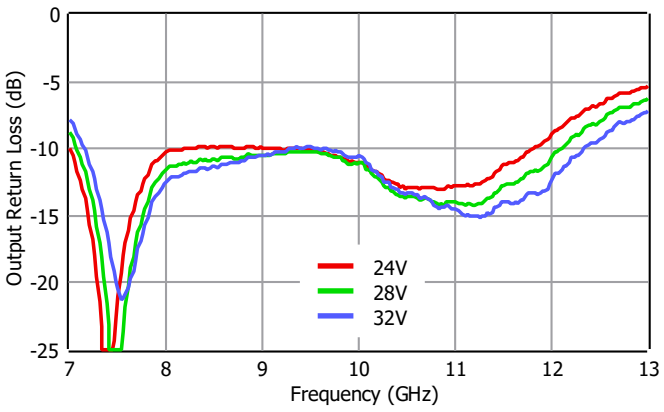
Input Return Loss vs Temperature



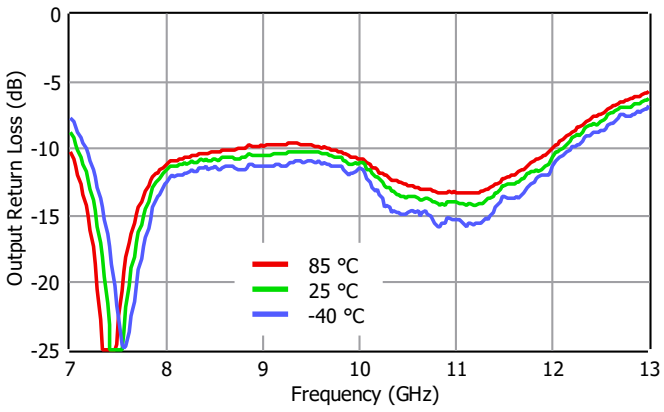
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

Output Return Loss vs Vdd



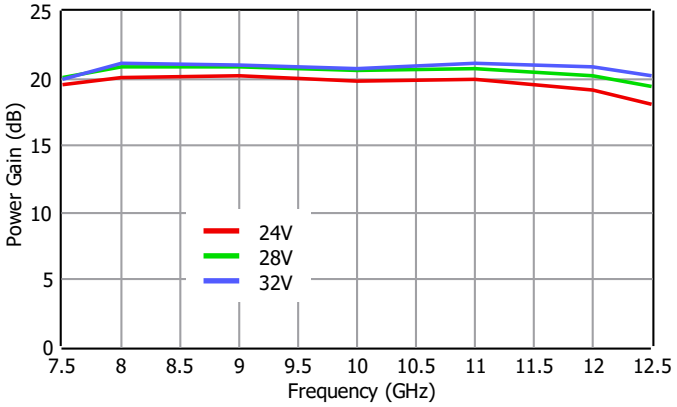
Output Return Loss vs Temperature



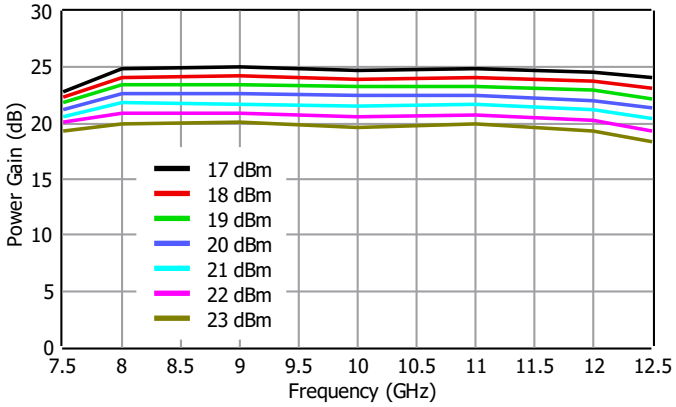
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

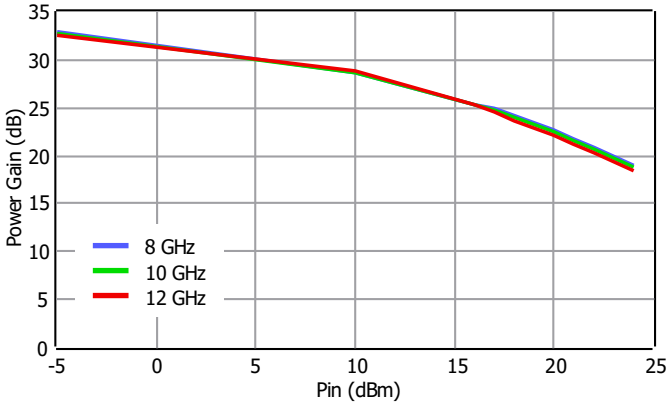
Power Gain vs Vdd, Pin = +22 dBm



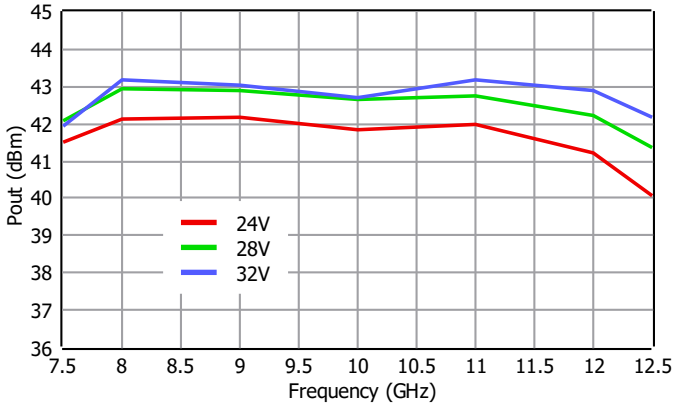
Power Gain vs Frequency, Pin



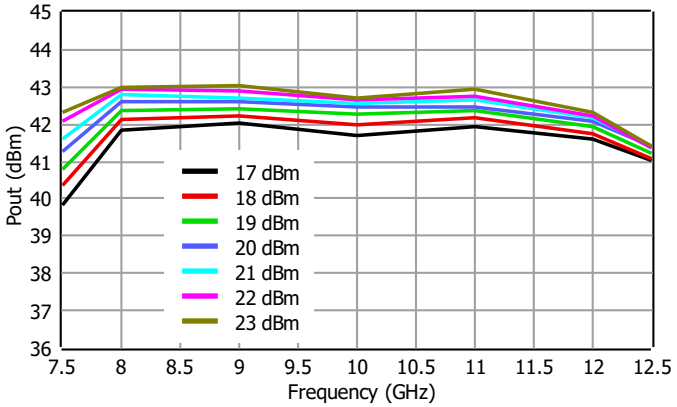
Power Gain vs Pin, Frequency



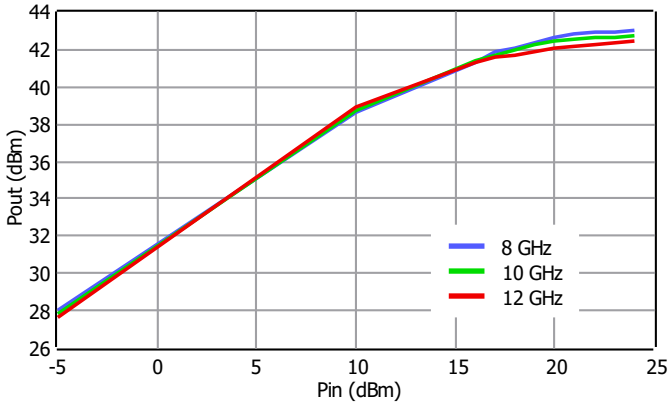
Pout vs Vdd, Pin = +22 dBm



Pout vs Frequency, Pin



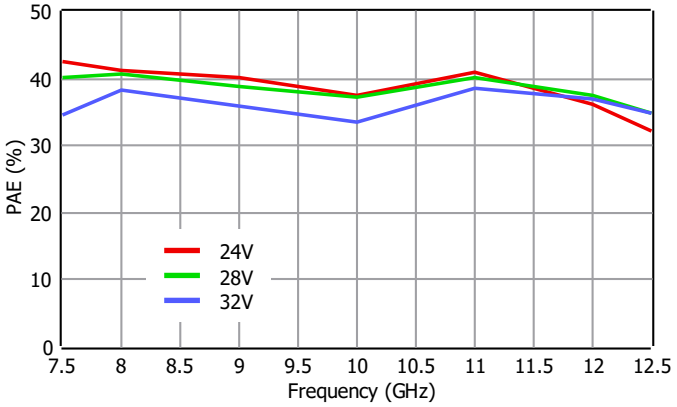
Pout vs Pin, Frequency



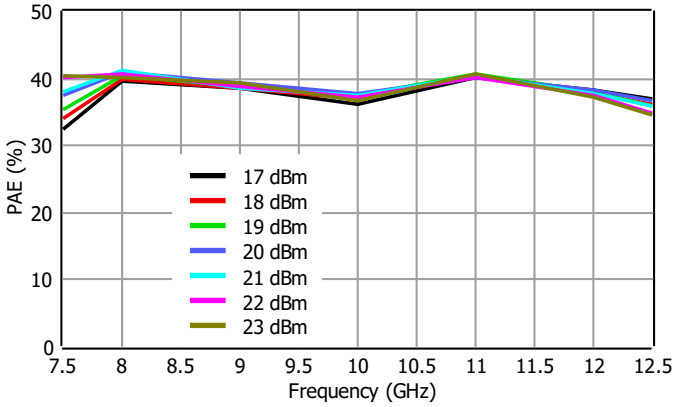
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

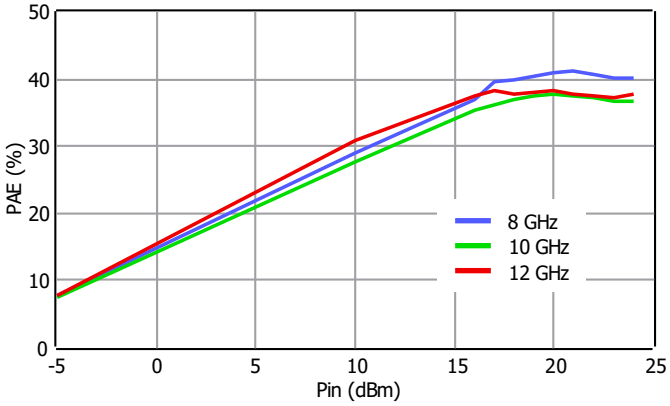
PAE vs Vdd, Pin = +22 dBm



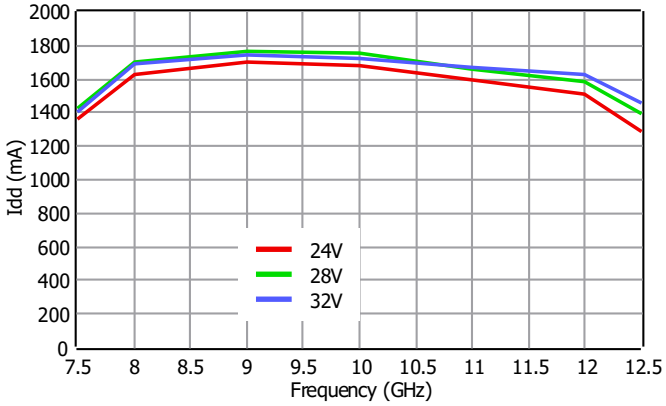
PAE vs Frequency, Pin



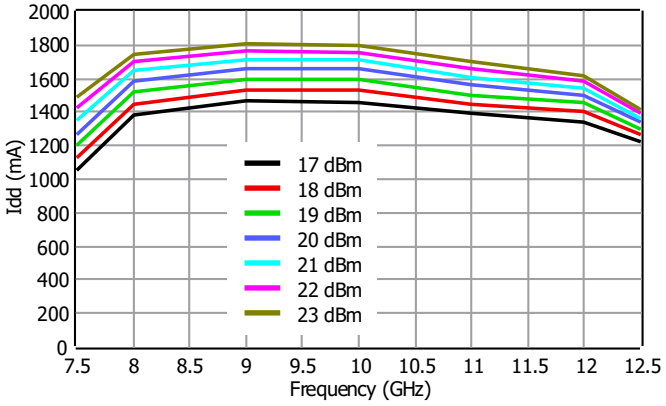
PAE vs Pin, Frequency



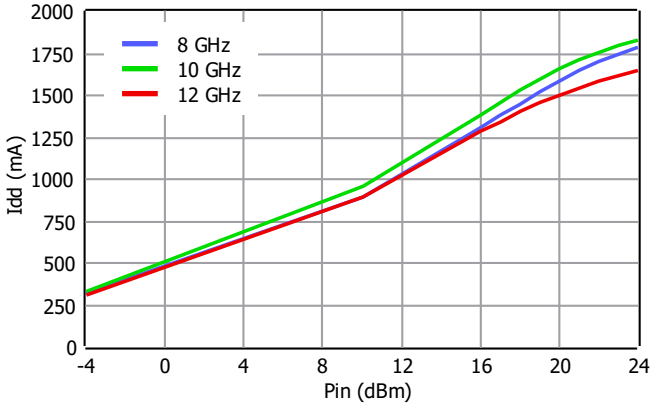
Idd vs Vdd, Pin = +22 dBm



Idd vs Frequency, Pin



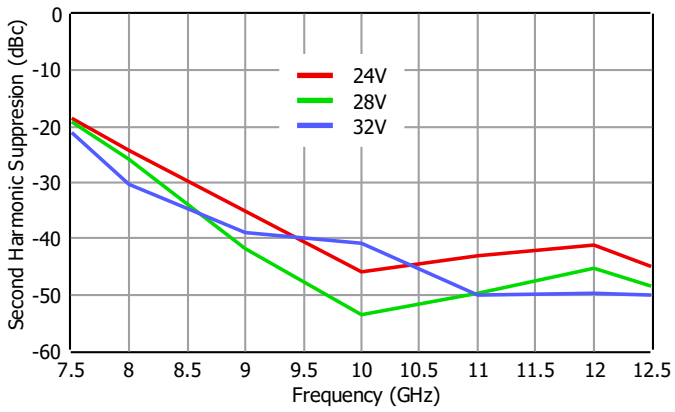
Idd vs. Pin, Frequency



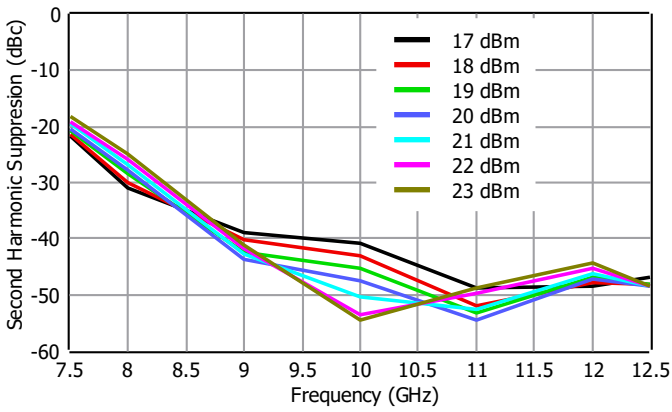
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

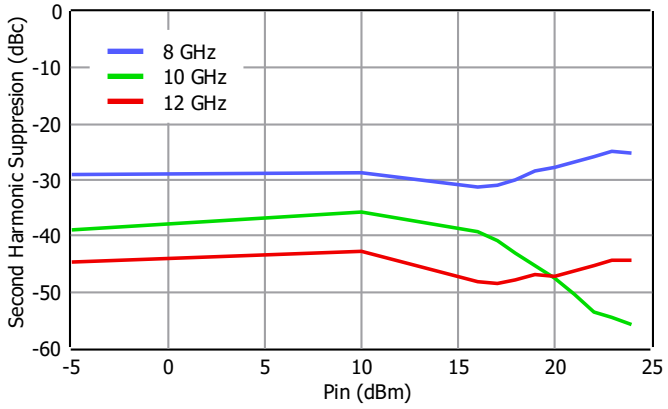
2nd Harmonic vs Vdd, Pin = +22 dBm



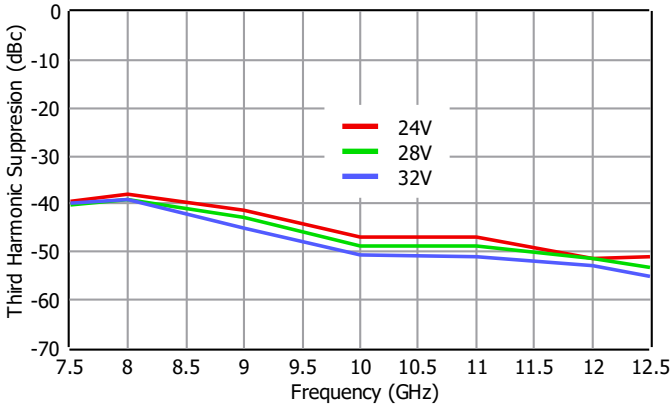
2nd Harmonic vs Frequency, Pin



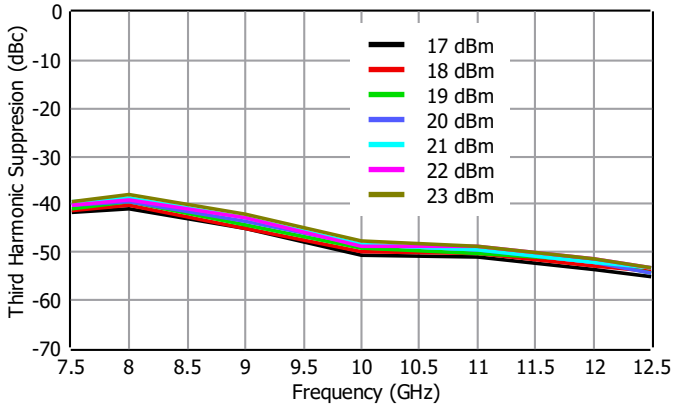
2nd Harmonic vs Pin, Frequency



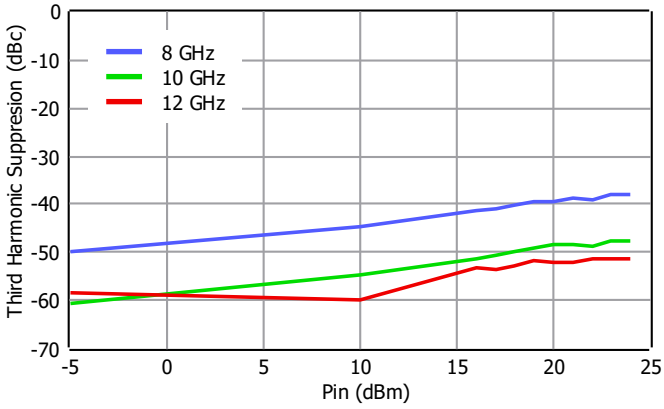
3rd Harmonic vs Vdd, Pin = +22 dBm



3rd Harmonic vs Frequency, Pin



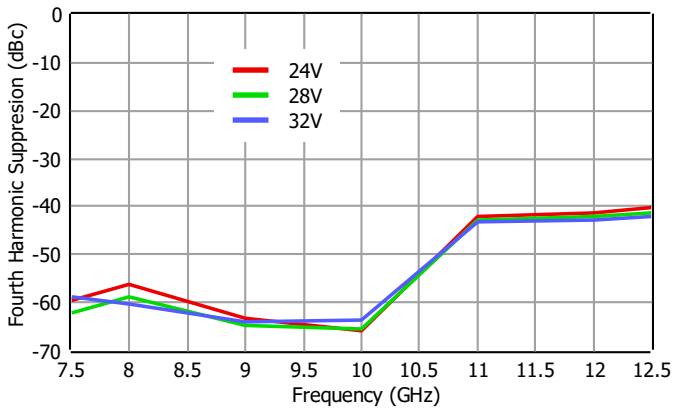
3rd Harmonic vs. Pin, Frequency



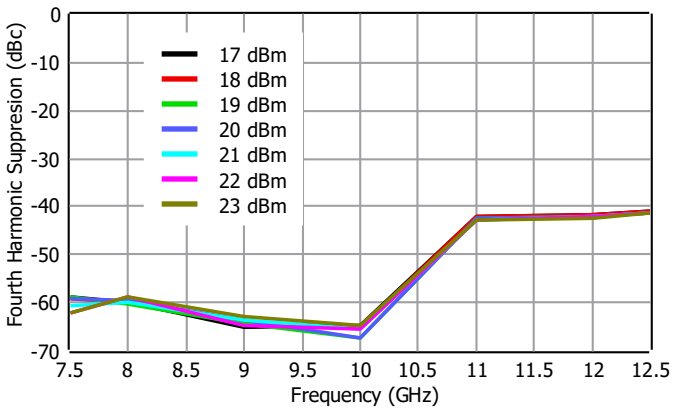
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 28 V, I_{DQ} = 200 mA, Typical, T = 25 C, CW.

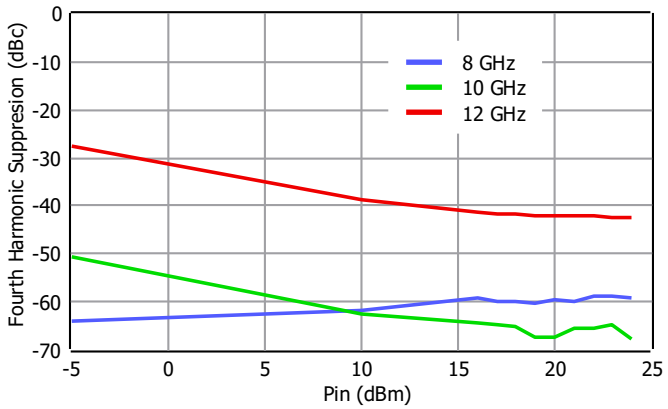
4th Harmonic vs Vdd, Pin = +22 dBm



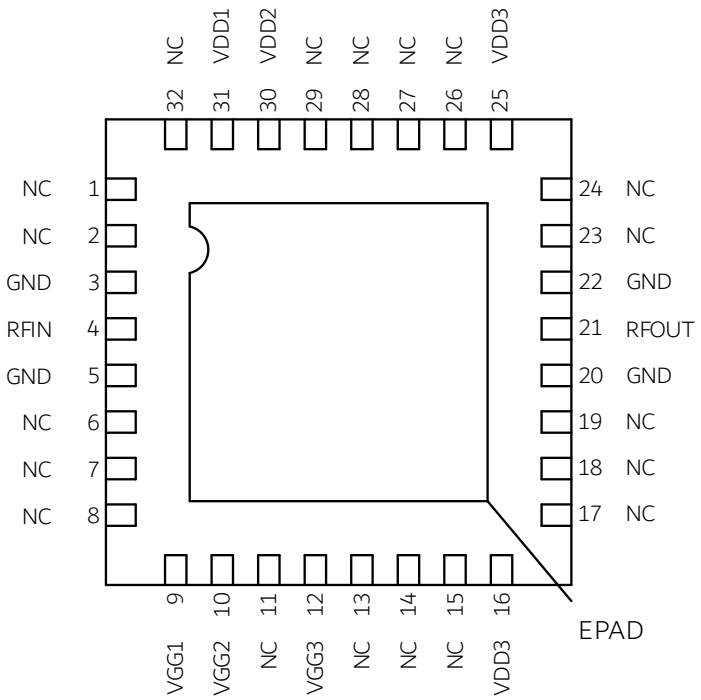
4th Harmonic vs Frequency, Pin



4th Harmonic vs Pin, Frequency



Pin Description

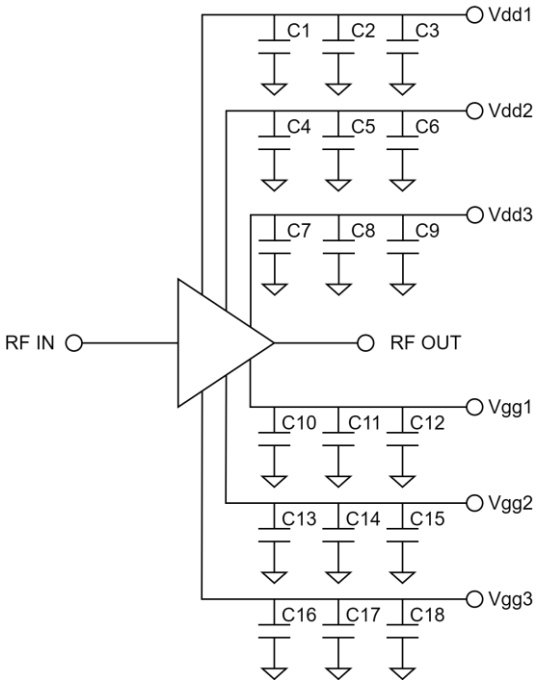


Top View

Pin Number	Pin Name	Description
4	RF IN	RF input pin. AC Coupled.
21	RF OUT	RF output pin. AC Coupled.
31	VDD1	Vdd supply pin for stage1.
30	VDD2	Vdd supply pin for stage2.
16, 25	VDD3	Vdd supply pin for stage3.
9	VGG1	Vgg bias pin for stage1.
10	VGG2	Vgg bias pin for stage2.
12	VGG3	Vgg bias pin for stage3.
1, 2, 6-8, 11, 13-15, 17-19, 23, 24, 26-29, 32	NC	These pins are not internally connected. Can be grounded on the PCB.
3, 5, 20, 22	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Applications Information

Signal entering from RF IN goes to RF OUT with an amplification.
A typical application schematic to operate the amplifier is given below.



C1 to C18 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 to C18 will improve this filtering.

All plots are generated with the ATEK581N5 mounted to a connectorized evaluation board. The PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

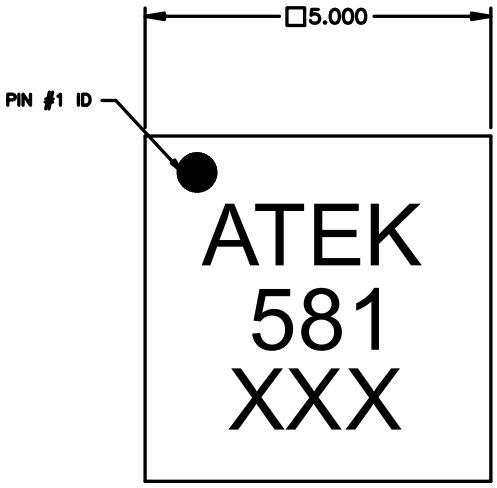
The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

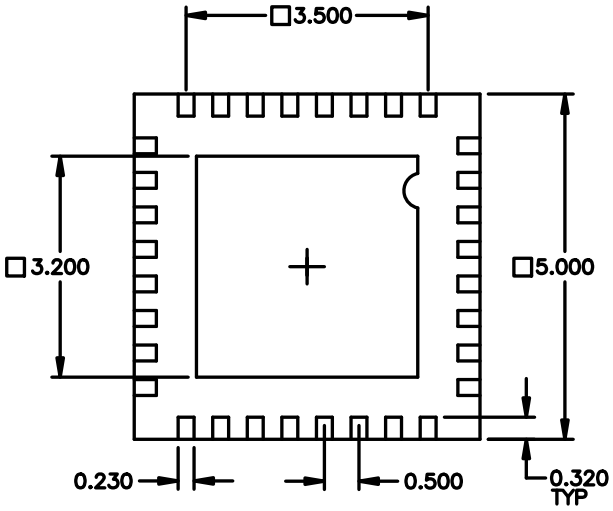
Parameter	Value /Range
Supply Voltage (Vdd)	+34V
Gate Voltage (Vg)	-5V min, 0V max
RF Input Power (Vdd = +28V)	+26dm
Channel Temperature	220 °C
Thermal Resistance	3.3 °C/W
Maximum Pulsed Power Dissipation (PDISS), Drain Bias Pulse Width=100us @10% Duty, TCASE 85°C, Derate 303mW/C above TCASE 85°C	40.9W
Storage Temperature	−55 to +125 °C
Operating Temperature	−40 to +85 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

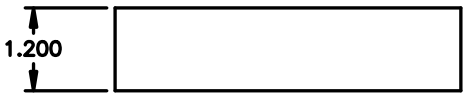
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. ALL DIMENSIONS IN MM

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

Notice

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
0.1	25.09.2025	Initial Release	
0.2	10.11.2025	Format and Content Fixed	
0.3	05.06.2025	Product Release, Format and Content Fixed	