RECOMMENDED FOR NEW DESIGNS

ATEK656BN5

2 - 18 GHz Switchable Band Pass Filter Bank

Product Description

The ATEK656BN5 is a high-performance, sub-octave GaAs MMIC switchable band pass filter bank that covers a wide frequency range of 2 to 18 GHz within a compact 5 x 5 mm SMD QFN package. Its internal architecture features an SP6T switch followed by 6 fixed-frequency bandpass filters and a secondary SP6T switch, with both the RF input and output internally matched to 50 ohms for straightforward system integration.

Operating this bi-directional filter bank requires a 3-bit, 0/-5V control signal to seamlessly cycle through its 6 discrete filter states while maintaining a passband insertion loss of approximately 7.5dB. Engineered for high-dynamic-range wideband receiver frontends, the device delivers a highly linear +32 dBm to +33 dBm IIP3, while its sub-octave configuration specifically targets and improves overall system IIP2 performance.

The ATEK656BN5 replaces the ATEK656N5.

Evaluation Board, custom package and module options are available upon request.

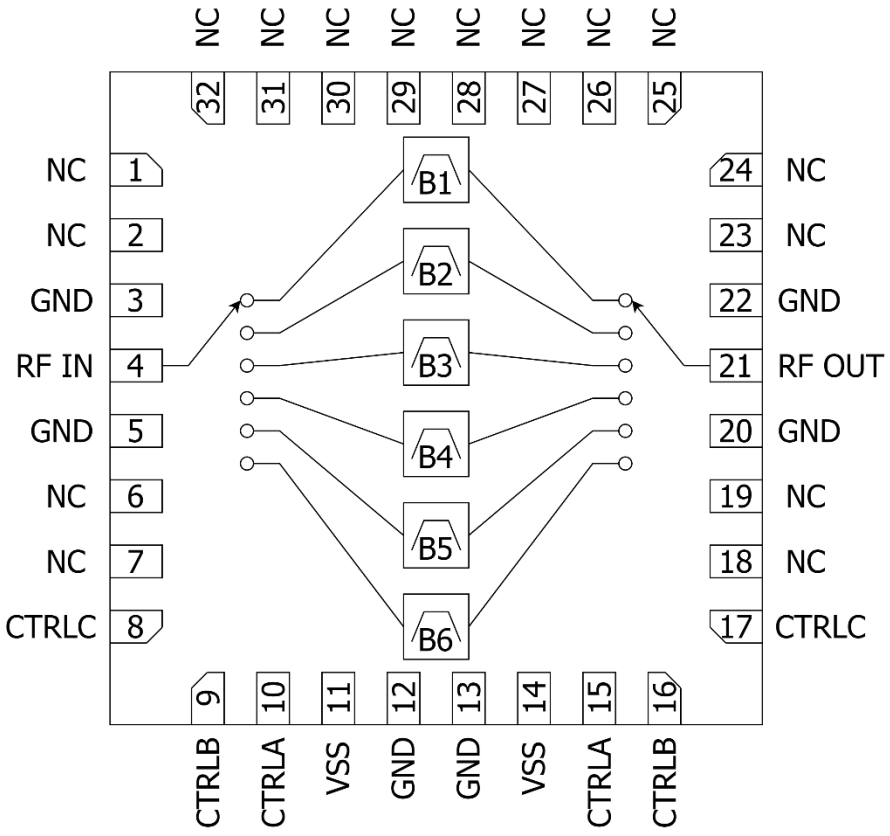
Product Features

- Frequency Range: 2 to 18 GHz
- 6 Switchable Band Pass Filters
- Rejection: -35 to -45dBc
- Tuning Speed: 130 ns
- Input IP3: +32 dBm
- 5x5mm Compact Size

Applications

- Wideband Receivers, SDRs
- Telecommunication
- Test and Measurement
- SATCOM
- EW / ECM / C-UAS

Functional Block Diagram



Electrical Specifications

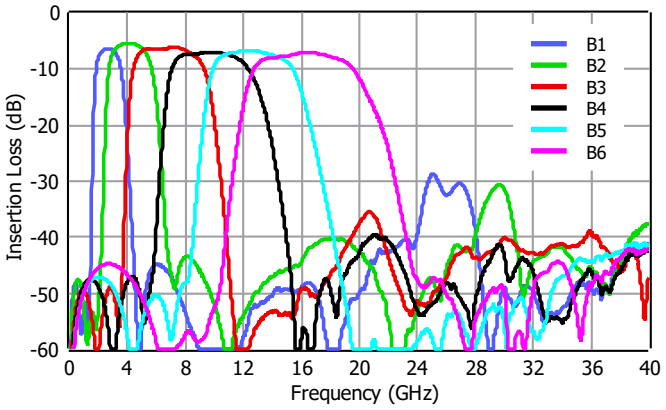
Conditions unless otherwise specified: V_{SS} = -5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		2		18	GHz
3dB Bandwidth (High Pass 3dB cutoff – Low Pass 3dB cutoff)	Band 1		2 – 3.5		GHz
	Band 2		2.8 – 5.4		
	Band 3		4.5 – 9		
	Band 4		7 – 12.3		
	Band 5		9.9 – 15.3		
	Band 6		12.8 – 19.3		
Insertion Loss	Band 1		7		dB
	Band 2		6.5		
	Band 3		7		
	Band 4		8		
	Band 5		8		
	Band 6		8.5		
Input Return Loss			-14		dB
Output Return Loss			-13		dB
Input IP3			32		dBm
Input P1dB			22		dBm
Switching Speed 50% Vctrl to 90% of RF Output	On		130		ns
	Off		15		
DC Supply Voltage (Vss)		-3	-5	-5.5	V
DC Supply Current			12		mA
Control Voltage (CTRL)	Low	0		-0.5	V
	High	-3		-5.5	
Control Supply Current (Total Ictrl)			0.3		mA
Operating Temperature		-40		85	°C

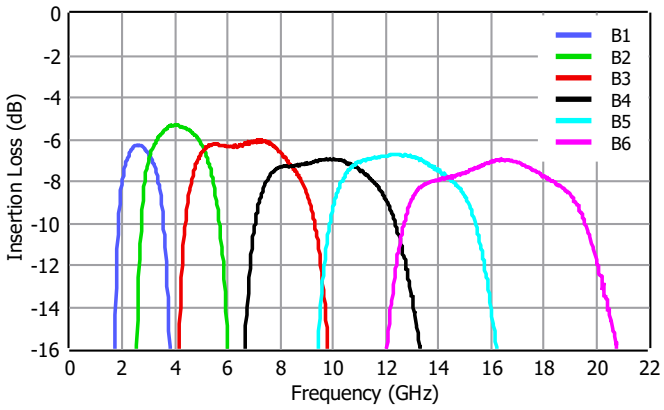
Typical Performance Plots

Conditions unless otherwise specified: V_{SS} = -5 V, Typical, T = 25 C, CW.

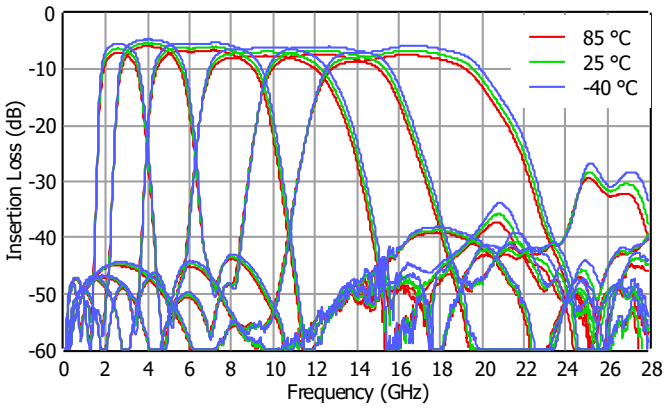
Insertion Loss



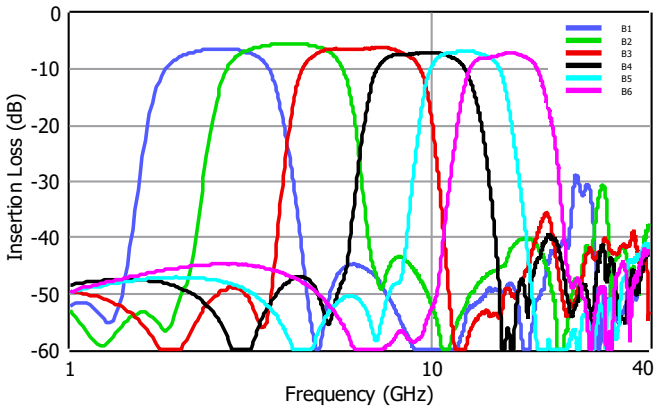
Insertion Loss, Zoom



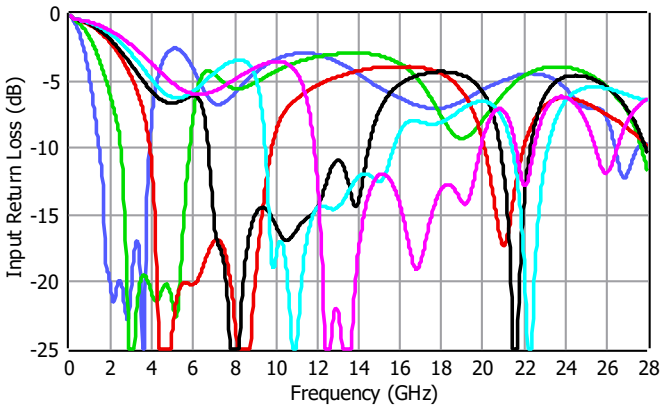
Insertion Loss vs Temperature



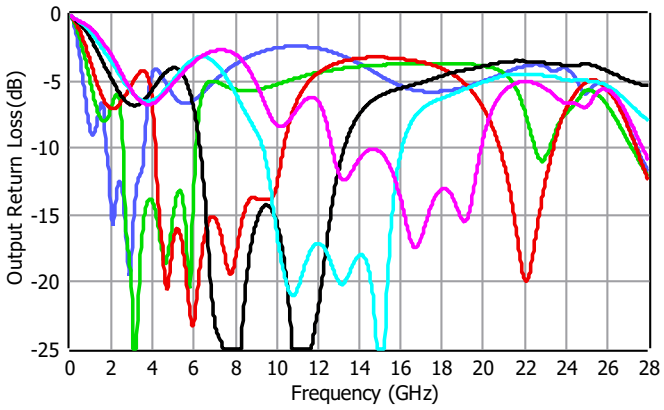
Insertion Loss, Log Scale



Input Return Loss



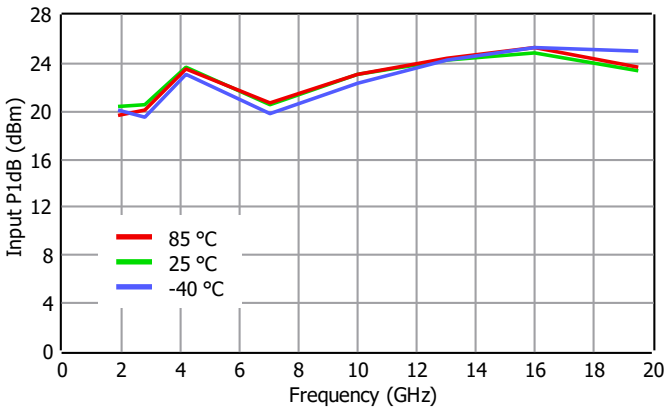
Output Return Loss



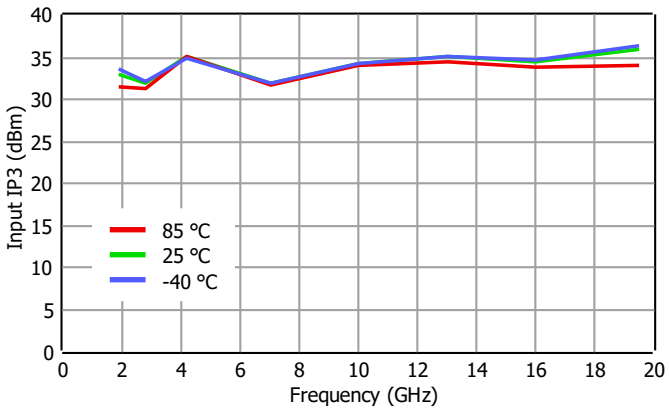
Typical Performance Plots

Conditions unless otherwise specified: V_{SS} = -5 V, Typical, T = 25 C, CW.

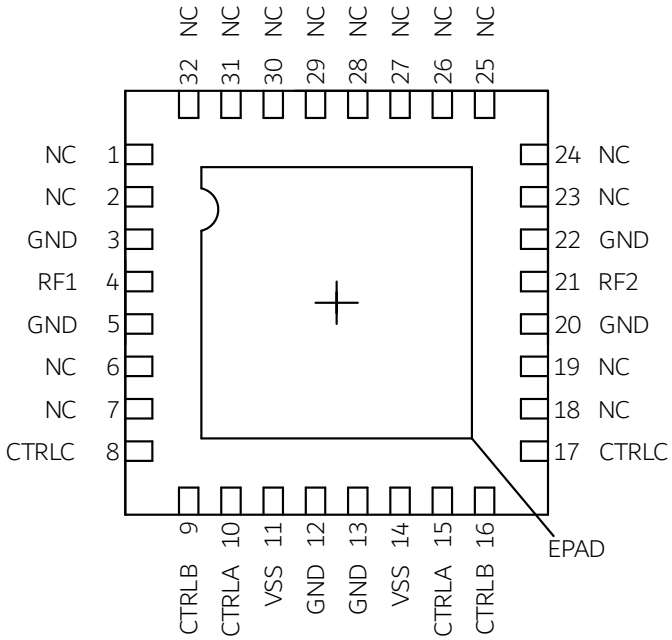
Input P1dB vs Temperature



Input IP3 vs Temperature



Pin Description



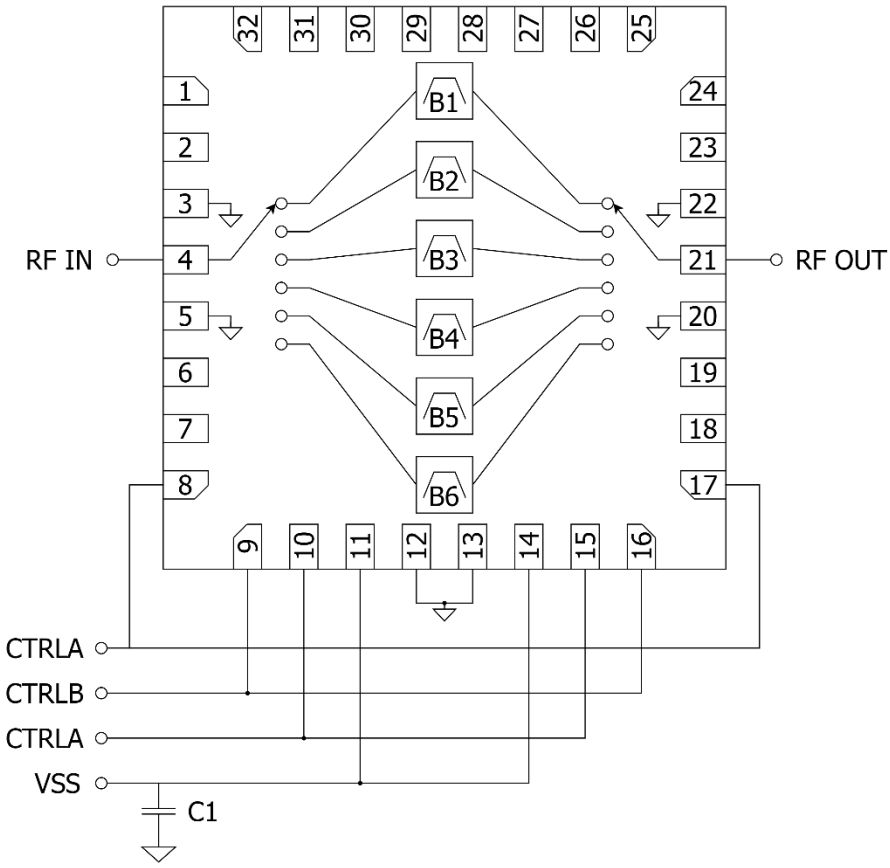
Pin Number	Pin Name	Description
4	RF1	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
21	RF2	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
11, 14	Vss	Voltage supply pin.
10, 15	CTRLA	Control pin. Two CTRLA pins are shorted internally. Using one of them is sufficient for controlling filter state.
9, 16	CTRLB	Control pin. Two CTRLB pins are shorted internally. Using one of them is sufficient for controlling filter state.
8, 17	CTRLC	Control pin. Two CTRLC pins are shorted internally. Using one of them is sufficient for controlling filter state.
1, 2, 6, 7, 18, 19, 23-32	NC	These pins are not internally connected. Can be grounded on the PCB.
3, 5, 12, 13, 20, 22	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

CTRLA	CTRLB	CTRLC	Filter Bank State
HIGH	HIGH	HIGH	Band1
LOW	HIGH	LOW	Band2
HIGH	LOW	HIGH	Band3
LOW	LOW	HIGH	Band4
LOW	HIGH	HIGH	Band5
HIGH	HIGH	LOW	Band6

Applications Information

Signal entering the RF1 pin goes into 6 selectable paths. All these paths are fixed frequency band pass filters.
A typical application schematic to operate the filterbank is given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vss supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then filterbank can be operated without C1.

Filterbank can be supplied in alternative packages and custom housing.

CTRL voltages are used for setting the switch state.

Small signal plots are gathered with probe PCB measurements, to generate data shown in this document, where RF1 is input and RF2 is the output.

Large signal data is generated with the ATEK656BN5 mounted to a connectorized evaluation PCB. The PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

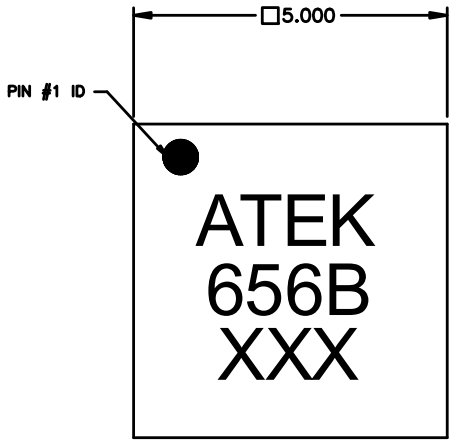
The NC pins of the Filterbank are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

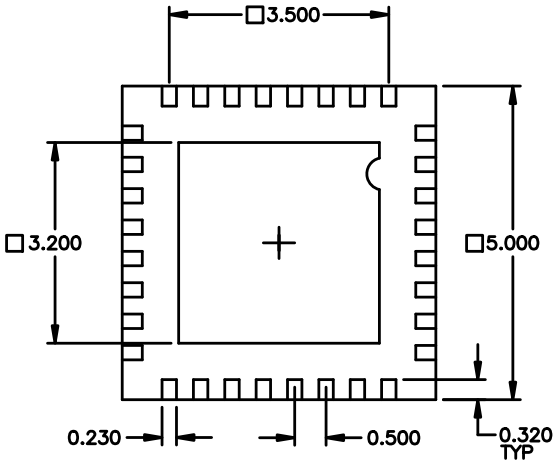
Parameter	Value/Range
Supply Voltage (Vss)	-6V
Vctrl	-6V
Supply Current (Iss)	18mA
Control Current (ICTRLA + ICTRLB + ICTRLC)	0.5mA
Channel Temperature	150 °C
Thermal Resistance	90 °C/W
RF Input Power (Vss= -5.0V)	+30dBm
Operating Temperature	−40 to +85 °C
Storage Temperature	−55 to +125 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

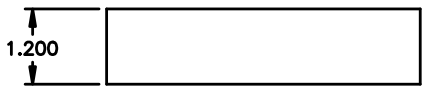
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. ALL DIMENSIONS IN MM
2. MARKING XXX INDICATES INTERNAL LOT CODE

Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
0.1	07.08.2026	Initial Release	
0.2	18.08.2026	Overtemp Data Added	
0.3	01.10.2026	Format and Content Fixed	