2 to 18 GHz Switchable Filter Bank w/Bypass

Product Description

ATEK672N5 is a GaAs MMIC filter bank with eight sub-octave filters offering fast <200nS tuning speed and excellent rejection of –50dBc from 2 to 18 GHz. Bypass ports are integrated to enable the addition of an external filter, through line, or amplification. The RF input and outputs are bidirectional and internally matched to 50 ohms for low SWaP transmit and receive applications.

The MMIC filter bank is powered by a single +5V supply drawing 18.5 mA with a 4-bit word controlling the selection of the 8 BPFs and bypass path.

Housed in 5x5 mm QFN surface mount package, the monolithic filter bank IC inherently minimizes phase noise degradation caused by mechanical vibration (microphonics).

MMICs and Evaluation Boards are available from stock. Custom package configurations, MMIC die, and module options are available upon request.

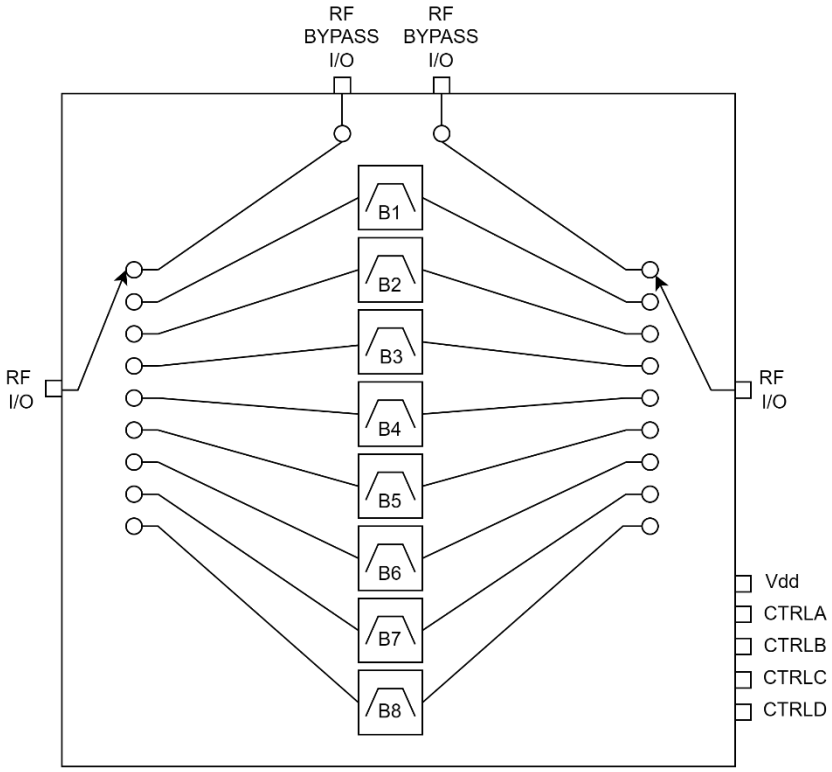
Product Features

- 8 Switchable Band Pass Filters
- Bypass Path for Off Chip Filter
- Excellent Rejection, -50dBc
- Fast Tuning Speed, <200nS
- Single +5V Supply
- 5x5 mm compact size

Applications

- Wideband Receivers & SDRs
- EW / ECM / C-UAS
- Telecom & SatCom
- Test & Measurement
- Ideal for Low SWaP

Functional Block Diagram



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Electrical Specifications

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range			2 - 18		GHz
3dB Bandwidth (High Pass 3dB cutoff – Low Pass 3dB cutoff)	Band 1 Band 2 Band 3 Band 4 Band 5 Band 6 Band 7 Band 8 External Bypass		1.7 – 4.3 3.5 - 6.4 5.5 - 8.5 7.3 – 10.6 9 – 12.9 11.1 – 14.9 12.4 – 17.4 14.8 – 19.5 LF - 18		dB
Insertion Loss	Filter Path Bypass Path		8 7		dB
Input Return Loss			-13		dB
Output Return Loss			-13		dB
Input IP3			43		dBm
Input P1dB			26		dBm
Switching Speed 50% Vctrl to 90% of RF Output	On Off		<200 <200		ns
0.1dB Settling Time			TBD		ns
DC Supply Voltage (Vdd)		3	5	5.5	V
DC Supply Current (Idd)			16		mA
Control Supply Current (Total Ictrl)			2.5		mA
Control Voltage (CTRL)	Low High	-0.1 3		0.5 5.5	V
Operating Temperature		-40		85	°C

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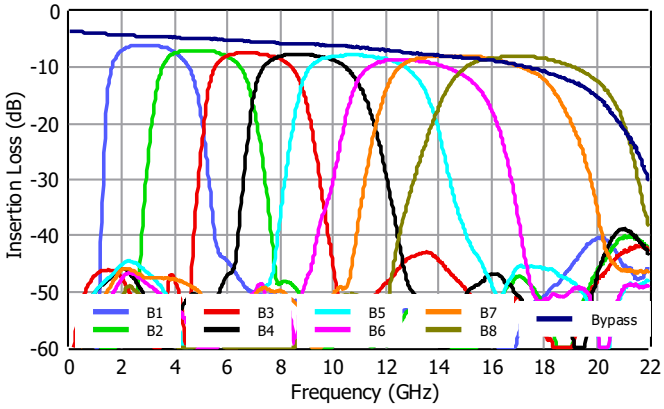
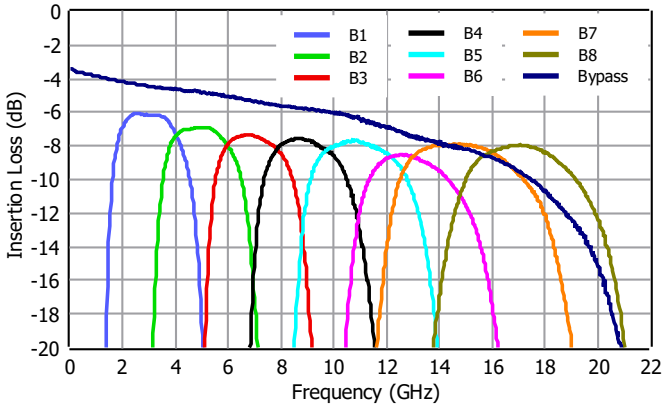
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

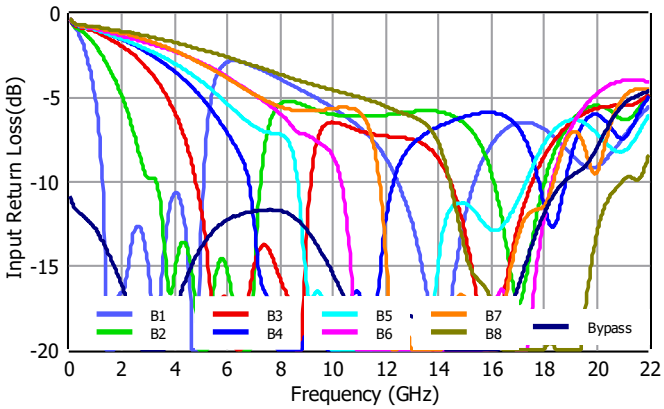
Insertion Loss



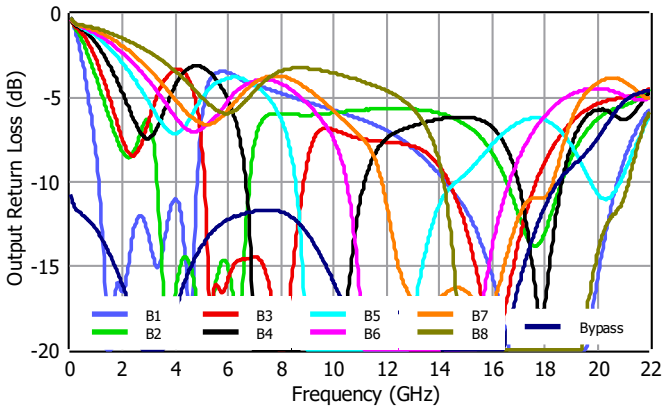
Insertion Loss, Zoom



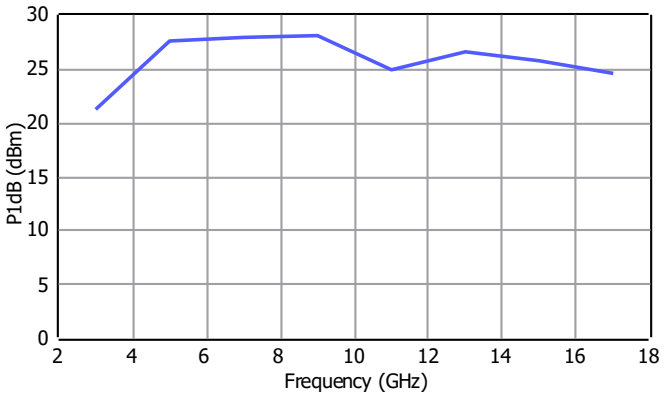
Input Return Loss



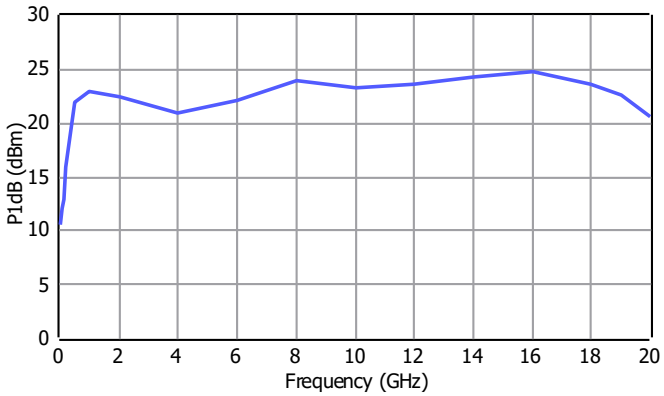
Output Return Loss



Input P1dB, Filter States



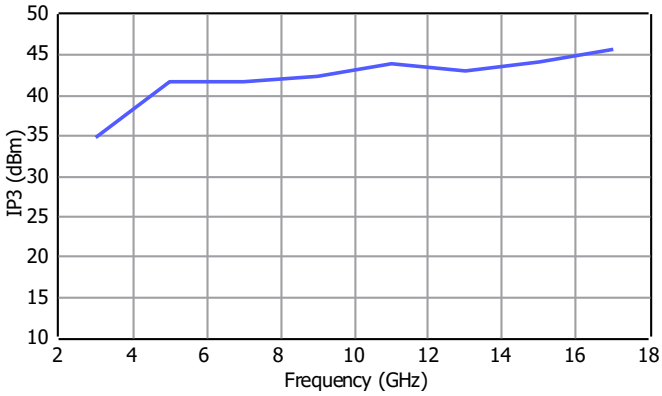
Input P1dB, Bypass State



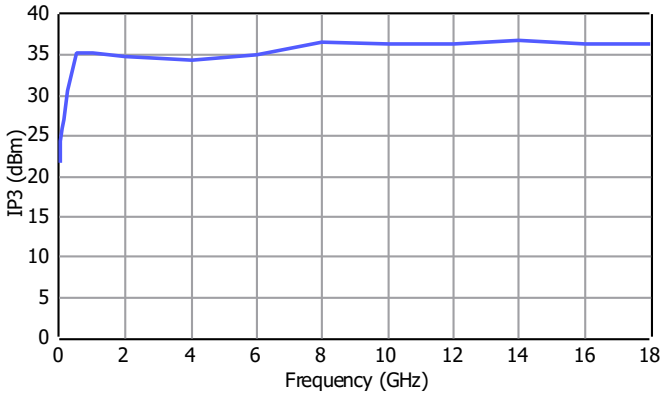
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

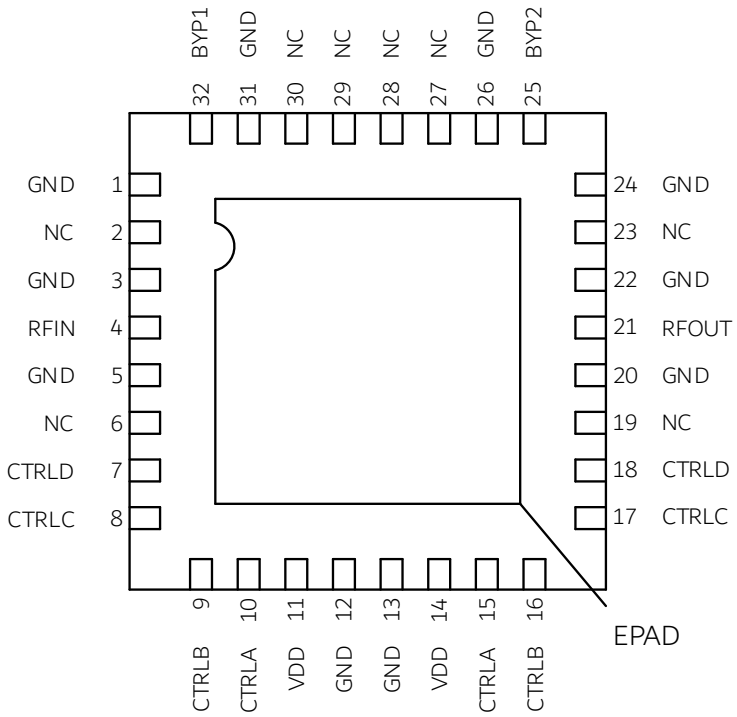
Input IP3, Filter States



Input IP3, Bypass State



Pin Description



Top View

Pin Number	Pin Name	Description
4	RF IN	RF input/output pin. DC coupled. Wideband external DC block capacitors are required.
21	RF OUT	RF input/output pin. DC coupled. Wideband external DC block capacitors are required.
32	BYP1	RF input/output pin. DC coupled. Wideband external DC block capacitors are required.
25	BYP2	RF input/output pin. DC coupled. Wideband external DC block capacitors are required.
11, 14	VDD	Vdd bias pin.
7, 18	CTRLD	Control D pin.
8, 17	CTRLC	Control C pin.
9, 16	CTRLB	Control B pin.
10, 15	CTRLA	Control A pin.
2, 6, 19, 23, 27-30	NC	These pins are not internally connected. Can be grounded on the PCB.
1, 3, 5, 12, 13, 20, 22, 24, 26, 31	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

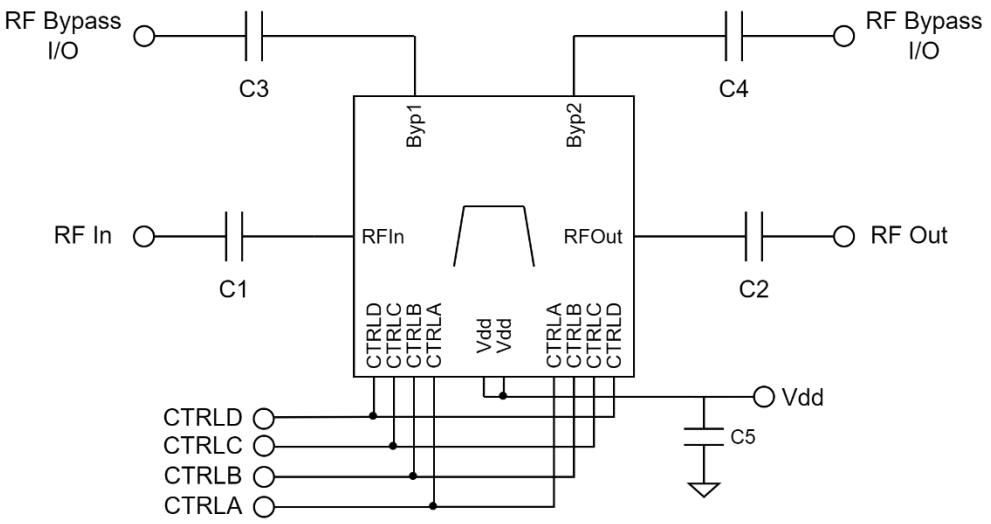
Control Interface

CTRLA	CTRLB	CTRLC	CTRLD	Filter Bank State
LOW	LOW	HIGH	LOW	Band1
LOW	LOW	LOW	HIGH	Band2
HIGH	LOW	LOW	HIGH	Band3
LOW	HIGH	LOW	HIGH	Band4
LOW	HIGH	HIGH	LOW	Band5
HIGH	HIGH	HIGH	LOW	Band6
HIGH	LOW	LOW	LOW	Band7
HIGH	LOW	HIGH	LOW	Band8
LOW	LOW	LOW	LOW	External Bypass State

Applications Information

Signal entering from RFIN pins goes into 9 selectable paths. 8 of these paths are fixed frequency band pass filters and the 9th path is routed to BYP1 pin. Symmetrical architecture lies between RFOUT and BYP2 pins. Thus, BYP1 and BYP2 pins can be used to add an off chip thru path to the PCB. This will allow users to add a bypass feature to the filterbank. Alternatively, a 9th filter can be connected between BYP1 and BYP2 pins. Similarly, BYP1 and BYP2 pins can be used to connect an alternative filterbank. This allows users to create filterbank configurations with higher filter counts in a modular architecture.

A typical application schematic to operate the filterbank is given below.



C1, C2, C3 and C4 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss. If RF3 and RF4 pins are not used, then using C3 and C4 is not required.

C5 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If these topics are of no concern, then filterbank can be operated without C5.

Small signal data plots are gathered with probe PCB measurements to generate plots shown in this document.

Large signal data are generated with connectorized evaluation of PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

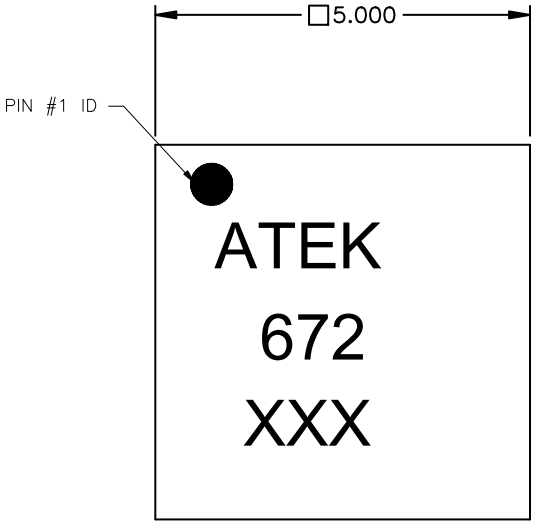
The NC pins of the Filterbank are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

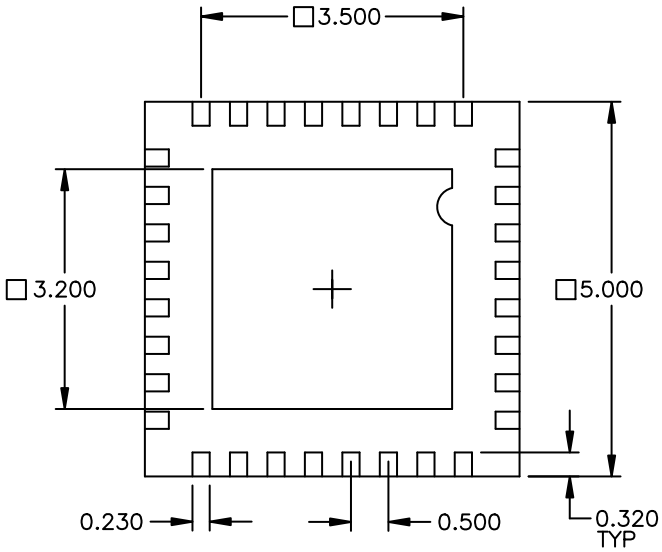
Parameter	Value/Range
Supply Voltage	+6V
VCTRL (VCTRLA, VCTRLB, VCTRLC) If VCTRL > VDD, then VCTRL – VDD must be lower than 2V	+6V
Supply Current	18mA
Control Current (ICTRLA+ICTRLB+ICTRLC+ ICTRLD)	4mA
Channel Temperature	+150 °C
Thermal Resistance	90 °C/W
RF Input Power (Vdd = +5.0V)	+30dBm
Storage Temperature	−55 to +125 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

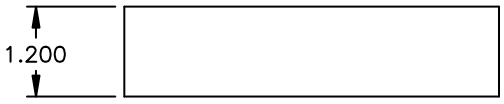
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. ALL DIMENSIONS IN MM

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
0.1	12.05.2026	Initial Release	
0.2	14.05.2026	Initial Release	
0.3	05.06.2026	Product Release, Format & Content Fixed	