*RECOMMENDED FOR NEW DESIGNS*

# ATEK673N5

## 4 to 23 GHz Switchable 6 BPF Bank w/Bypass

## Product Description

ATEK673N5 is a GaAs MMIC filter bank with six sub-octave filters offering fast <400nS tuning speed and excellent rejection of –45dBc from 4 to 23 GHz. Bypass ports are integrated to enable the addition of an external filter, through line, or amplification.

The RF input and outputs are bidirectional and internally matched to 50 ohms for low SWaP transmit and receive applications.

The MMIC filter bank is powered by a single +5V supply drawing 11 mA with a 4-bit word controlling the selection of the 6 BPFs and bypass path.

Housed in 5x5 mm QFN surface mount package, the monolithic filter bank IC inherently minimizes phase noise degradation caused by mechanical vibration (microphonics).

MMICs and Evaluation Boards are available from stock. Custom package configurations, MMIC die, and module options are available upon request.

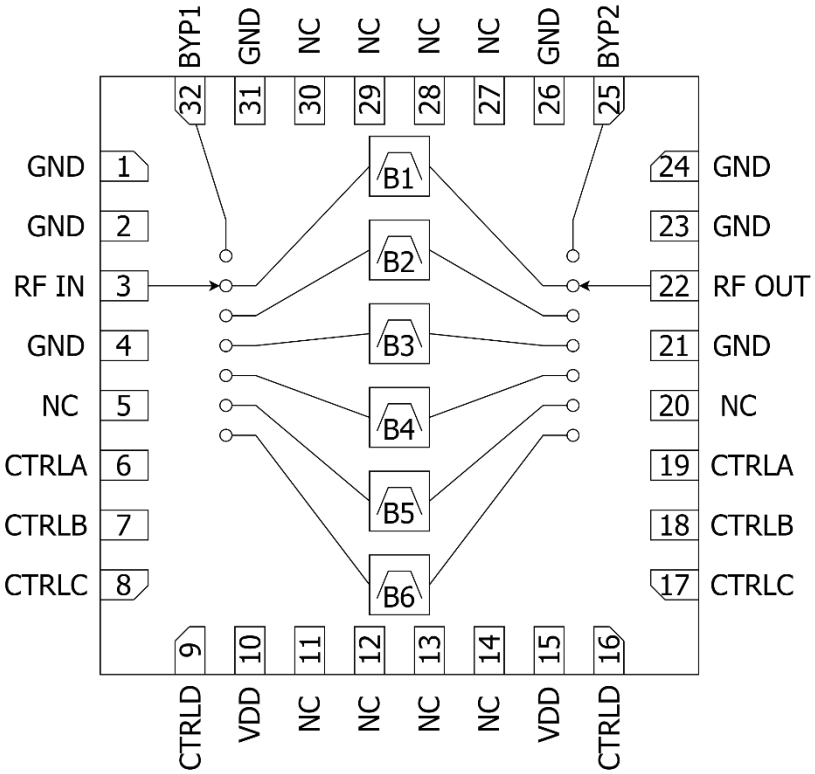
## Product Features

- 6 Switchable Band Pass Filters
- Bypass Path for External Filter
- Excellent Rejection: -45dBc
- Insertion Loss: 7 dB
- +5V @ 11mA Single Supply
- 5x5mm Compact Size

## Applications

- Wideband Receivers & SDRs
- EW / ECM / C-UAS
- Telecom & SatCom
- Test & Measurement
- Ideal for Low SWaP

## Functional Block Diagram



# 4 to 23 GHz Switchable 6 BPF Bank w/Bypass

## Electrical Specifications

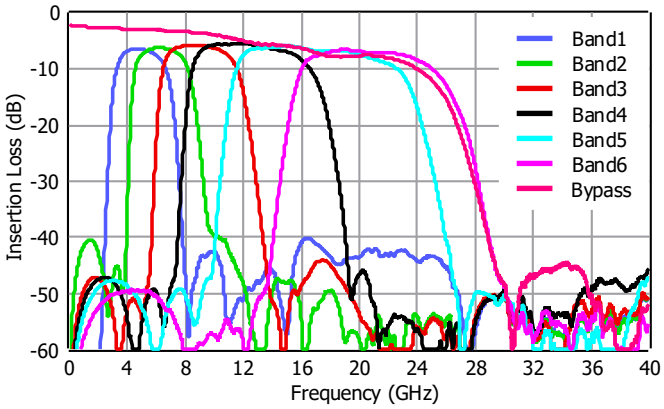
Conditions unless otherwise specified: $V_{DD}$ = 5 V, Typical, T = 25 C, CW.

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 4 | | 23 | GHz |
| 3dB Bandwidth<br>(High Pass 3dB cutoff – Low Pass 3dB cutoff) | Band 1<br>Band 2<br>Band 3<br>Band 4<br>Band 5<br>Band 6 | | 3.3 – 6.5<br>4.6 – 8<br>6.6 – 11.3<br>8.7 – 16<br>11.6 – 21.6<br>16 - 24.8 | | GHz |
| Insertion Loss | Filter Path<br>Bypass Path | | 7<br>7 | | dB |
| Input Return Loss | | | -13 | | dB |
| Output Return Loss | | | -13 | | dB |
| Input IP3 | | | 44 | | dBm |
| Input P1dB | | | 23 | | dBm |
| Switching Speed<br>50% Vctrl to 90% of RF Output | On<br>Off | | 370<br>125 | | ns |
| DC Supply Voltage (Vdd) | | 3 | 5 | 5.5 | V |
| DC Supply Current (Idd) | | | 11 | | mA |
| Control Supply Current (Total Ictrl) | | | 2.5 | | mA |
| Control Voltage (CTRL) | Low<br>High | -0.1<br>3 | | 0.5<br>5.5 | V |
| Operating Temperature | | -40 | | 85 | °C |

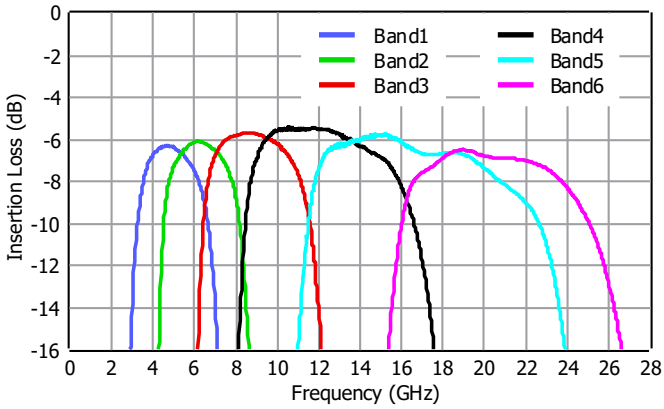
## Typical Performance Plots

Conditions unless otherwise specified: $V_{DD}$ = 5 V, Typical, T = 25 C, CW.

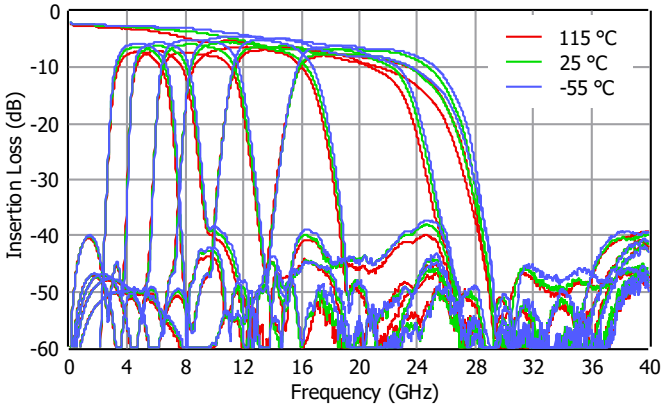
Insertion Loss



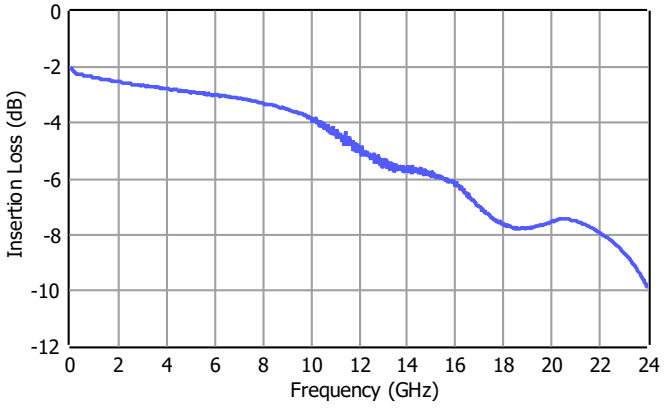

Insertion Loss, Zoom



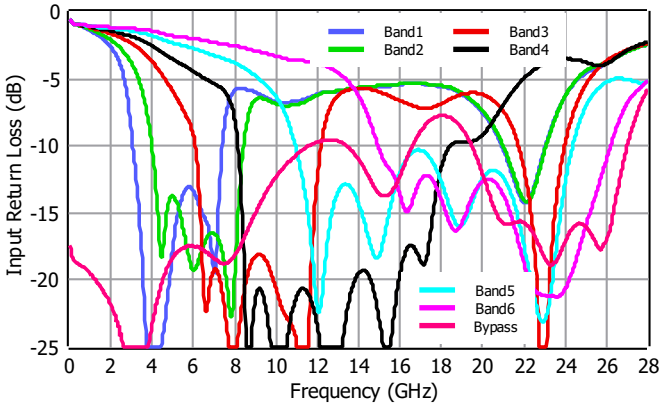

Insertion Loss vs Temperature



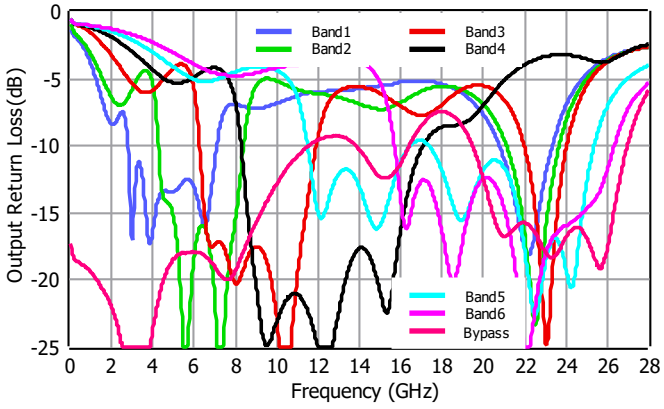

Insertion Loss, Bypass




Input Return Loss



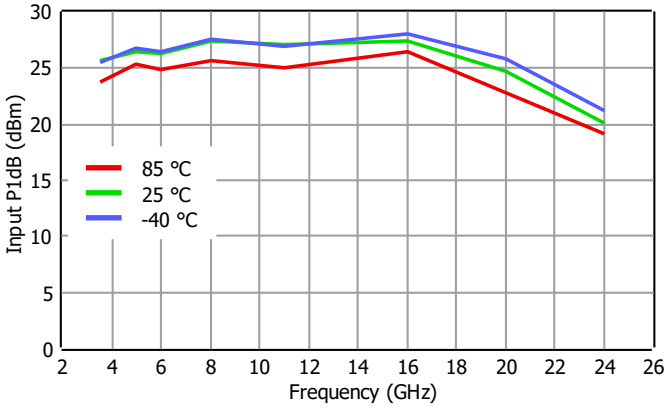

Output Return Loss



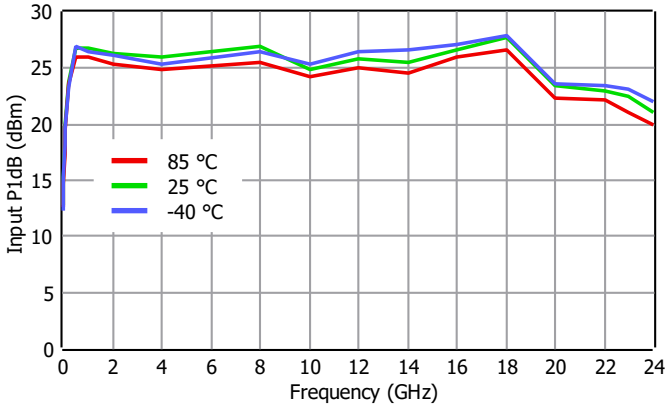
## Typical Performance Plots

Conditions unless otherwise specified: $V_{DD}$ = 5 V, Typical, T = 25 C, CW.

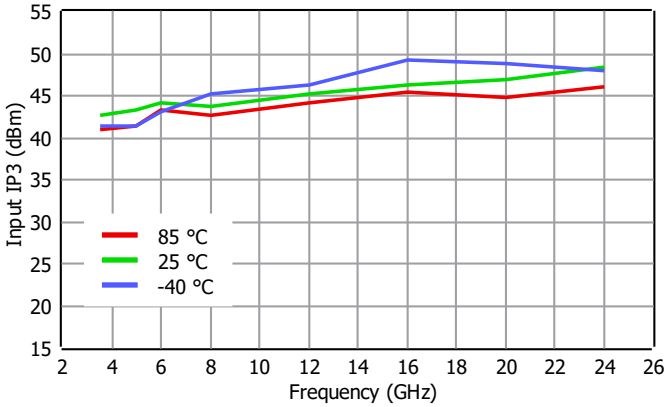
Input P1dB vs Temperature, Filter States



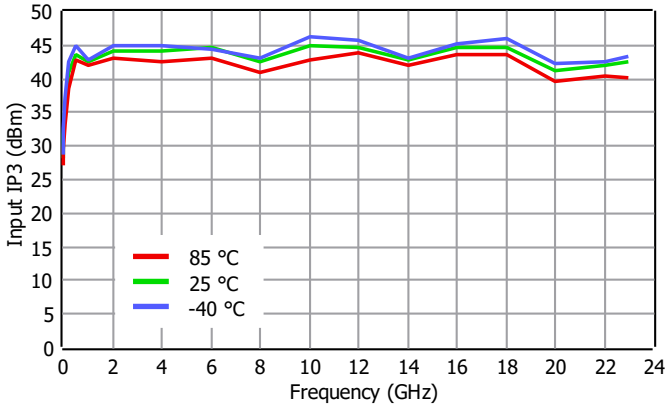

Input P1dB vs Temperature, Bypass State



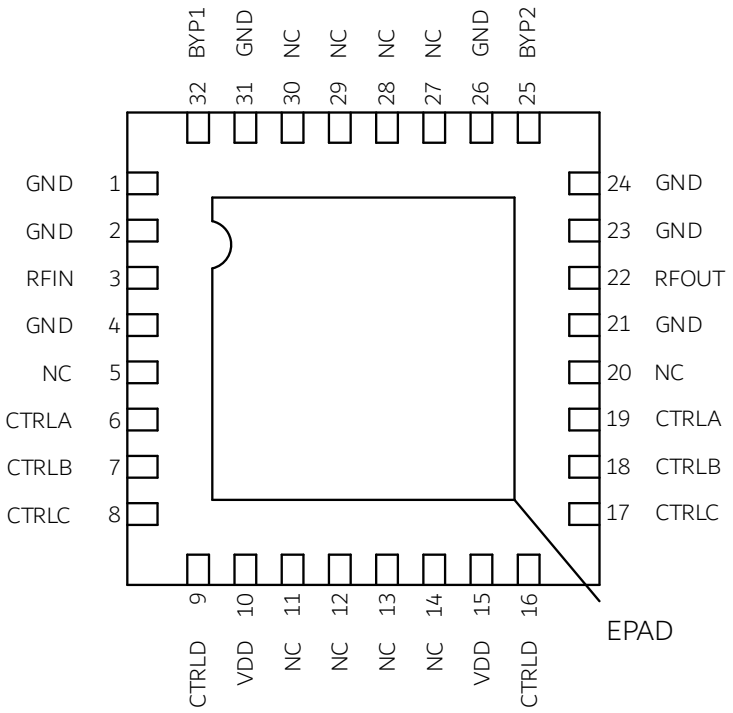

Input IP3 vs Temperature, Filter States




Input IP3 vs Temperature, Bypass State



## Pin Description (Top View)




| Pin Number | Pin Name | Description |
|---|---|---|
| 3 | RF IN | RF input/output pin. DC coupled. Wideband external DC block capacitors are required. |
| 22 | RF OUT | RF input/output pin. DC coupled. Wideband external DC block capacitors are required. |
| 32 | BYP1 | RF input/output pin. DC coupled. Wideband external DC block capacitors are required. |
| 25 | BYP2 | RF input/output pin. DC coupled. Wideband external DC block capacitors are required. |
| 10, 15 | VDD | Vdd bias pin. |
| 6, 19 | CTRLA | Control A pin. |
| 7, 18 | CTRLB | Control B pin. |
| 8, 17 | CTRLC | Control C pin. |
| 9, 16 | CTRLD | Control D pin. |
| 5, 11-14, 20, 27-30 | NC | These pins are not internally connected. Can be grounded on the PCB. |
| 1, 2, 4, 21, 23, 24, 26, 31 | GND | Ground. |
| 33 | EPAD | Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND. |

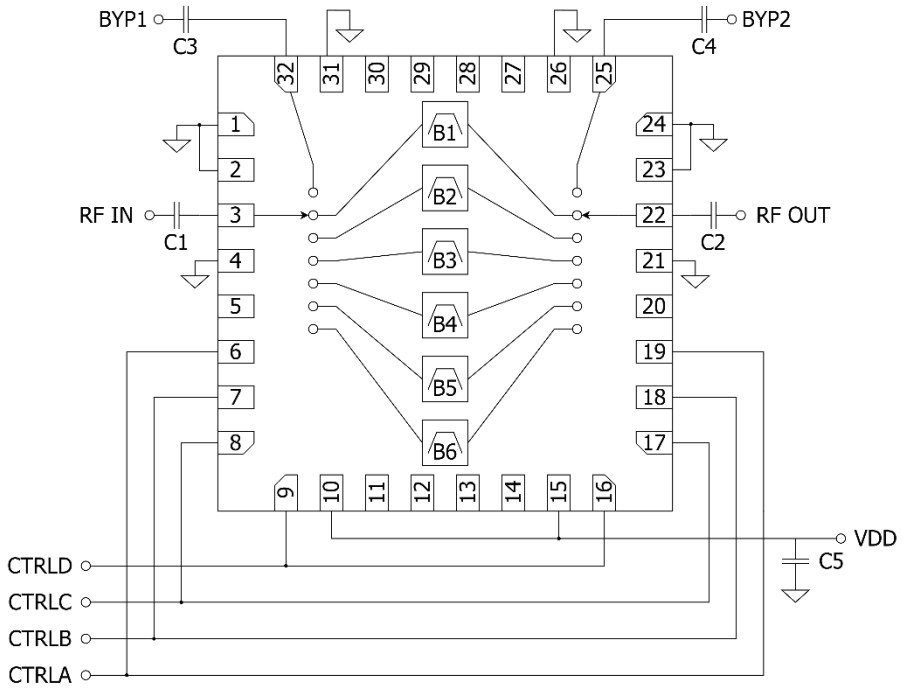
## Control Interface

| CTRLA | CTRLB | CTRLC | CTRLD | Filter Bank State |
|---|---|---|---|---|
| LOW | HIGH | HIGH | HIGH | Band1 |
| LOW | HIGH | HIGH | LOW | Band2 |
| HIGH | LOW | HIGH | LOW | Band3 |
| LOW | LOW | HIGH | LOW | Band4 |
| HIGH | LOW | LOW | LOW | Band5 |
| LOW | HIGH | LOW | LOW | Band6 |
| LOW | LOW | LOW | LOW | External Bypass State |

# 4 to 23 GHz Switchable 6 BPF Bank w/Bypass

## Applications Information

Signal entering from RF IN goes to RF OUT with band pass filtering.
A typical application schematic to operate the filter is given below.




C1, C2, C3, and C4 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

C5 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C5 will improve this filtering. If this filtering is of no concern, then filters can be operated without C5.

Small signal data plots are gathered with the ATEK673N5 mounted to an evaluation PCB to generate the plots shown in this document.

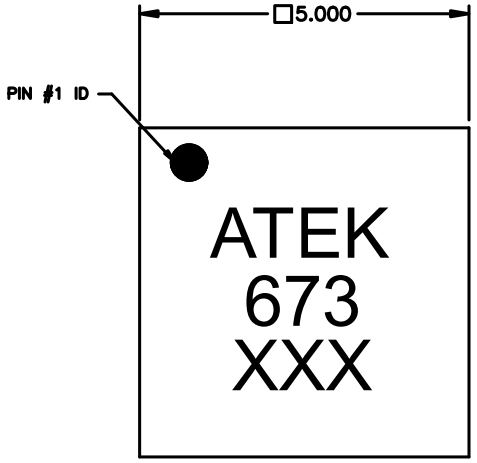
The NC pins of the filter are connected to the GND on the PCBs used to generate the plots shown in this document.

## Absolute Maximum Ratings

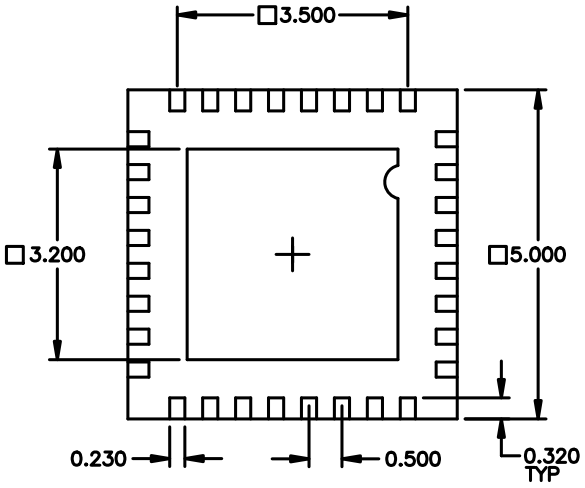
| Parameter | Value/Range |
|---|---|
| Supply Voltage | +6V |
| VCTRL (VCTRLA, VCTRLB, VCTRLC)<br>If VCTRL> VDD, then VCTRL – VDD must be lower than 2V. | +6V |
| Supply Current | 15mA |
| Control Current<br>(ICTRLA + ICTRLB + ICTRLC + ICTRLD) | 4mA |
| Channel Temperature | +150 °C |
| Thermal Resistance | 90 °C/W |
| RF Input Power (Vdd = +5.0V) | +30dBm |
| Storage Temperature | −55 to +125 °C |
| Operating Temperature | −40 to +85 °C |

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information




TOP VIEW




BOTTOM VIEW




SIDE VIEW

NOTES

1. ALL DIMENSIONS IN MM
2. MARKING XXX INDICATES INTERNAL LOT CODE

## Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

## Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

## Notice

This document and its contents are property of ATEK MIDAS. ATEK MIDAS has carefully reviewed the product specification information herein, and it is believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or errors, and the information within may be changed at any time without prior notice. Use of this information and/or any of our products does not convey to the user any patent rights or licenses. ATEK MIDAS products are designed to be used only within the electrical and environmental limits published in their respective data sheets or custom quoted specifications. ATEK MIDAS does not authorize the use of any of its products beyond the current published data sheet limits. Such use beyond the currently published electrical and/or environmental data sheet limits voids all ATEK MIDAS warranties. ATEK MIDAS reserves the right to change component circuitry, package material, assembly/test/inspect processes, specifications or other information at any time without prior notice. ATEK MIDAS shall have no responsibility for the customer's products, customer applications, and actions of the customer related to this product.

## Revisions

| Revision No | Revision Date | Revision Reason | Section / Page No |
|---|---|---|---|
| 0.1 | 06.06.2026 | Initial Release | |
| 0.2 | 07.06.2026 | Format Update | |
| 0.3 | 15.06.2026 | Plots Added | |
| 0.4 | 13.08.2026 | Large Signal and Overtemp Data Added | |
| 0.5 | 17.08.2026 | Format and Content Fixed | |
| 0.6 | 01.10.2026 | Format and Content Fixed | |