RECOMMENDED FOR NEW DESIGNS

ATEK897N4

18 to 26 GHz Digitally Tunable Band Pass Filter

Product Description

ATEK897N4 is a GaAs MMIC digitally tunable band pass filter offering low 8dB in-band loss and excellent rejection of –40 to –30 dBc from 18 to 26 GHz.

The RF input and outputs are bidirectional and internally matched to 50 ohms for low SWaP transmit and receive applications.

The MMIC filter bank is powered by a single +5V supply drawing 9 mA with an 8-bit GPIO control interface selecting 256 filter states.

Housed in 4x4 mm QFN surface mount package, the monolithic filter bank IC inherently minimizes phase noise degradation caused by mechanical vibration (microphonics).

MMICs and Evaluation Boards are available from stock. Custom package configurations, MMIC die, and module options are available upon request.

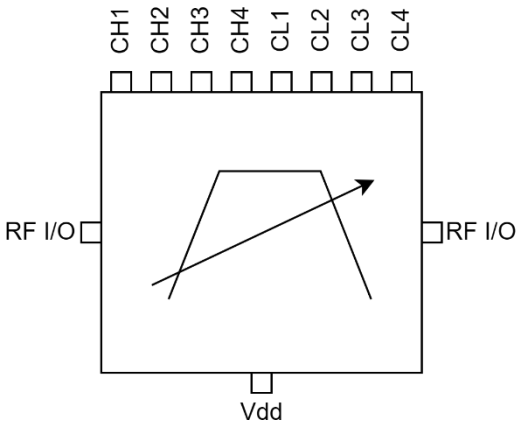
Product Features

- 256 Filter States, 18 to 26 GHz
- High Rejection, -40 dBc
- Fast Tuning Speed, <200 nS
- P1dB: +28 dBm
- Single +5V @ 9mA Supply
- 4x4 mm compact size

Applications

- Wideband Receivers & SDRs
- EW / ECM / C-UAS
- Telecom & SatCom
- Test & Measurement
- Ideal for Low SWaP

Functional Block Diagram



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Electrical Specifications

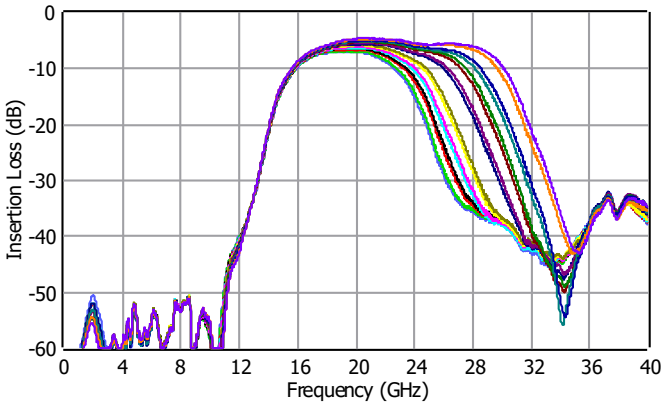
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		17	18 - 26	29	GHz
Insertion Loss			8		dB
Input Return Loss			-7		dB
Output Return Loss			-10		dB
Input IP3			45		dBm
Input P1dB			28		dBm
Switching Speed 50% Vctrl to 90% of RF Output	On Off		<200 <200		nS
0.1dB Settling Time			TBD		nS
DC Supply Voltage (Vdd)			5		V
DC Supply Current (Idd)			9		mA
Control Voltage (CTRL)	Low High	-0.1 2.5		0.5 5.5	V
Control Current (Ictrl)			5.5		mA
Operating Temperature		-40		85	°C

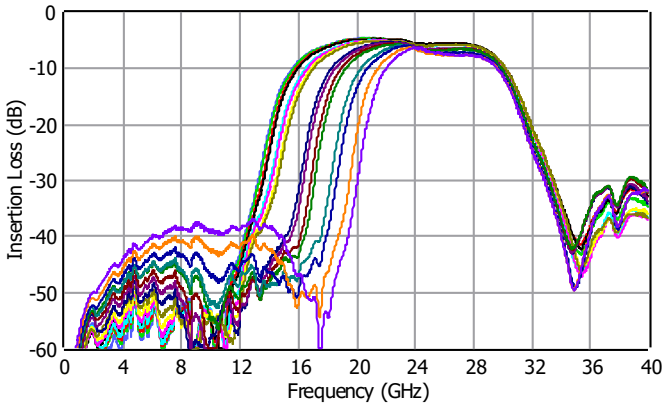
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

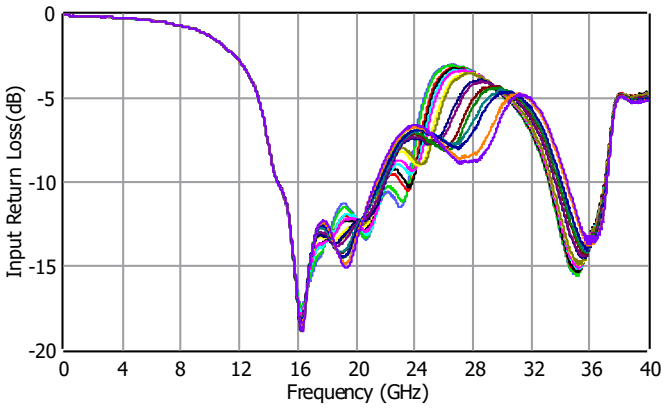
Insertion Loss, Low Pass Tuning



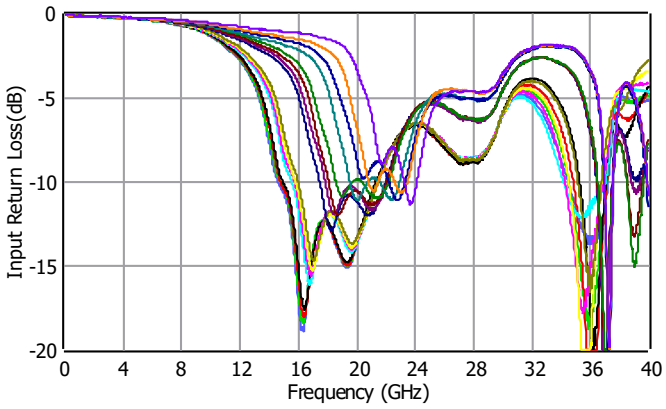
Insertion Loss, High Pass Tuning



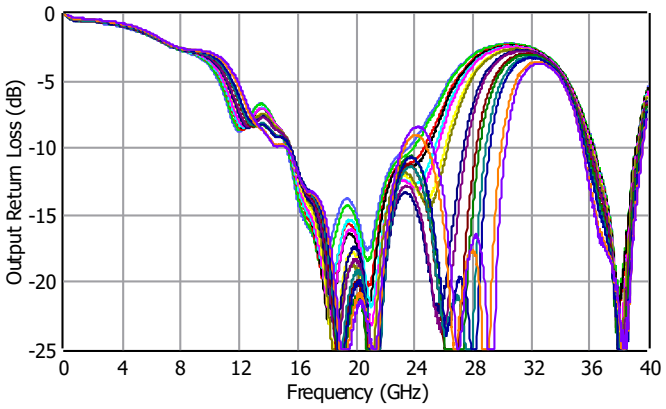
Input Return Loss, Low Pass Tuning



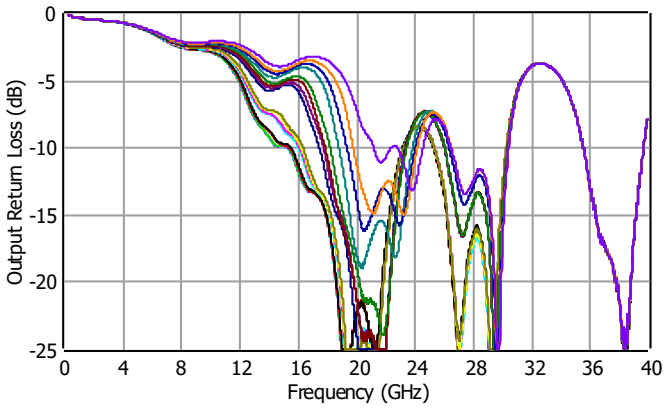
Input Return Loss, High Pass Tuning



Output Return Loss, Low Pass Tuning



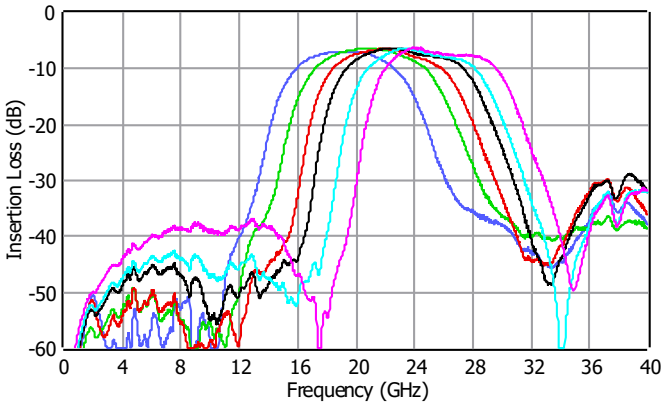
Output Return Loss, High Pass Tuning



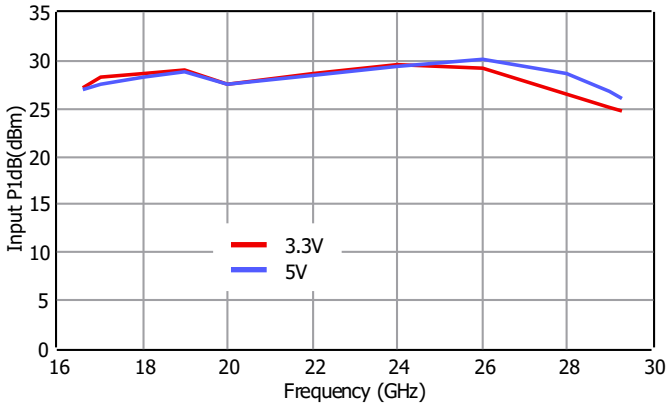
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

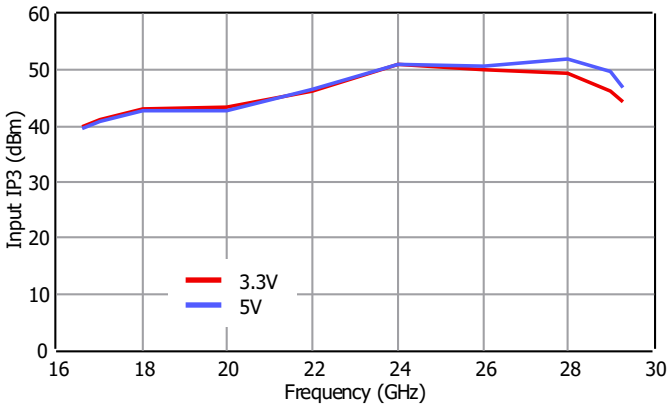
Insertion Loss



Input P1dB at Widest Bandwith

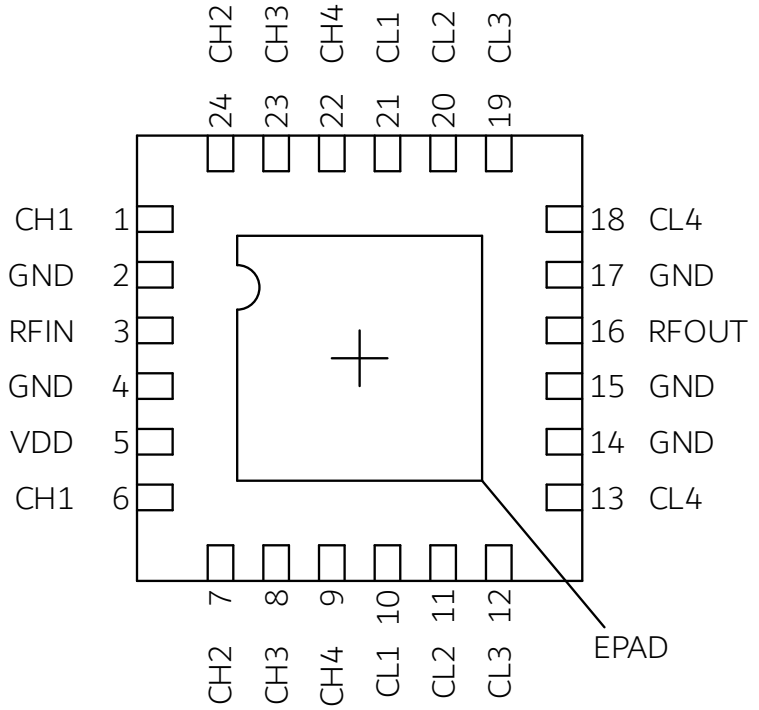


Input IP3 at Widest Bandwith



18 to 26 GHz Digitally Tunable Band Pass Filter

Pin Description



Pin Number	Pin Name	Description
3	RF IN	RF input/output pin. AC coupled.
16	RF OUT	RF input/output pin. AC coupled.
6	VDD	Vdd supply pin.
1, 6	CH1	High Pass Control Pin1
7, 24	CH2	High Pass Control Pin2
8, 23	CH3	High Pass Control Pin3
9, 22	CH4	High Pass Control Pin4
10, 21	CL1	Low Pass Control Pin1
11, 20	CL2	Low Pass Control Pin2
12, 19	CL3	Low Pass Control Pin3
13, 18	CL4	Low Pass Control Pin4
2, 4, 14, 15, 17	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

H4	H3	H2	H1	Typical High Pass 3dB Cutoff Frequency (GHz)	L4	L3	L2	L1	Typical Low Pass 3dB Cutoff Frequency (GHz)
LOW	LOW	LOW	LOW	16.45	LOW	LOW	LOW	LOW	22.6
LOW	LOW	LOW	HIGH	16.55	LOW	LOW	LOW	HIGH	22.75
LOW	LOW	HIGH	LOW	16.75	LOW	LOW	HIGH	LOW	23.0
LOW	LOW	HIGH	HIGH	16.85	LOW	LOW	HIGH	HIGH	23.15
LOW	HIGH	LOW	LOW	17.3	LOW	HIGH	LOW	LOW	23.5
LOW	HIGH	LOW	HIGH	17.45	LOW	HIGH	LOW	HIGH	23.65
LOW	HIGH	HIGH	LOW	17.65	LOW	HIGH	HIGH	LOW	24.0
LOW	HIGH	HIGH	HIGH	17.8	LOW	HIGH	HIGH	HIGH	24.15
HIGH	LOW	LOW	LOW	18.85	HIGH	LOW	LOW	LOW	25.25
HIGH	LOW	LOW	HIGH	19.1	HIGH	LOW	LOW	HIGH	25.5
HIGH	LOW	HIGH	LOW	19.4	HIGH	LOW	HIGH	LOW	26.3
HIGH	LOW	HIGH	HIGH	19.7	HIGH	LOW	HIGH	HIGH	26.6
HIGH	HIGH	LOW	LOW	20.7	HIGH	HIGH	LOW	LOW	27.25
HIGH	HIGH	LOW	HIGH	21.1	HIGH	HIGH	LOW	HIGH	27.65
HIGH	HIGH	HIGH	LOW	21.6	HIGH	HIGH	HIGH	LOW	28.8
HIGH	HIGH	HIGH	HIGH	22.2	HIGH	HIGH	HIGH	HIGH	29.2

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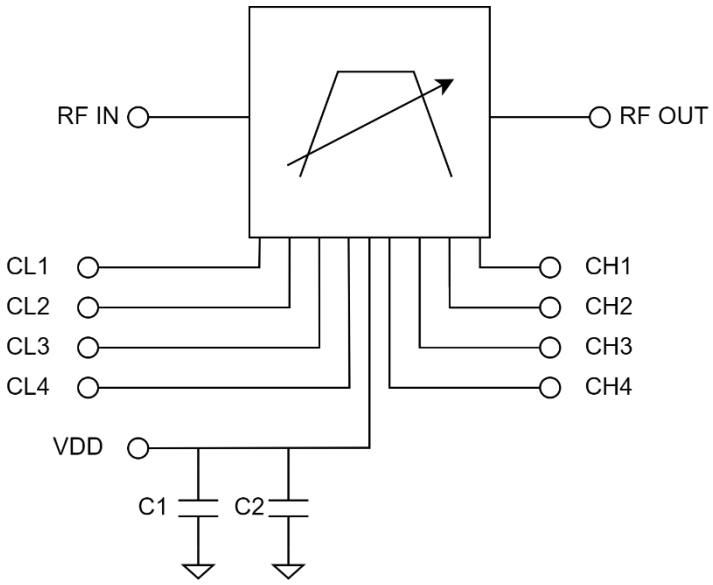
Applications Information

Signal entering from RF input goes to RF output with band pass filtering.
Typical application schematic to operate the filter is given below.



C1 and C2 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 and C2 will improve this filtering. If this filtering is of no concern, then filters can be operated without C1 and C2.

Small signal data plots are gathered with probe PCB measurements to generate plots shown in this document.

Large signal data are generated with connectorized evaluation PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

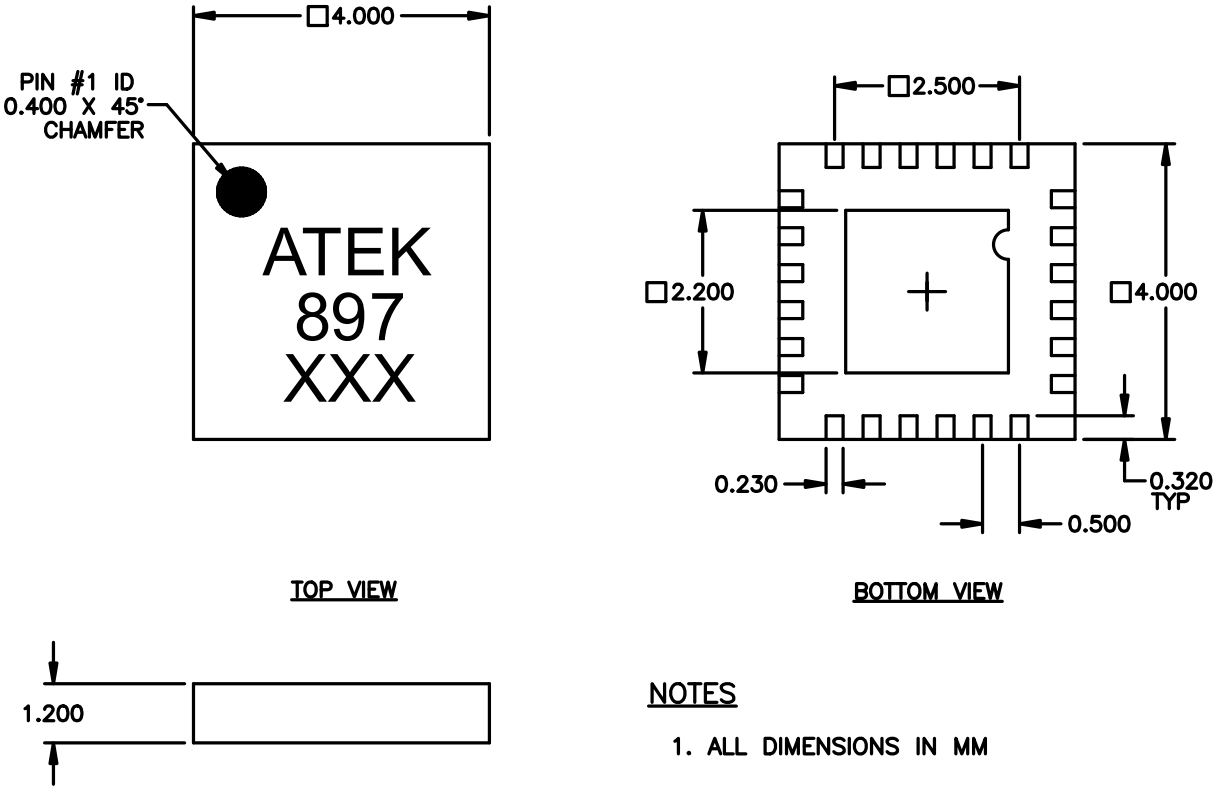
The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

Paramete	Value/Range
Supply Voltage	+6.0V
VCTRL (VCTRLA, VCTRLB, VCTRLC) If VCTRL> VDD, then VCTRL – VDD must be lower than 2V.	+6.0V
Supply Current	10.5mA
Control Current (ICTRLA + ICTRLB + ICTRLC)	7.2mA
Channel Temperature	150 °C
Thermal Resistance	90 °C/W
RF Input Power	+30dBm
Storage Temperature	−55 to +125 °C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

Notice

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
0.1	12.05.2026	Initial Release	
0.2	04.06.2026	Format and Content Fixed	
0.3	05.06.2026	Product Release, Format and Content Fixed	