C3M0015065D

Silicon Carbide Power MOSFET
C3M^{TM} MOSFET Technology
N-Channel Enhancement Mode

Features

- 3rd Generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)
- Halogen free, RoHS compliant

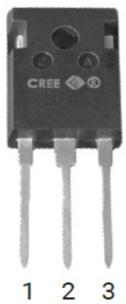
Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Applications

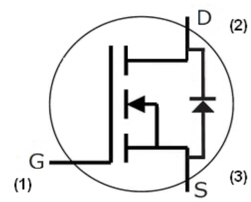
- EV charging
- Solar PV Inverters
- UPS
- SMPS
- DC/DC converters

Package



Halogen-Free

RoHS



Part Number	Package	Marking
C3M0015065D	TO-247-3	C3M0015065D

Maximum Ratings (T_C=25˚C, unless otherwise specified)

Symbol	Parameter	Value	Unit	Note
V_{DSmax}	Drain - Source Voltage	650	V	
V_{GSmax}	Gate - Source voltage	-8/+19	V	Note 1
I_D	Continuous Drain Current, V_{GS} = 15 V, T_C = 25˚C	120	A	Fig. 19 Note 2
	Continuous Drain Current, V_{GS} = 15 V, T_C = 100˚C	96		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}	418	A	
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C	416	W	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +175	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s	260	˚C	
M_d	Mounting Torque, (M3 or 6-32 screw)	1 8.8	Nm lbf-in	

Note (1): Recommended turn off / turn on gate voltage V_{GS} -4V...0V / +15V
Note (2): Package limited to 120 A

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 15.5 mA	Fig. 11
			1.9		V	V_{DS} = V_{GS}, I_D = 15.5 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance	10.5	15	21	mΩ	V_{GS} = 15 V, I_D = 55.8A	Fig. 4, 5,6
			20			V_{GS} = 15 V, I_D = 55.8A, T_J = 175ºC	
g_{fs}	Transconductance		42		S	V_{DS}= 20 V, I_{DS}= 55.8 A	Fig. 7
			40			V_{DS}= 20 V, I_{DS}= 55.8 A, T_J = 175ºC	
C_{iss}	Input Capacitance		5011		pF	V_{GS} = 0 V, V_{DS} = 400 V f = 100 Khz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		289				
C_{rss}	Reverse Transfer Capacitance		31				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		357				Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		516				Note: 3
E_{oss}	C_{oss} Stored Energy		29		μJ		Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		1500		μJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L= 57.6 μH, T_J = 175ºC FWD = Internal Body Diode of MOSFET	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		700				
E_{ON}	Turn-On Switching Energy (External Diode)		1200		μJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L= 57.6 μH, T_J = 175ºC FWD = External SiC DIODE	Fig. 25
E_{OFF}	Turn Off Switching Energy (External Diode)		1000				
$t_{d(on)}$	Turn-On Delay Time		22		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L= 57.6 μH Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		125				
$t_{d(off)}$	Turn-Off Delay Time		58				
t_f	Fall Time		25				
$R_{G(int)}$	Internal Gate Resistance		1.5		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		54		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 55.8 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		62				
Q_g	Total Gate Charge		188				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

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Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.7		V	V_{GS} = -4 V, I_{SD} = 27.9 A, T_J = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 27.9 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		79	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S, pulse}$	Diode pulse Current		418	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recovery time	85		ns	V_{GS} = -4 V, I_{SD} = 55.8 A, V_R = 400 V dif/dt = 1500 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	667		nC		
I_{rrm}	Peak Reverse Recovery Current	17		A		
t_{rr}	Reverse Recovery time	74		ns	V_{GS} = -4 V, I_{SD} = 55.8 A, V_R = 400 V dif/dt = 1000 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	562		nC		
I_{rrm}	Peak Reverse Recovery Current	14		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.35	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

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Typical Performance

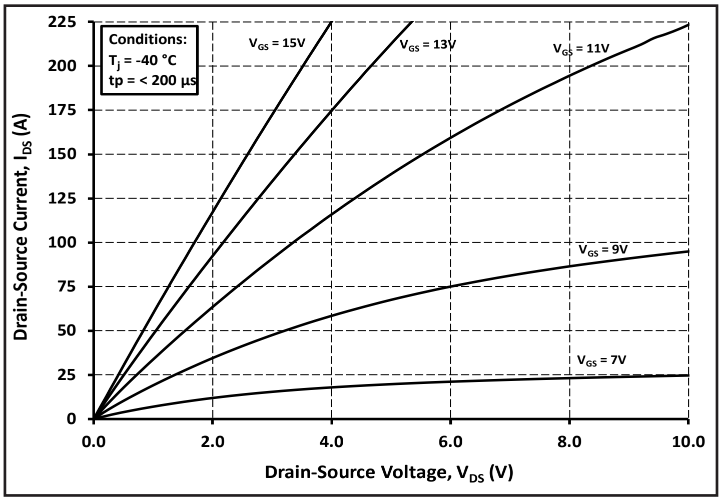

Figure 1. Output Characteristics T_J = -40 °C

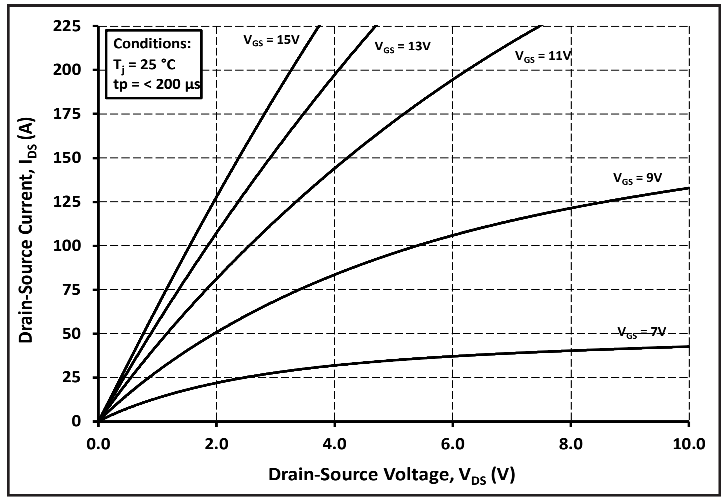

Figure 2. Output Characteristics T_J = 25 °C

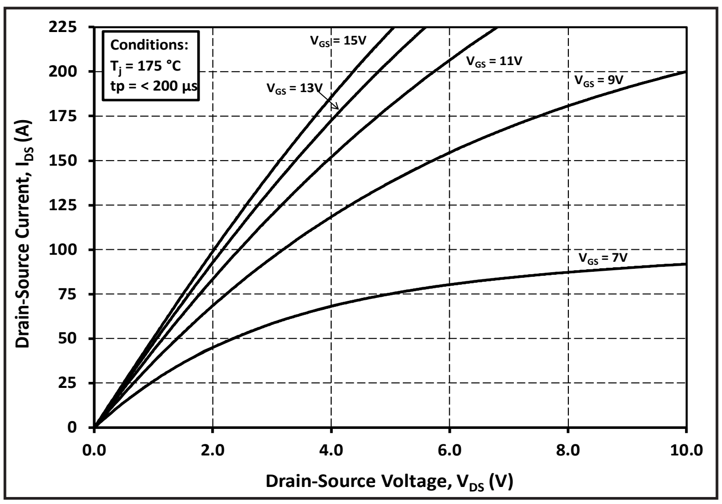

Figure 3. Output Characteristics T_J = 175 °C

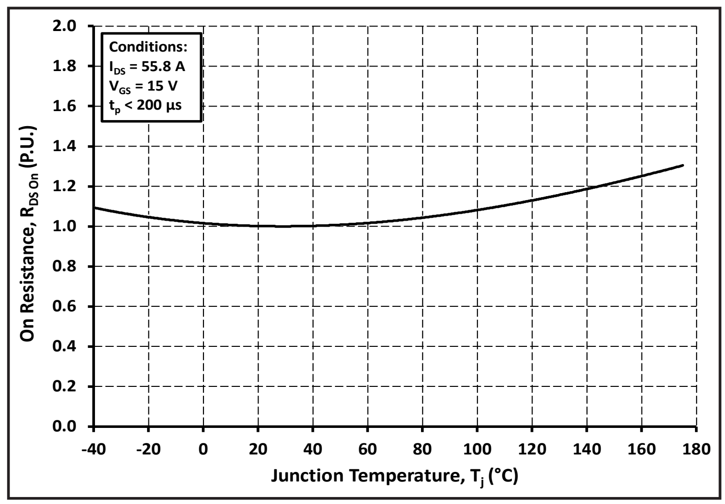

Figure 4. Normalized On-Resistance vs. Temperature

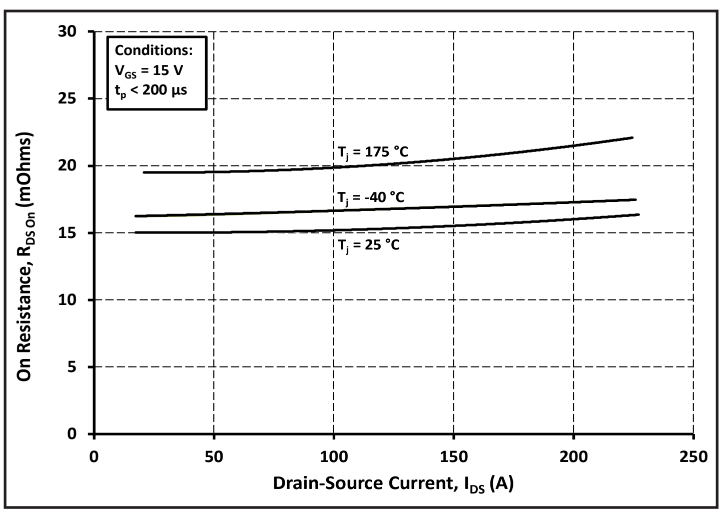

Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

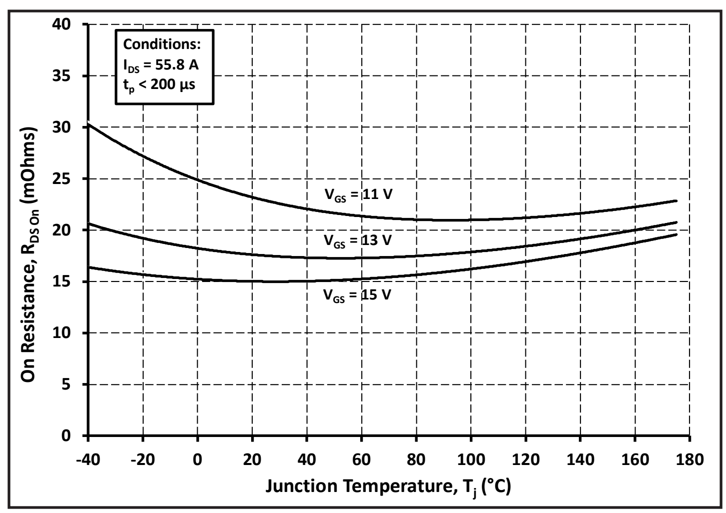

Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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Typical Performance

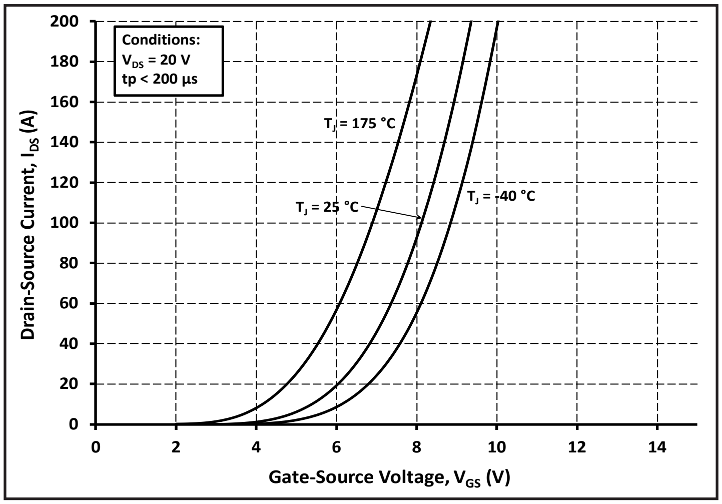

Figure 7. Transfer Characteristic for Various Junction Temperatures

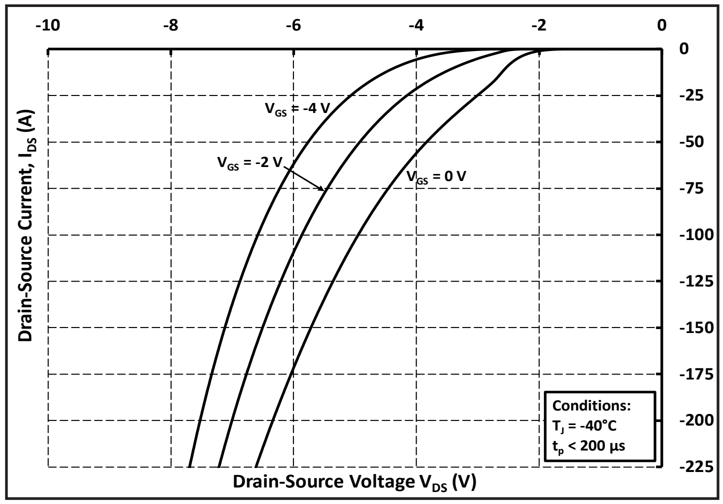

Figure 8. Body Diode Characteristic at -40 °C

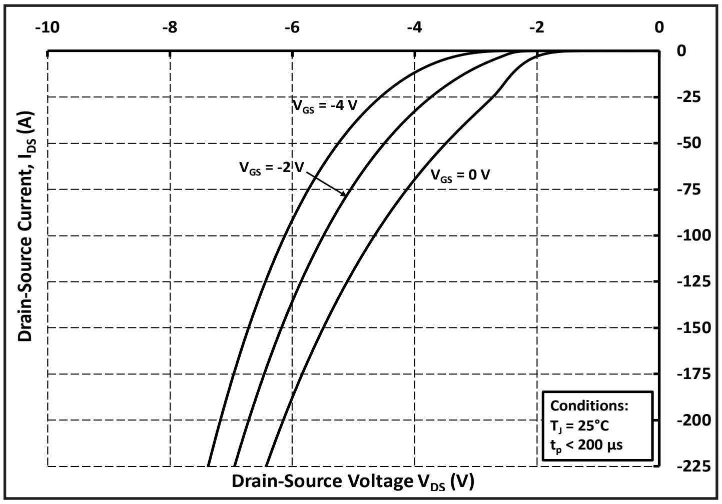

Figure 9. Body Diode Characteristic at 25 °C

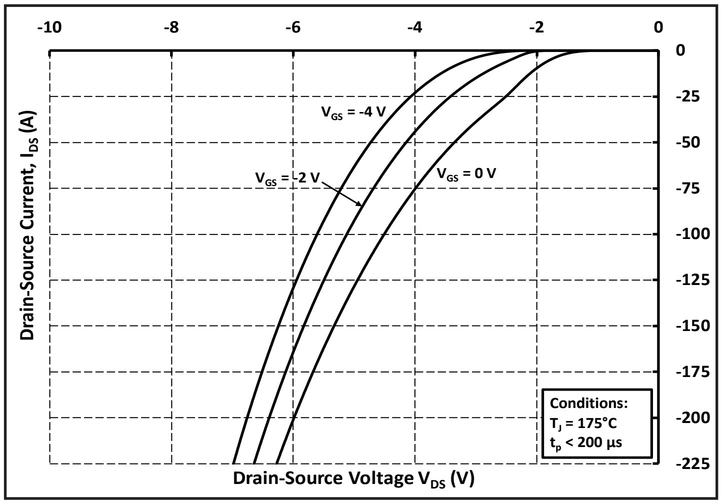

Figure 10. Body Diode Characteristic at 175 °C

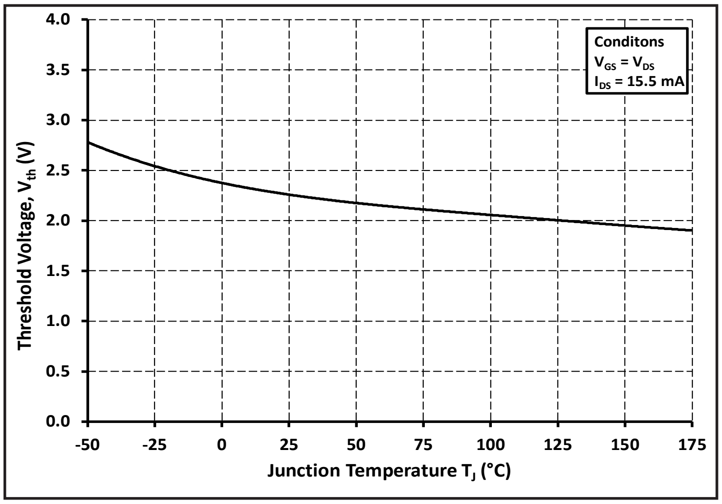

Figure 11. Threshold Voltage vs. Temperature

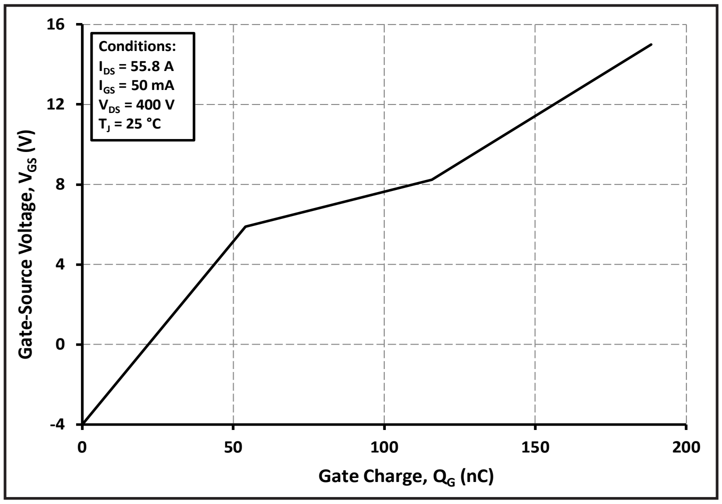

Figure 12. Gate Charge Characteristics

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Typical Performance

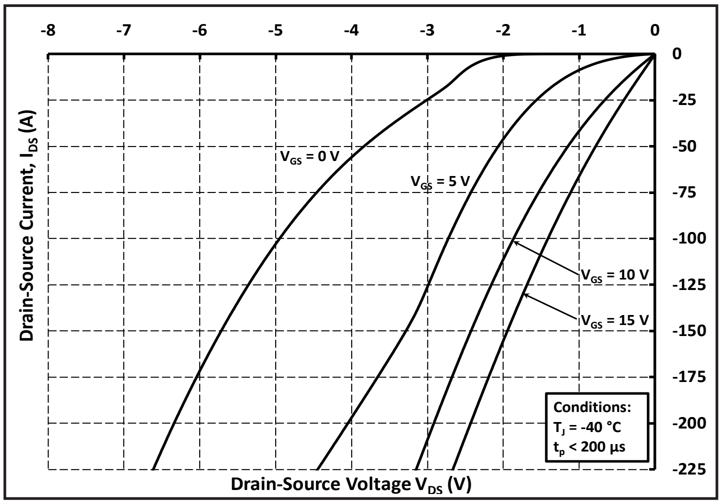

Figure 13. 3rd Quadrant Characteristic at -40 °C

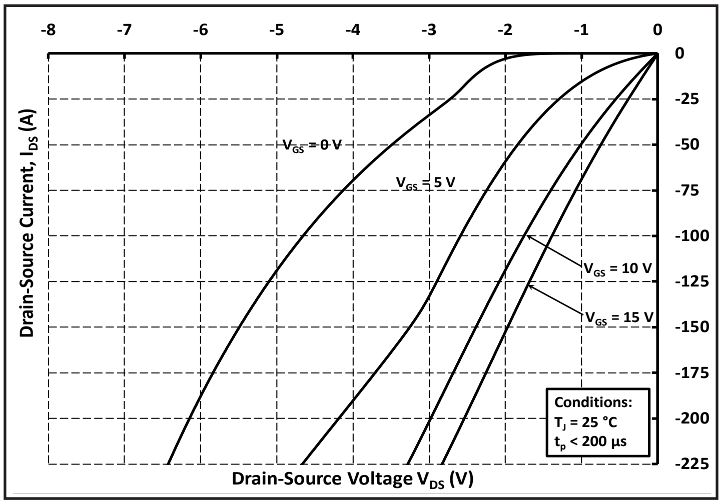

Figure 14. 3rd Quadrant Characteristic at 25 °C

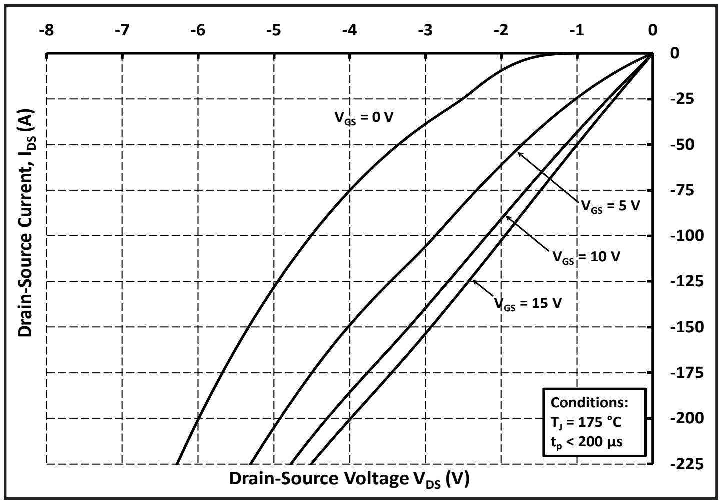

Figure 15. 3rd Quadrant Characteristic at 175 °C

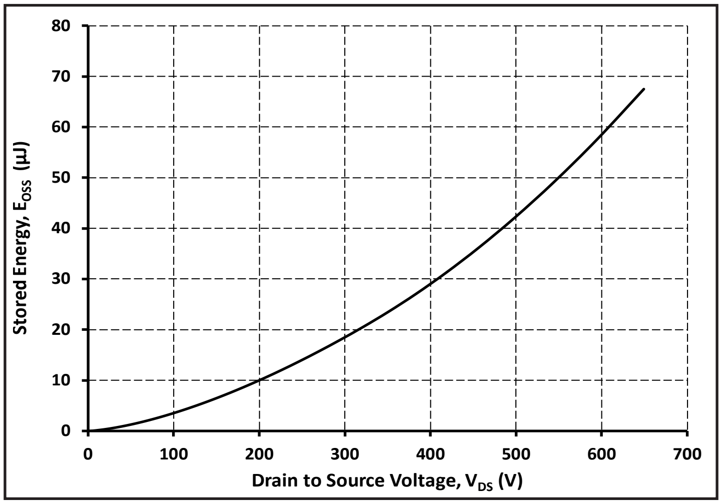

Figure 16. Output Capacitor Stored Energy

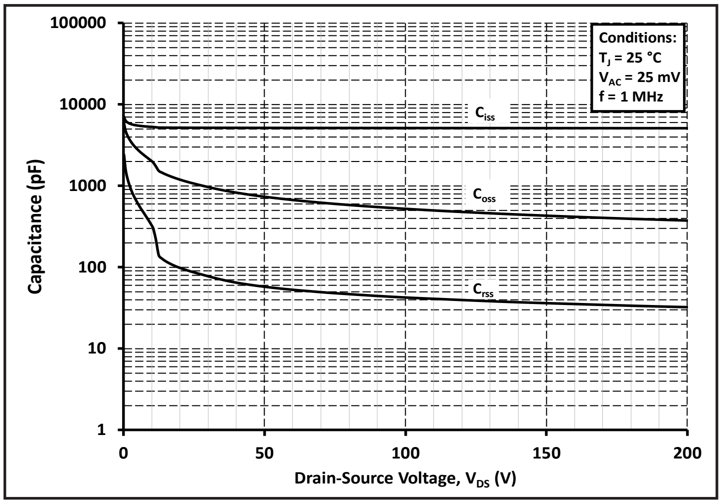

Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

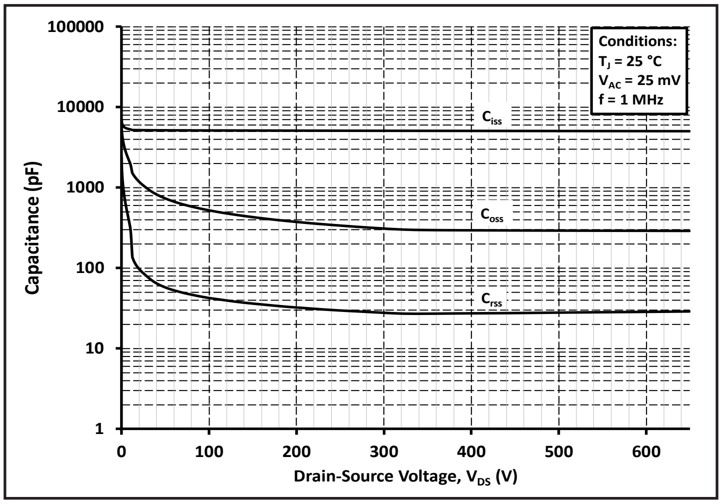

Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

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Typical Performance

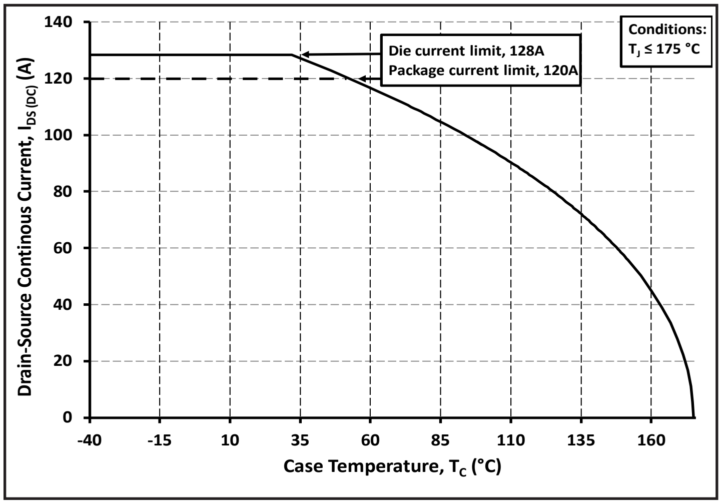

Figure 19. Continuous Drain Current Derating vs. Case Temperature

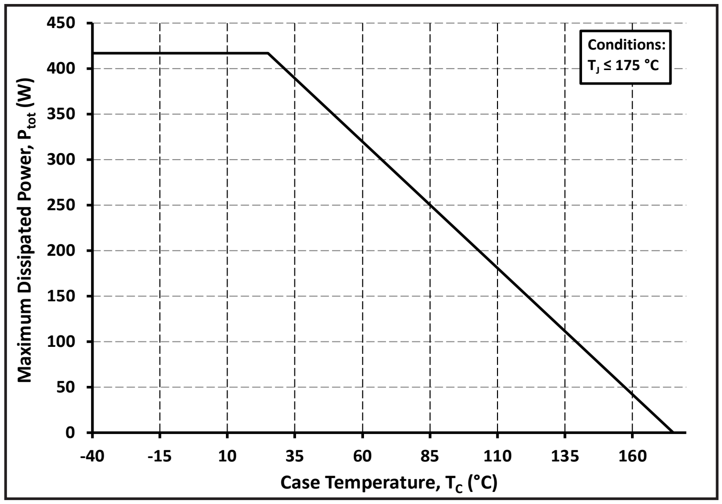

Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

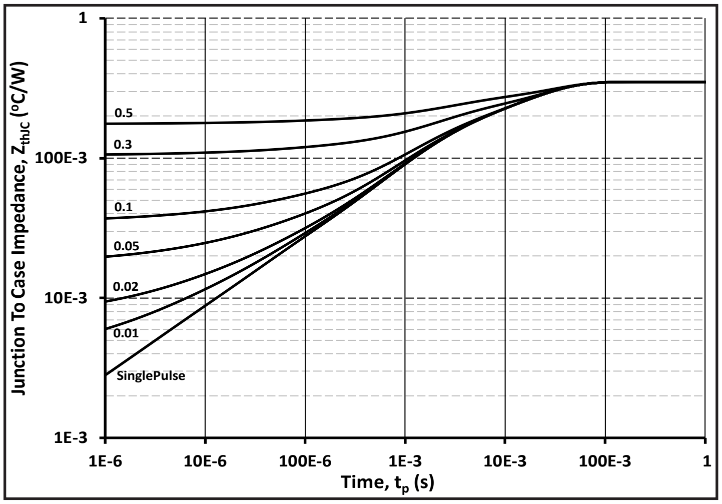

Figure 21. Transient Thermal Impedance (Junction - Case)

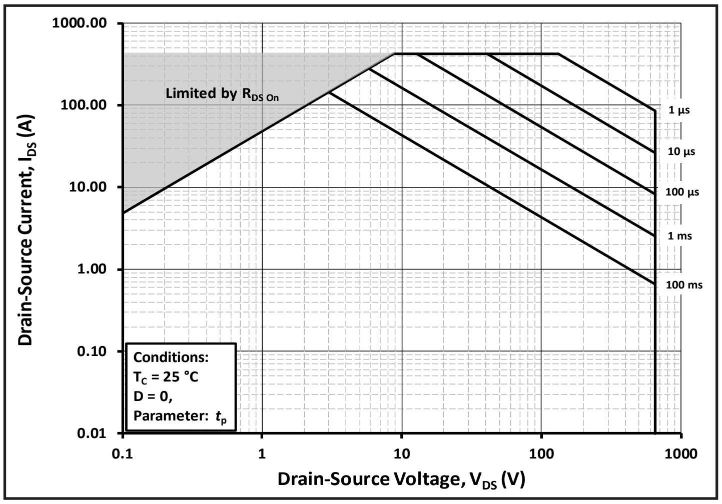

Figure 22. Safe Operating Area

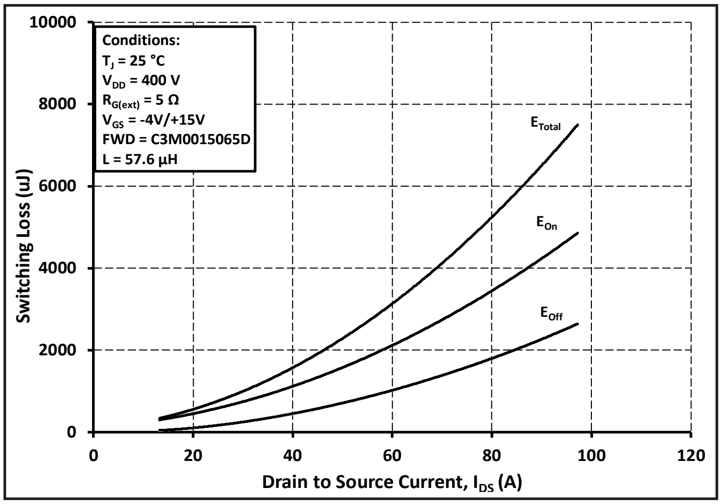

Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

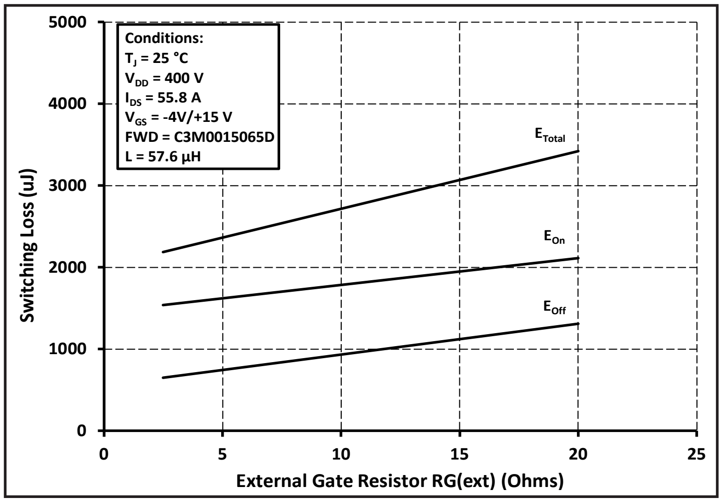

Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

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Typical Performance

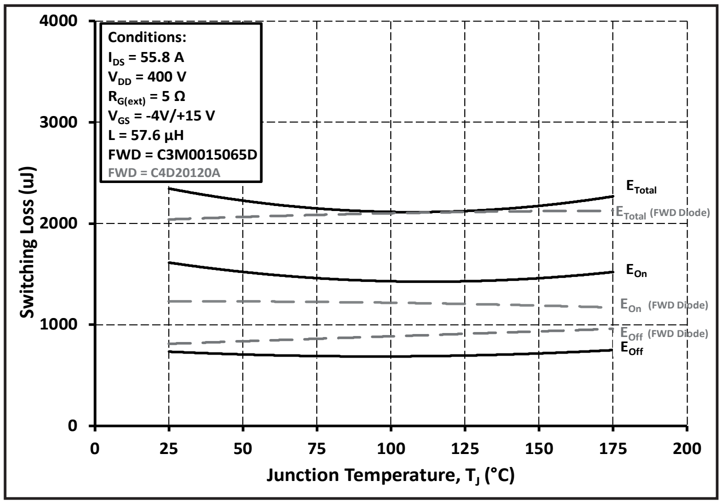

Figure 25. Clamped Inductive Switching Energy vs. Temperature

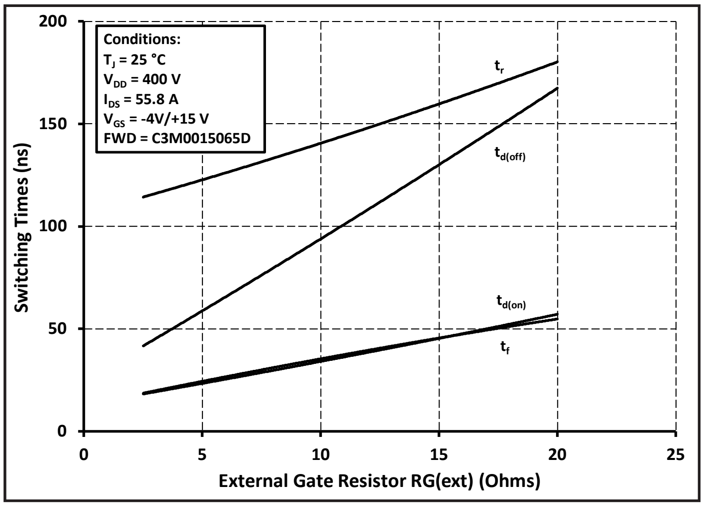

Figure 26. Switching Times vs. $R_{G(ext)}$

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Test Circuit Schematic

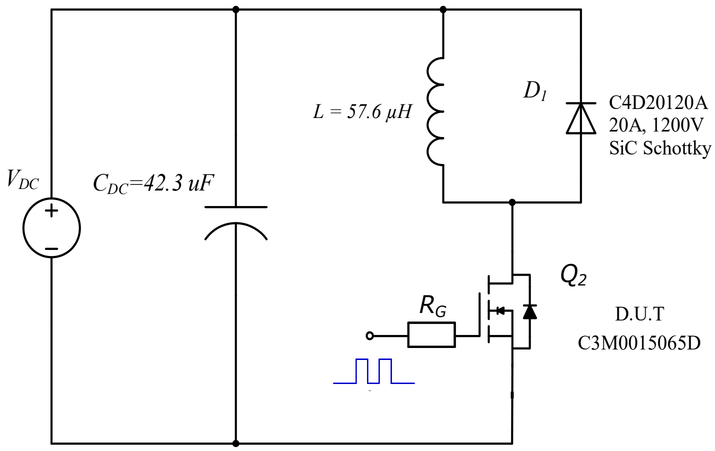

Figure 27. Clamped Inductive Switching Waveform Test Circuit

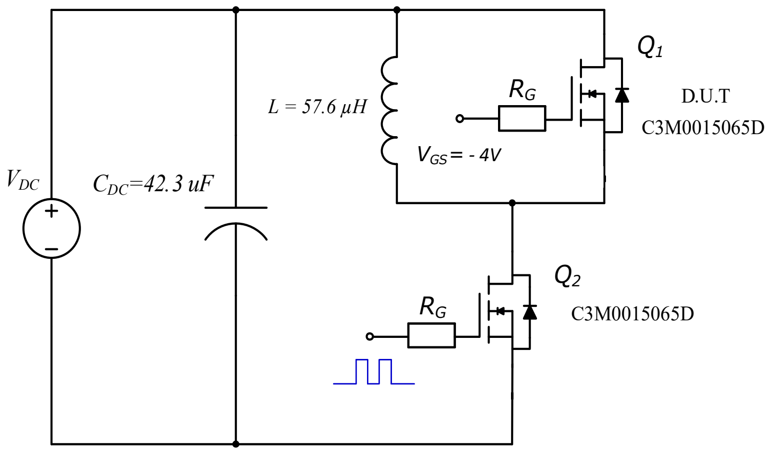

Figure 28. Body Diode Recovery Test Circuit

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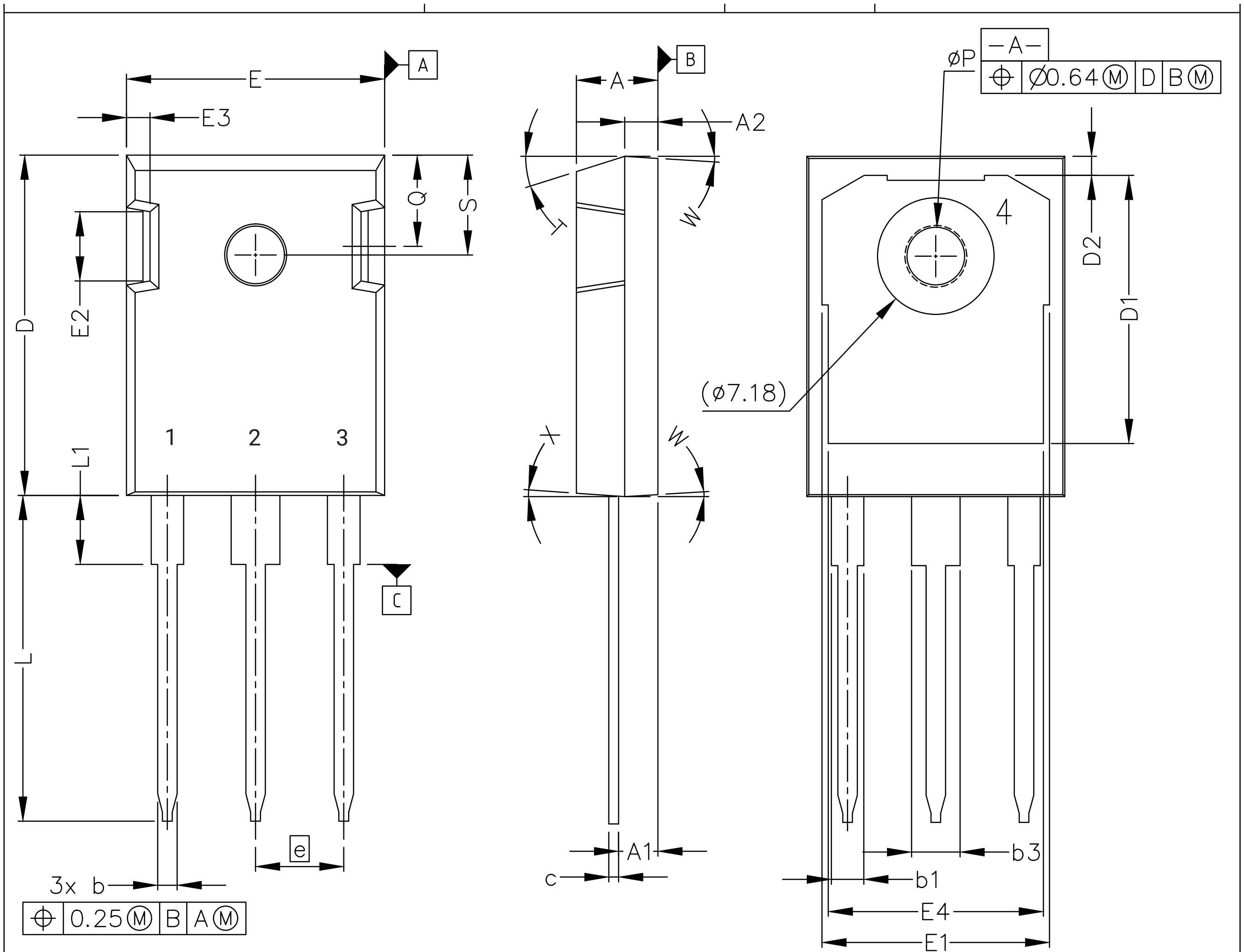
Package Dimensions

Package TO-247-3



NOTE ;
1. ALL METAL SURFACES: TIN PLATED,EXCEPT AREA OF CUT
2. DIMENSIONING & TOLERANCEING CONFIRM TO
   ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
   ANGLES ARE IN DEGREES.
4. THIS DRAWING WILL MEET ALL DIMENSIONS REQUIREMENT
   OF JEDEC outlines TO-247 AD.
5. DIMENSION DO NOT INCLUDE BURR OR MOLD FLASH.

1 - GATE
2 - DRAIN (COLLECTOR)
3 - SOURCE (EMITTER)
4 - DRAIN (COLLECTOR)

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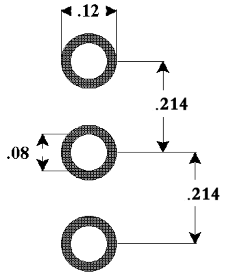
Package Dimensions

Package TO-247-3

SYM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	.190	.205
A1	2.29	2.54	.090	.100
A2	1.91	2.16	.075	.085
b	1.07	1.33	.042	.052
b1	1.91	2.41	.075	.095
b3	2.87	3.38	.113	.133
c	0.55	0.68	.022	.027
D	20.80	21.10	.819	.831
D1	16.25	17.65	.640	.695
D2	0.95	1.25	.037	.049
E	15.75	16.13	.620	.635
E1	13.10	14.15	.516	.557
E2	3.68	5.10	.145	.201
E3	1.00	1.90	.039	.075
E4	12.38	13.43	.487	.529
e	5.44 BSC		.214 BSC	
N	3		3	
L	19.81	20.32	.780	.800
L1	4.10	4.40	.161	.173
ØP	3.51	3.65	.138	.144
Q	5.49	6.00	.216	.236
S	6.04	6.30	.238	.248
T	17.5° REF.			
W	3.5° REF.			
X	4° REF.			

Recommended Solder Pad Layout



TO-247-3

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REACh Compliance
REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Cree representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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