uPOL MODULE

1000mA, High Efficiency uPOL Module

MUN12AD01-SG

FEATURES:

- High Density Fully Integration Module
- 1000mA Output Current
- Input Voltage Range from 4.5V to 16.0V
- Output Voltage Range from 0.8V to 6.0V
- 94% Peak Efficiency at 5 Vin to 3.3 Vout
- Force PWM mode
- Enable Function
- Protections (UVLO, OCP: Non-latching)
- Internal Soft Start
- Compact Size: 3.9mm*2.6mm*1.7mm
- Pb-free for RoHS compliant
- MSL 2, 260°C Reflow

APPLICATIONS:

- DSL Modem / LCD TV
- Portable TV / Access Point Router

GENERAL DESCRIPTION:

The MUN12AD01-SG is non-isolated dc-dc converters. The PWM switching regulator, high frequency power inductor, and most of support components are integrated in one hybrid package.

Other features include remote enable function, internal soft-start, non-latching over current protection, and input under voltage locked-out capability.

The low profile and compact size package (3.9mm × 2.6mm x 1.7mm) is suitable for automated assembly by standard surface mount equipment. The MUN12AD01-SG is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

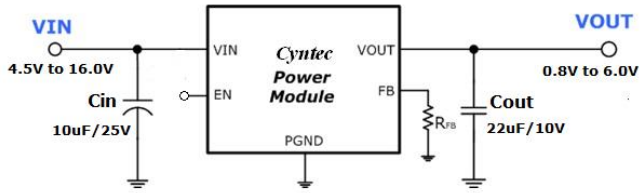


FIG.1 TYPICAL APPLICATION CIRCUIT

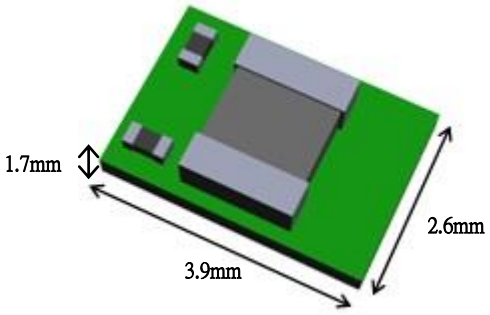


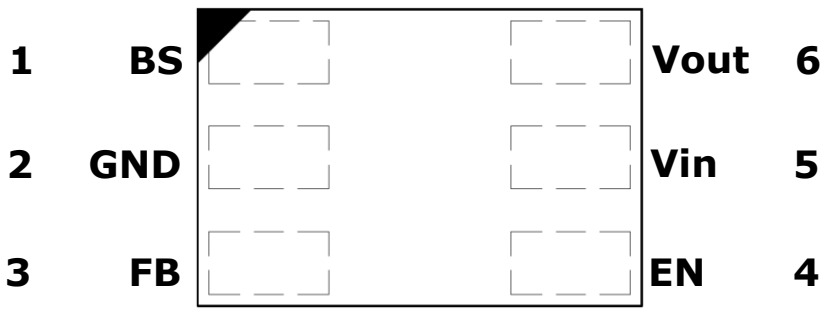
FIG.2 HIGH DENSITY uPOL MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN12AD01-SG	-40 ~ +85	DFN	Level 2	-

Order Code	Packing	Quantity
MUN12AD01-SG	Tape and reel	1000

PIN CONFIGURATION:



TOP VIEW

Symbol	Pin No.	Description
BS	1	Boot-Strap Pin. No need connection.
GND	2	Power ground pin for signal, input, and output return path. This pin needs to be connected to one or more ground planes directly.
FB	3	Feedback input. Connect to output through a voltage dividing resistor between this pin to GND for adjusting output voltage. Place this resistor as closely as possible to this pin.
EN	4	On/Off control pin for module.
VIN	5	Input pin. Decouple this pin to GND pin with 10uF ceramic cap
VOUT	6	Power output pin. Connect to output for the load.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-	-	18	V
EN to GND	Note 1	-	-	VIN+0.3	V
Tc	Case Temperature of Inductor	-40	-	+110	°C
Tj	Junction Temperature (Main IC)	-40	-	+125	°C
Tstg	Storage Temperature	-40	-	+125	°C
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+16	V
VOUT	Adjuested Output Voltage	+0.8	-	+6.0	V
Ta	Ambient Tamperture	-40	-	+85	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient. (Note 1)	-	50	-	°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers 2oz. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 12V, Vout = 3.3V, Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Switching Frequency			-	1.2	-	MHz
■ Input Characteristics						
I_{IN}	Input supply bias current	Vin = 12V, Iout = 0A EN = With pull-up 100kΩ to VIN Vout = 3.3V	-	14	-	mA
I_S	Input supply current	Iout = 5mA Vout = 3.3V	-	14.3	-	mA
		Iout = 100mA Vout = 3.3V	-	41.7	-	mA
		Iout = 1000mA Vout = 3.3V	-	319	-	mA
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Vin=12V, Vout=3.3V	0	-	1000	mA
$V_{O(SET)}$	Ouput voltage set point	With 1% tolerance for external resistor used to set output voltage	-3.0	-	+3.0	% $V_{O(SET)}$
ΔV_{OUT} / ΔV_{IN}	Line regulation accuracy	Vin = 12V to 5.0V Vout = 3.3V, Iout = 1000mA	-	0.2	-	% $V_{O(SET)}$
ΔV_{OUT} / ΔI_{OUT}	Load regulation accuracy	Iout = 0A to 1000mA Vin = 12 V, Vout = 3.3V	-	0.5	-	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 12V, Vout = 1.2V IOUT = 1000mA	-	8	-	mVp-p
		Vin = 12V, Vout = 5.0V IOUT = 1000mA	-	11	-	mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	Iout = 0.5A to 1.0A Current slew rate = 0.06A/uS Vin = 12V, Vout = 3.3V	-	35	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	Iout = 1.0A to 0.5A Current slew rate = 0.06A/uS Vin = 12V, Vout = 3.3V	-	35	-	mVp-p

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 12V, Vout = 3.3V, Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
V_{EN_TH}	Enable threshold voltage		1.5	-	-	V
	Disable threshold voltage		-	-	0.4	V
■ Fault Protection						
V_{UVLO_TH}	Input under voltage lockout threshold	Falling	-	-	4.5	V
T_{OTP}	Over temp protection		-	150	-	°C
I_{LIMIT_TH}	Current limit threshold	Peak value of inductor current	1.8	-	3.0	A

TYPICAL PERFORMANCE CHARACTERISTICS: (1.2 VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 1.2Vout.

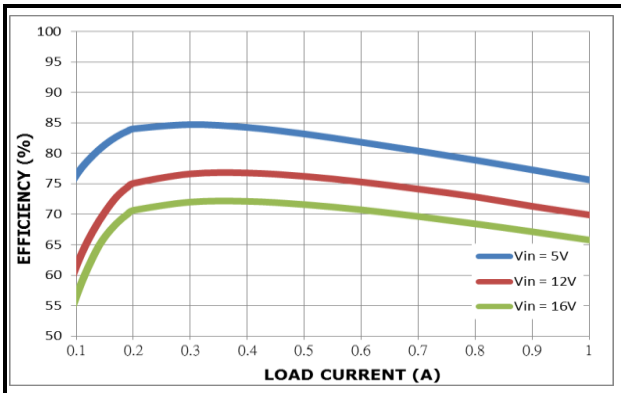


FIG.3 EFFICIENCY V.S. LOAD CURRENT

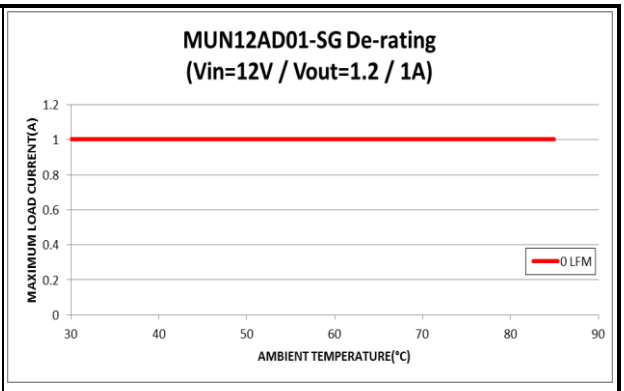


FIG.4 DE-RATING CURVE AT 12V VIN

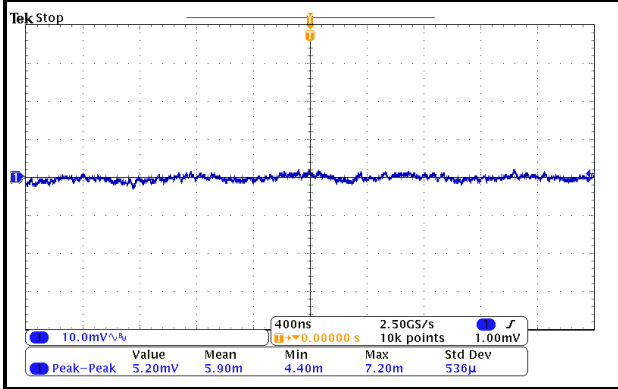


FIG.5 OUTPUT RIPPLE
(12V VIN, IOUT=0 A)

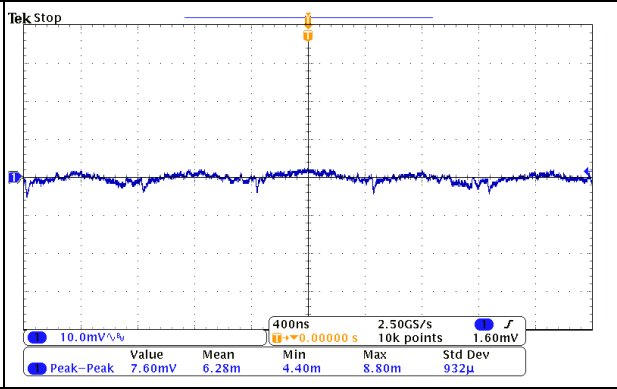


FIG.6 OUTPUT RIPPLE
(12V VIN, IOUT=1 A)

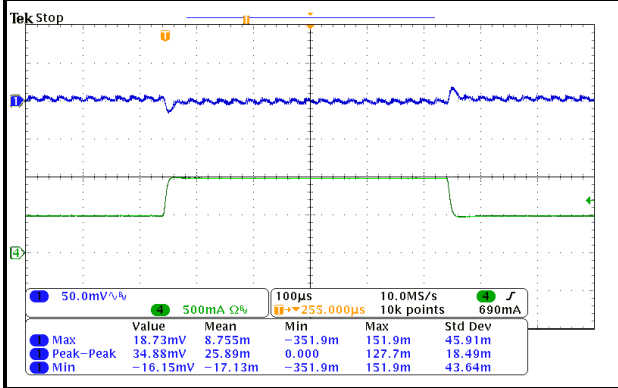


FIG.7 TRANSIENT RESPONSE
(12V VIN, 50% to 100% LOAD STEP)

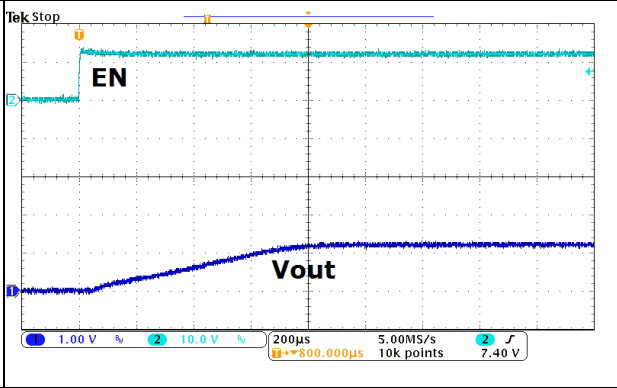


FIG.8 TURN-ON
(12V VIN, IOUT=1 A)

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8 VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 1.8Vout.

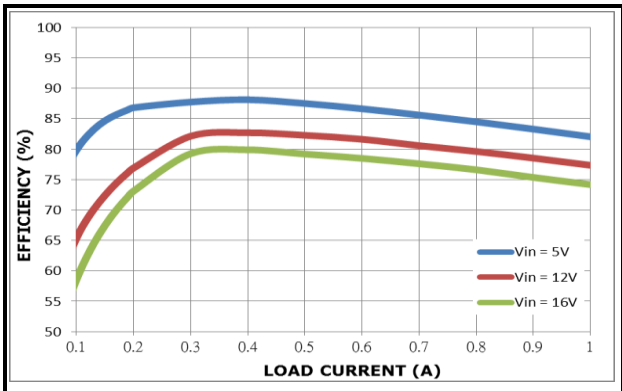


FIG.9 EFFICIENCY V.S. LOAD CURRENT

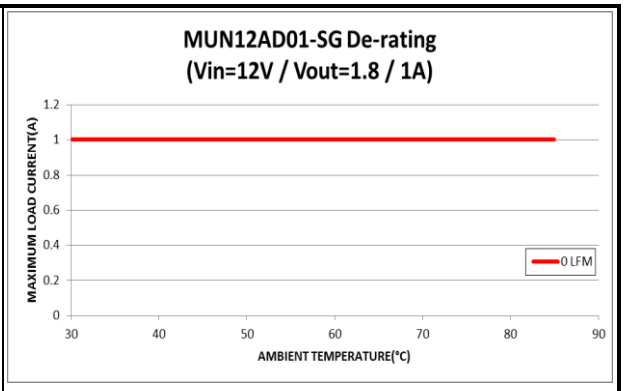


FIG.10 DE-RATING CURVE AT 12V VIN

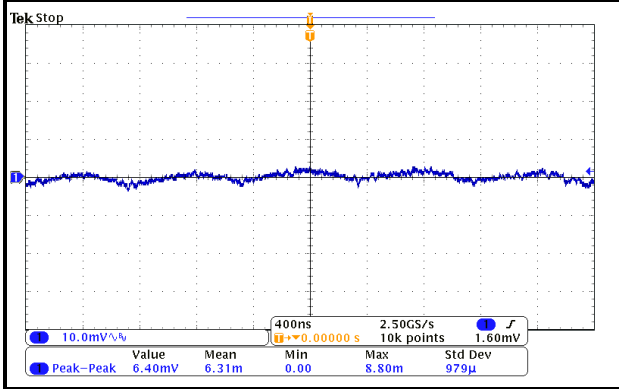


FIG.11 OUTPUT RIPPLE
(12V VIN, IOUT=0 A)

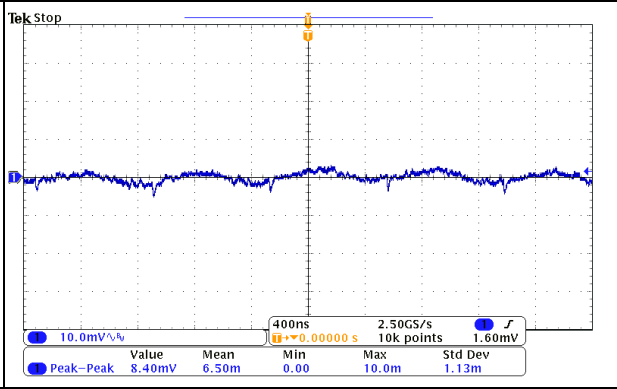


FIG.12 OUTPUT RIPPLE
(12V VIN, IOUT=1 A)

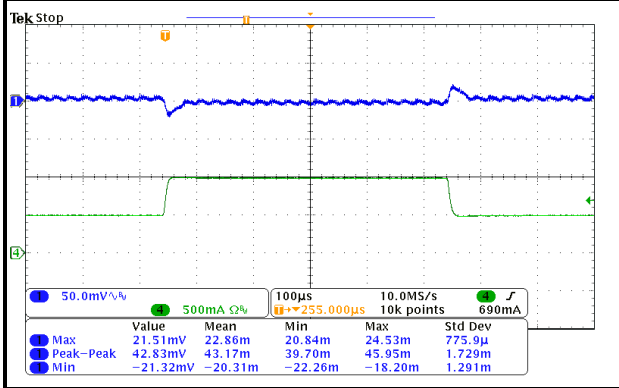


FIG.13 TRANSIENT RESPONSE
(12V VIN, 50% to 100% LOAD STEP)

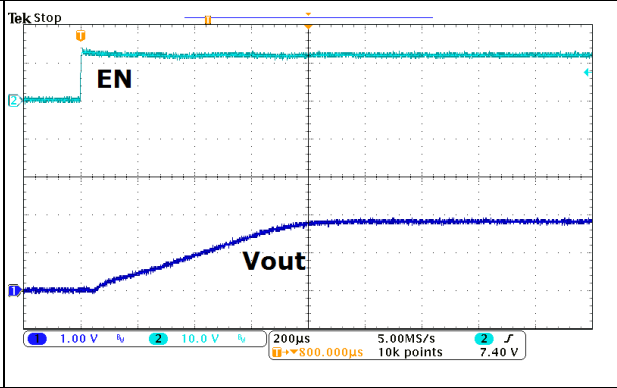


FIG.14 TURN-ON
(12V VIN, IOUT=1 A)

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3 VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 3.3Vout.

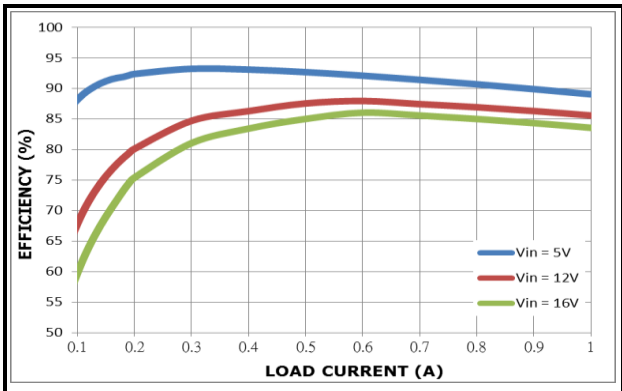


FIG.15 EFFICIENCY V.S. LOAD CURRENT

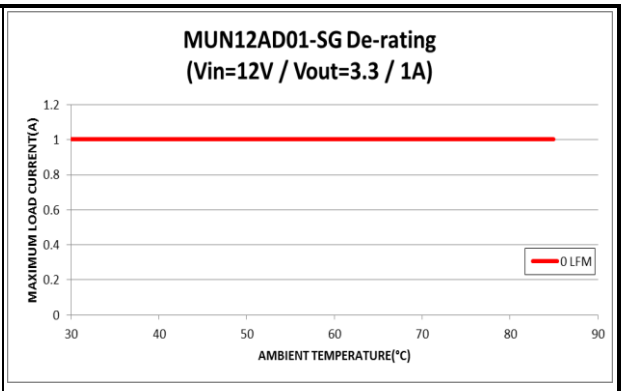


FIG.16 DE-RATING CURVE AT 12V VIN

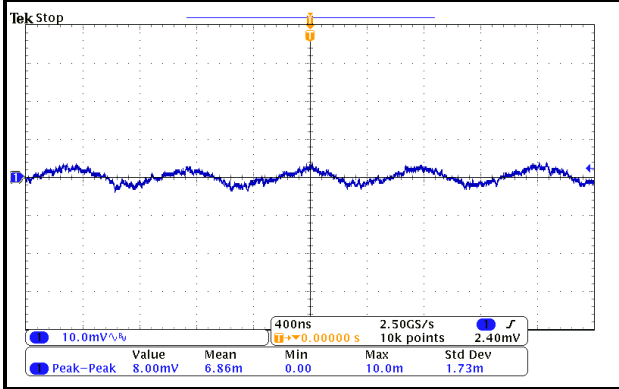


FIG.17 OUTPUT RIPPLE
(12V VIN, IOUT=0 A)

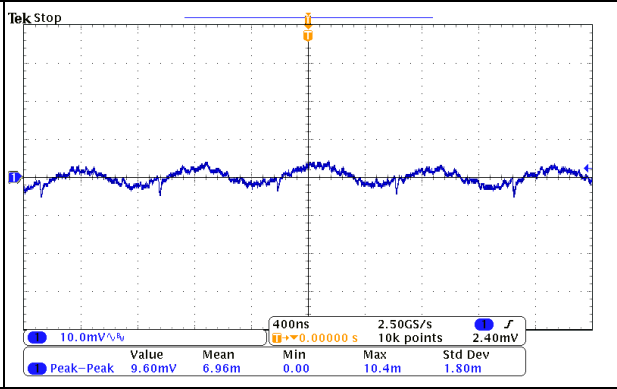


FIG.18 OUTPUT RIPPLE
(12V VIN, IOUT=1 A)

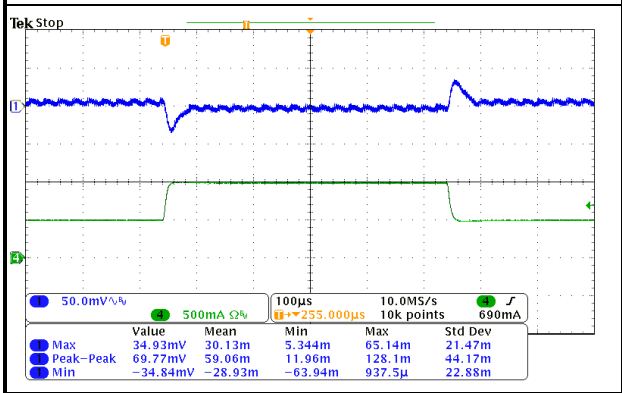


FIG.19 TRANSIENT RESPONSE
(12V VIN, 0% to 100% LOAD STEP)

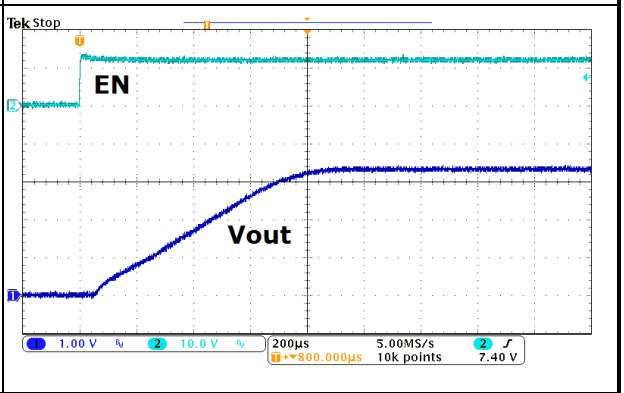


FIG.20 TURN-ON
(12V VIN, IOUT=1 A)

TYPICAL PERFORMANCE CHARACTERISTICS: (5.0 VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Cin =10uF/50V/1210/X7R, Cout = 22uF/16V/1210/X7R.
The following figures provide the typical characteristic curves at 5.0Vout.

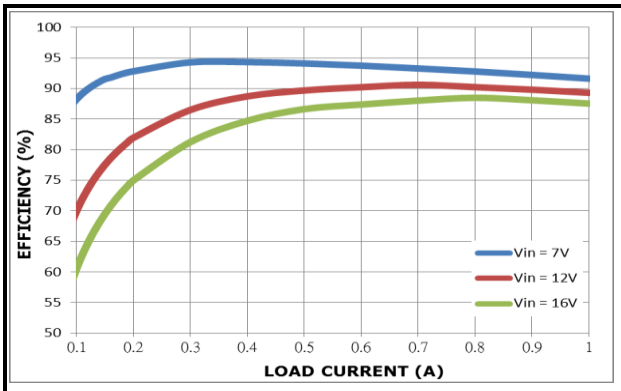


FIG.21 EFFICIENCY V.S. LOAD CURRENT

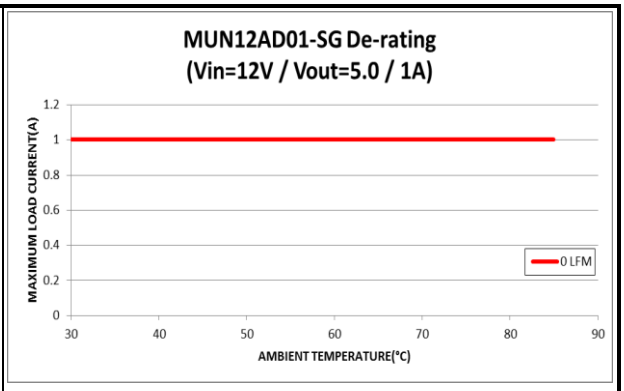


FIG.22 DE-RATING CURVE AT 12V VIN

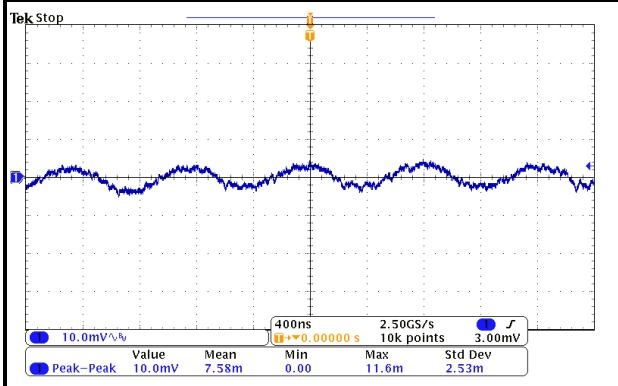


FIG.23 OUTPUT RIPPLE
(12V VIN, IOUT=0 A)

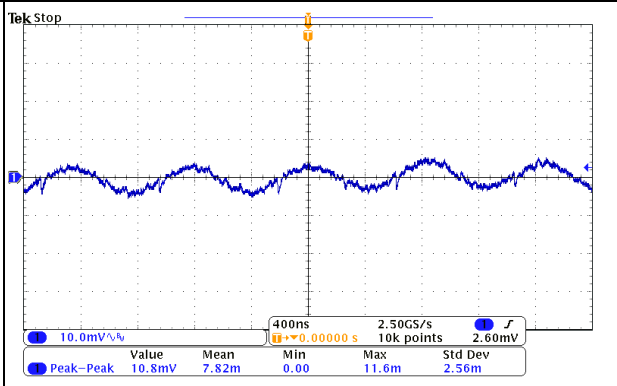


FIG.24 OUTPUT RIPPLE
(12V VIN, IOUT=1 A)

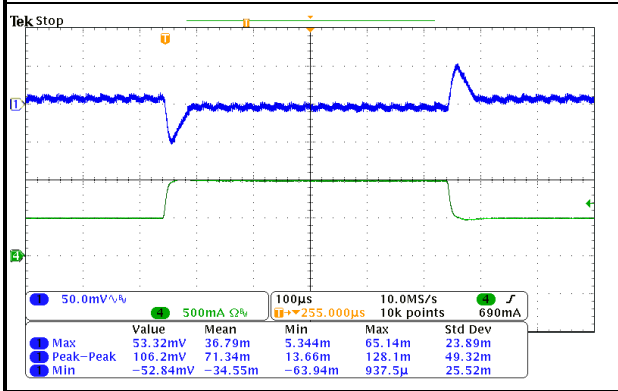


FIG.25 TRANSIENT RESPONSE
(12V VIN, 50% to 100% LOAD STEP)

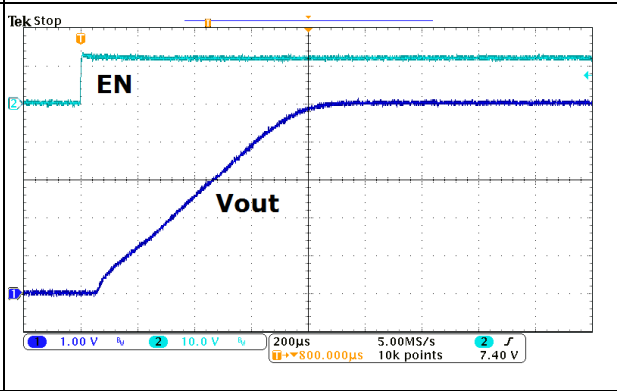


FIG.26 TURN-ON
(12V VIN, IOUT=1 A)

APPLICATIONS INFORMATION: (Cont.)

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected source with low AC impedance source supply and a highly inductive in which line inductance can affect the stability of the module. An input capacitance must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response as step load changes, the additional capacitor at the output must be used. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±2% reference voltage. The output voltage can be programed by the dividing resistance RFB which respects to FB pin and GND pin. The output voltage can be calculated as shown in Equation 1.(R1 is integrated in Module :100KΩ+/-1%)

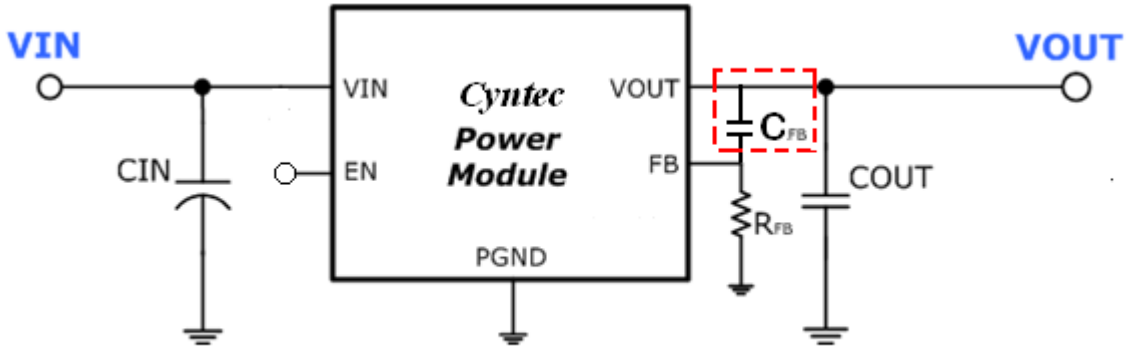
$$Vout=0.6*(1+R1/R_{FB})$$

Vout (V)	1	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB}	150KΩ	100KΩ	66.67KΩ	50KΩ	31.58KΩ	22.22KΩ	13.64KΩ

APPLICATIONS INFORMATION: (Cont.)

LOAD TRANSIENT CONSIDERATIONS:

The MUN12AD01-SG integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 100pF ceramic cap between Vout and FB may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 27 shows the module application schematics for input voltage +12V and turn on by input voltage directly through enable resistor (R1).

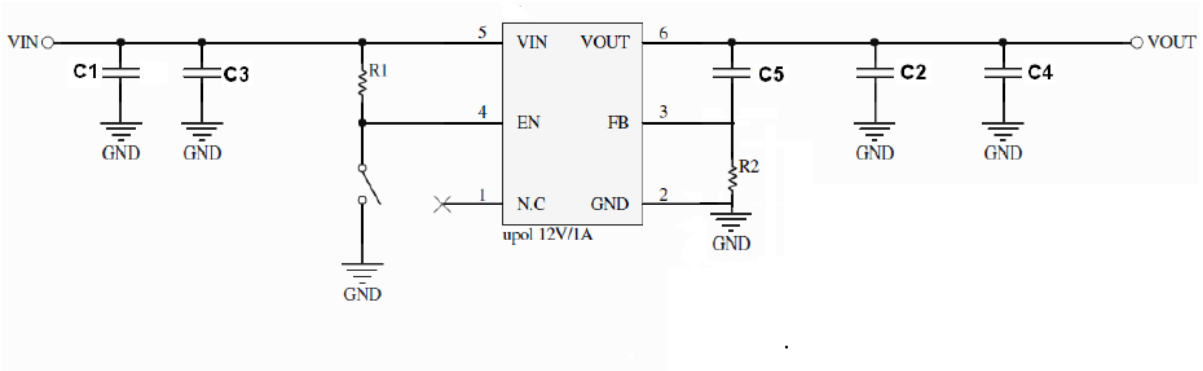


FIG.27 REFERENCE CIRCUIT FOR GENERAL APPLICATION

APPLICATIONS INFORMATION: (Cont.)

RECOMMEND PCB LAYOUT:

Figure 28 shows recommendation PCB layout for using uPOL module,

- C3/C4 are bypass filter for high frequency noise.
- Design paths of main current wide and short as Make the traces of the main current paths as short and wide as possible.
- Place the input/out capacitor as close as possible to the uPOL module pins.
- Ensure all feedback network connections are short, direct and don't close BS pin.
- C5 and R2 must be placed as close as possible to the FB pin.
- The GND pin and should be connected to a strong ground plane for heat dissipating.

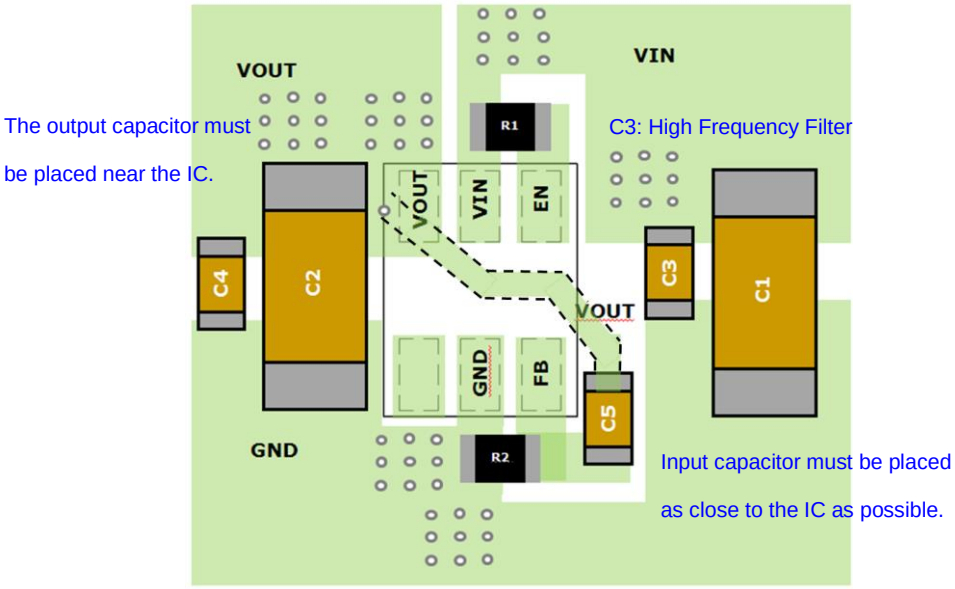


FIG.28 PCB LAYOUT

APPLICATIONS INFORMATION: (Cont.)

Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 29. Then Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The MUN12AD01-SG module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

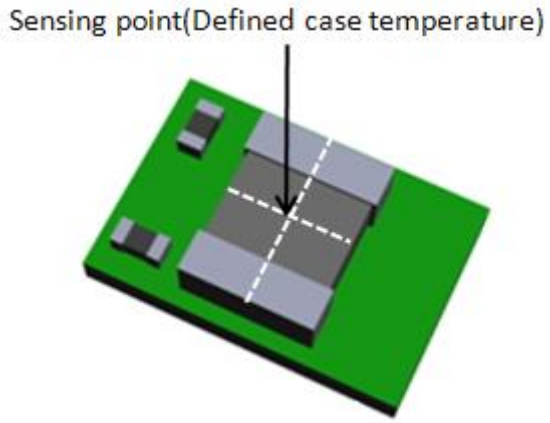


FIG 29. Case Temperature Sensing Point

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 30 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

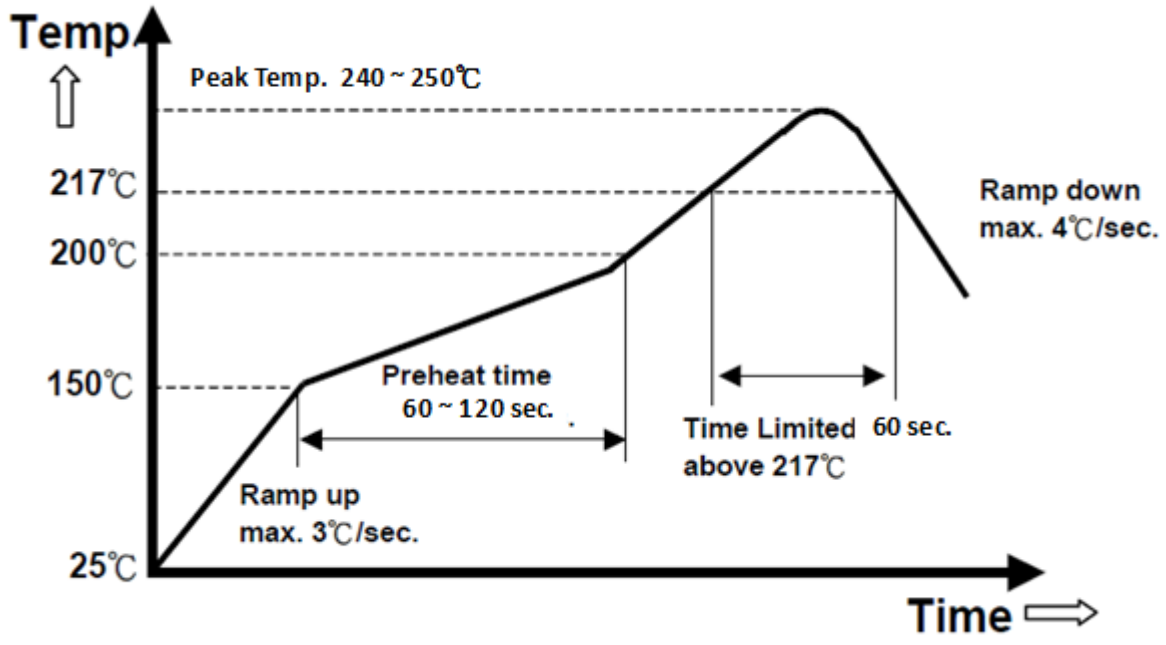
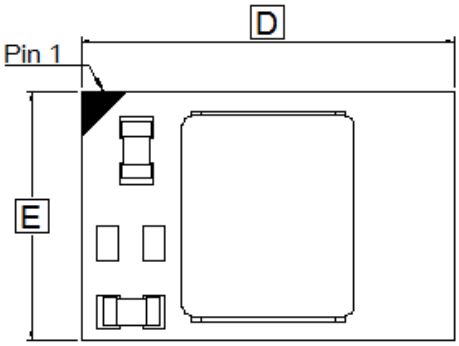


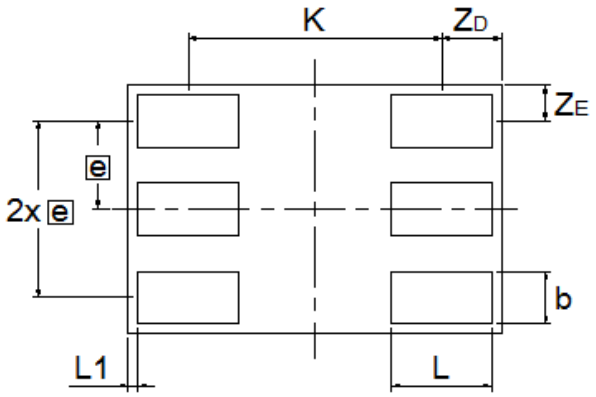
FIG.30 Recommendation Reflow Profile

PACKAGE OUTLINE DRAW:

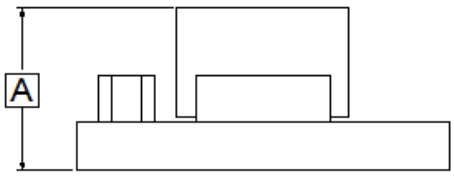
Unit:mm



Top View



Bottom View

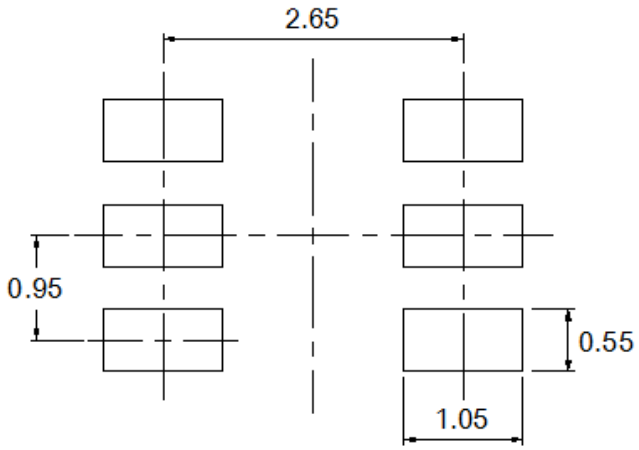


End View

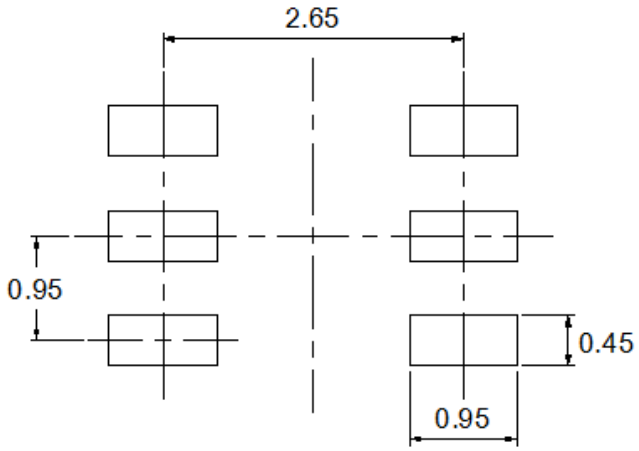
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.40	1.55	1.70
D	3.8	3.9	4.0
E	2.5	2.6	2.7
K	2.55	2.65	2.75
e	0.85	0.95	1.05
b	0.45	0.55	0.65
L	0.95	1.05	1.15
L1	0.00	0.10	0.20
ZD	0.50	0.65	0.80
ZE	0.25	0.40	0.55

LAND PATTERN REFERENCE:

Unit:mm



RECOMMENDED LAND PATTERN

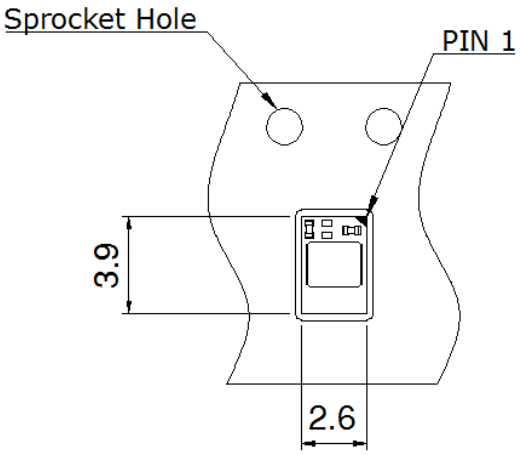


RECOMMENDED STENCIL PATTERN
BASED ON 0.1mm THICKNESS STENCIL

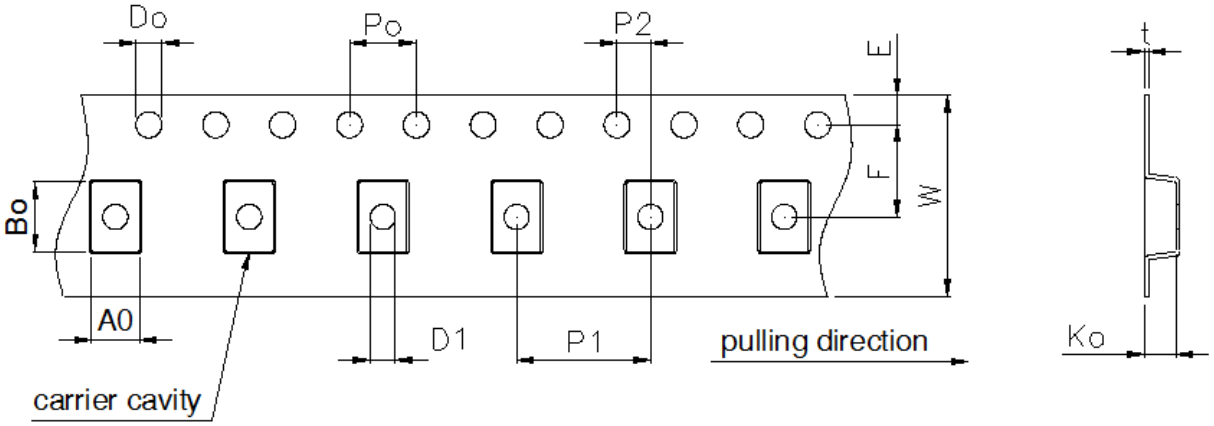
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

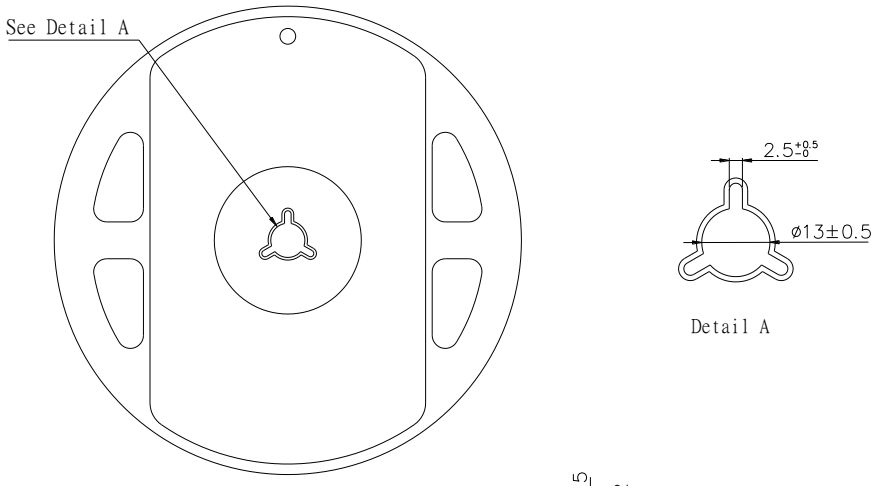


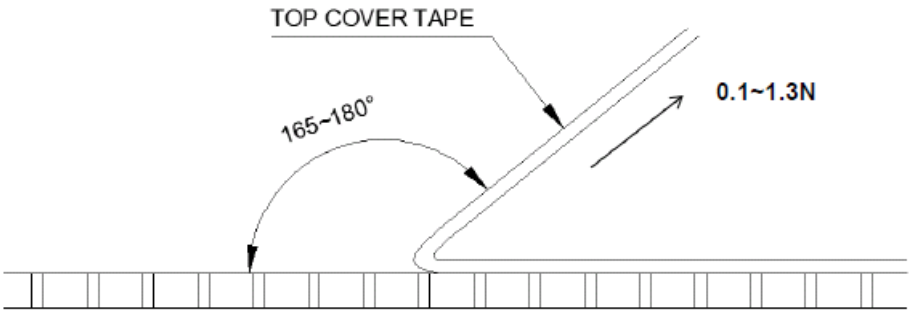
A0	2.9± 0.10	E	1.75 ± 0.10
B0	4.2 ± 0.10	K0	1.88 ± 0.10
F	5.50 ± 0.05	P0	4.00 ± 0.10
W	12.00 ±0.30	P1	8.00 ± 0.10
D0	φ1.55 ±0.05	P2	2.00 ± 0.05
D1	φ1.50± 0.10	t	0.25 ± 0.10

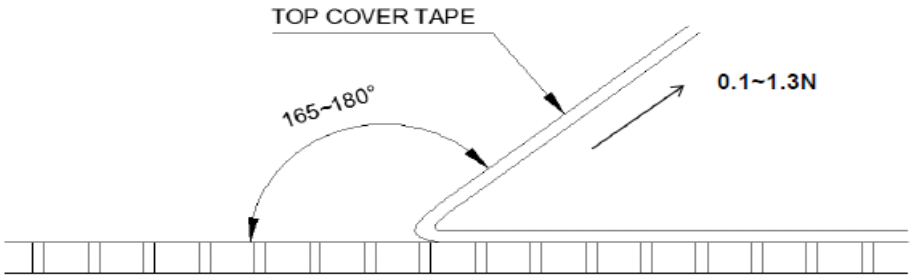
PACKING REFERENCE: (Cont.)

Unit: mm

Reel Dimension







REVISION HISTORY:

Date	Revision	Changes
2014.08.01	00	Preliminary Spec. issued initially.
2014.08.07	01	Change Vout range.
2014.10.23	02	Change figure of module; Add Load Transient Consideration.
2015.01.07	03	Add package information.
2015.06.29	04	Add reflow parameters. Add reference circuit for general application.
2015.10.05	05	Add Temperature Information of page 2
2015.11.23	06	Update page 14 reflow parameters
2016.03.28	07	Change input voltage range from 18V to 16V and output voltage range from 6V to 5V
2016.09.29	08	1. Change output voltage form 5V to 6V 2. Add Page 2 order information 3. Change Page 4~9 test condition and update test figures 4. Page 12 add matter needing attention for feedback network
2016.12.29	09	1. Correcting Page 2 package name from QFN to DFN