uPOL MODULE

2A, High Efficiency uPOL Module

MUN3CAD02-JE

FEATURES:

- High Density uPOL Module
- 2A Output Current
- Input Voltage Range from 2.7V to 5.5V
- Adjustable Output Voltage
- Enable / Power Good Function
- Forced PWM Mode
- Protections (input UVLO, OCP: Non-latching, OTP, OVP)
- Internal Soft Start 2.1mS
- Compact Size: 3.5mm*2.5mm*1.5mm
- Pb-free for RoHS compliant
- 100% dropout voltage
- MSL 2, 260°C Reflow

APPLICATIONS:

- 100G/400G/800G Optical module
- Server power / telecom power
- SSD

GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 2A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and voltage dividing resistors.

The module was forced PWM mode, through constant on-time control. The module offers a simpler control loop and faster transient response. Other features include remote enable function, internal soft-start, non-latching over current protection, power good, and input under voltage locked-out capability.

The low profile and compact size package is suitable for automated assembly by standard surface mount equipment.

TYPICAL APPLICATION CIRCUIT& PACKAGE:

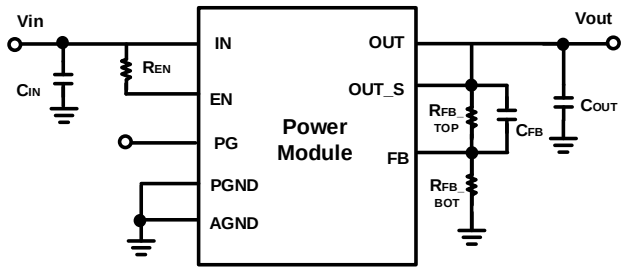


FIG.1 TYPICAL APPLICATION CIRCUIT

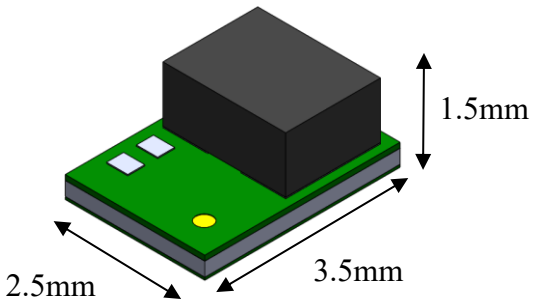


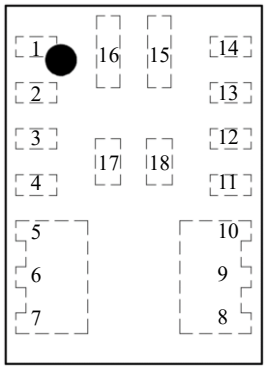
FIG.2 HIGH DENSITY uPOL MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN3CAD02-JE	-40 ~ +105	QFN	Level 2	-

Order Code	Packing	Quantity
MUN3CAD02-JE	Tape and reel	2000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
AGND	1	Analog ground. The internal controller ground
FB	2	Feedback input. Connect an external resistor divider from the output to FB and FB to GND.
OUT_S	3	Output Voltage Sense Pin.
EN	4	Enable control. Do not be float.
SW	5~7、15	Switch node. Leave it no connection.
OUT	8~10	Power output pin.
NC	11	No connection. Float NC or connect NC to GND
PG	12	Power Good indicator. Power Good indicator. With internal 500kΩ pull-up resistor to VIN.
IN	13~14	Power input pin.
PGND	16	Power ground.
NC	17~18	No connection. Leave NC floating.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impacted product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-0.3	-	+6.0	V
VOUT to GND		-	-	+6.0	V
SW to GND		-0.3	-	VIN+0.3	V
The other pin to GND		-0.3	-	+6.0	V
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Machine Model (MM)	-	-	200	V
	Charge Device Model (CDM)	-	-	1000	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+2.7	-	+5.5	V
VOUT	Output Setting Voltage	+0.6	-	+3.3	V
Ta	Ambient Temperature	-40	-	+105	°C
Tj	Junction Temperature	-40	-	+135	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient, Ta = 25℃ (Note 1)	-	50.3	-	°C/W

NOTES:
1. Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers, 2 oz per layer. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 3.3V, Vout = 1.8V, Cin =22uF/6.3V/0805/X7R, Cout = 22uF/6.3V/0805/X7R, RFB_top = 100kΩ, CFB = 100pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
Vin	Input voltage range		+2.7	-	+5.5	V
UVLO	Input Under voltage lockout	Vin increasing	2.3	2.4	2.5	V
I_{SD}	Input shutdown current	Vin=3.3V, EN=GND	-	5.0	-	uA
I_{IN}	Input supply bias current	Vin=3.3V, Iout=0A Vout=1.8V, EN=HIGH	-	12	-	mA
I_S	Input supply current	Vin=3.3V, EN=HIGH Iout=2.0A Vout=1.8V	-	1.22	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output current		0	-	2	A
V_{FBREF}	Feedback Regulation Voltage		591	600	609	mV
R_{DR}	Dropout resistance	100% on duty	-	90	-	mΩ
Tss	Soft start		-	2.1	-	mS

ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2 oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 3.3V, Vout = 1.8V, Cin =22uF/6.3V/0805/X7R, Cout = 22uF/6.3V/0805/X7R, RFB_top = 100kΩ, CFB = 100pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
V_{EN_TH}	Enable upper threshold voltage	V_{EN_TH} rising	1.17	1.2	1.23	V
	Enable lower threshold voltage	V_{EN_TH} falling	1.07	1.1	1.13	V
EN_{PDR}	Internal Pull Down Resistor		-	1	-	MΩ
F_{OSC}	Oscillator frequency	PWM Operation	-	1.2	-	MHz
V_{PGUV_TH}	PG Under-Voltage Lower Threshold	V_{FB} rising, PG Low-to-HiZ, % with respect to V_{FEREF}	-	-10	-	%
V_{PGUV_HY}	PG Under-Voltage Hysteresis	V_{FB} falling, PG HiZ-to-Low % with respect to V_{FEREF}	-	-15	-	%
V_{PGOV_HY}	PG Over-Voltage Hysteresis	V_{FB} rising, PG HiZ-to-Low % with respect to V_{FEREF}	-	15	-	%
V_{PGOV_TH}	PG Over-Voltage Upper Threshold	V_{FB} falling, PG Low-to-HiZ, % with respect to V_{FEREF}	-	10	-	%
PG_{PUR}	PG Pull-up resister		-	500	-	KΩ
V_{PG_LV}	PG logic low voltage	I_{PG} = 1mA	-	0.2	0.3	V
■ Fault Protection						
I_{LIMIT_TH}	Current limit threshold	Peak value of output current	-	5.2	-	A
T_{OTP}	Over temperature protection		-	160	-	°C
T_{HY}	Thermal Shutdown Hysteresis		-	30	-	°C
OVP	Over voltage protection	VFB rising, % with respect to V_{REF}	+18	+20	+22	%

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin =22uF/6.3V/0805/X7R, Cout = 22uF/6.3V/0805/X7R, RFB_top = 100kΩ, CFB = 100pF.
The following figures provide the typical characteristic curves at 1.0Vout.

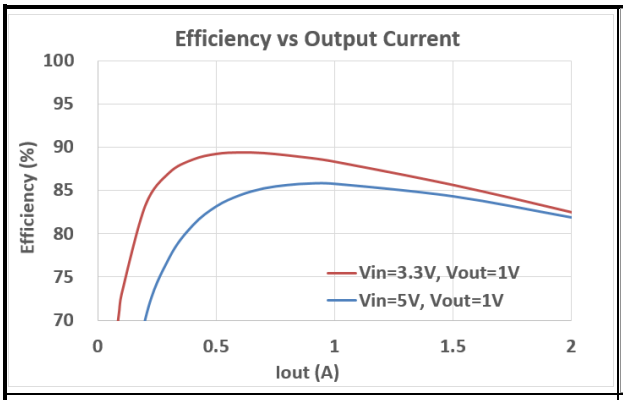


FIG.3 EFFICIENCY V.S. LOAD CURRENT

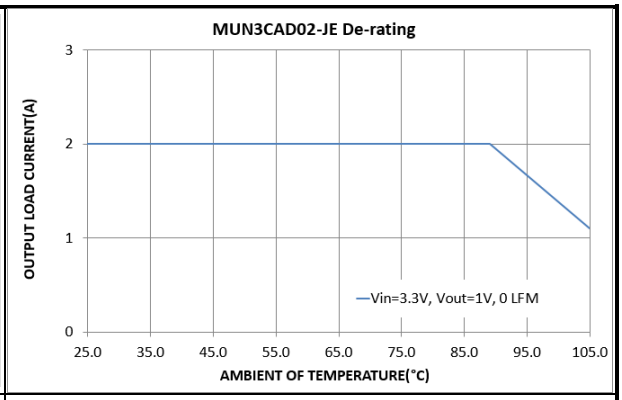


FIG.4 DE-RATING CURVE

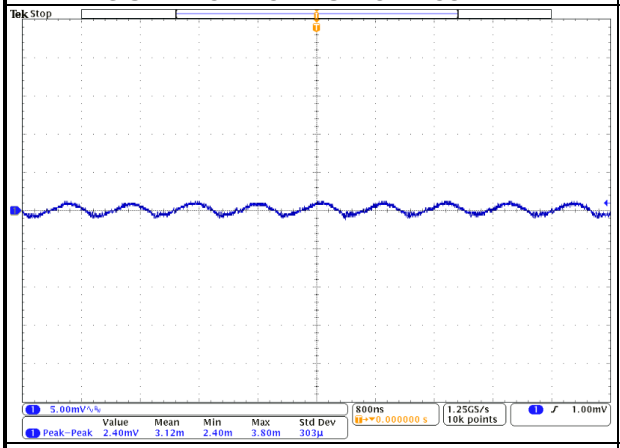


FIG.5 OUTPUT RIPPLE
(Vin=3.3V, Vout=1.0V, Iout=0A)

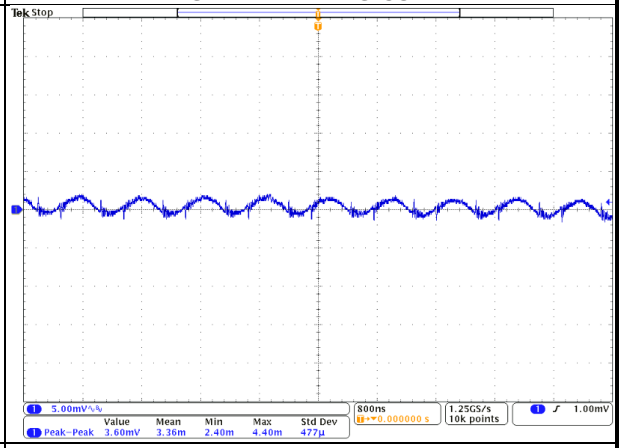


FIG.6 OUTPUT RIPPLE
(Vin=3.3V, Vout=1.0V, Iout=2A)

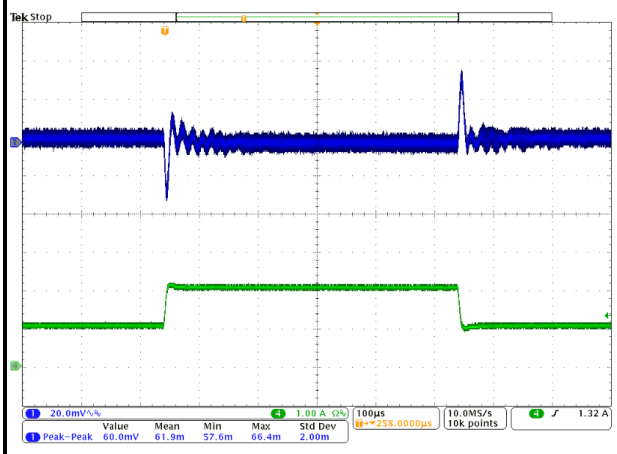


FIG.7 TRANSIENT RESPONSE
(Vin=3.3V, Vout=1V, Iout=1A to 2A load step)

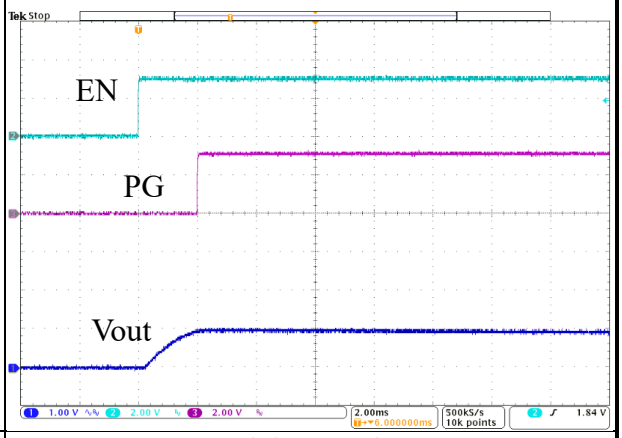


FIG.8 TURN-ON
(Vin=3.3V, Vout=1.0V, Iout=2A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin =22uF/6.3V/0805/X7R, Cout = 22uF/6.3V/0805/X7R, RFB_top = 100kΩ, CFB =100pF.
The following figures provide the typical characteristic curves at 1.8Vout.

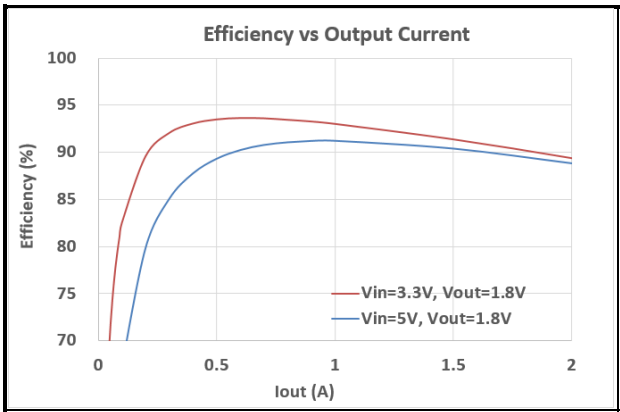


FIG.9 EFFICIENCY V.S. LOAD CURRENT

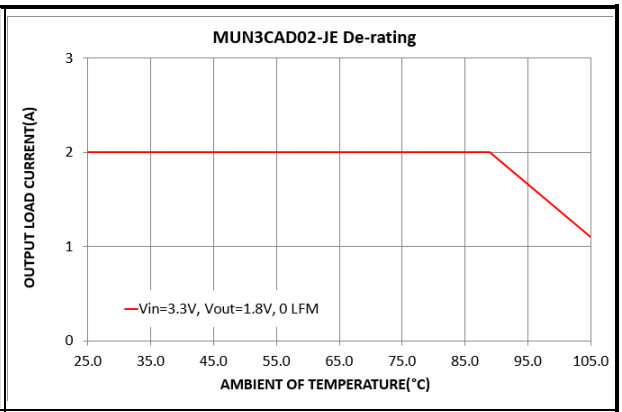


FIG.10 DE-RATING CURVE

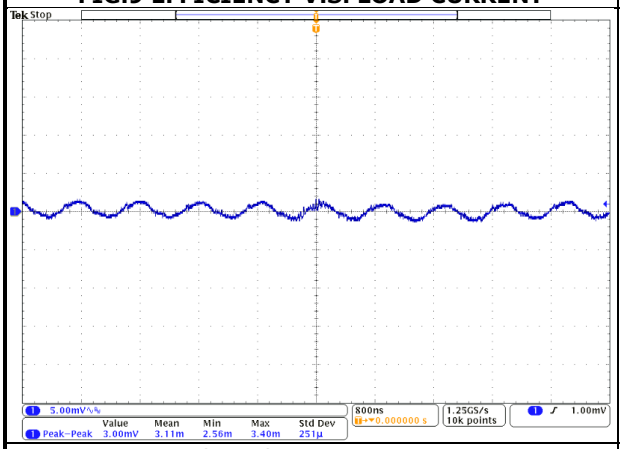


FIG.11 OUTPUT RIPPLE
(Vin=3.3V, Vout=1.8V, Iout=0A)

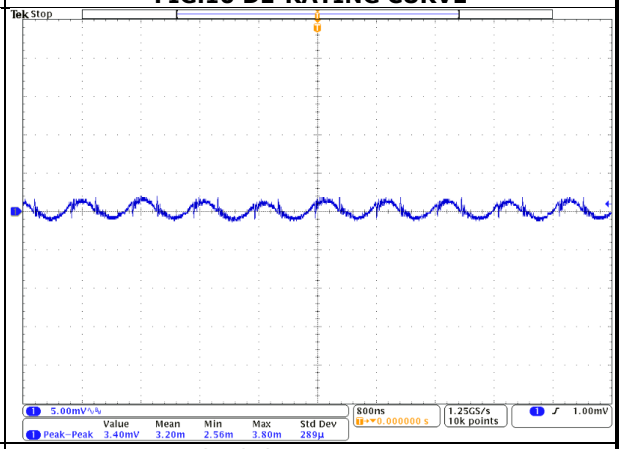


FIG.12 OUTPUT RIPPLE
(Vin=3.3V, Vout=1.8V, Iout=2A)

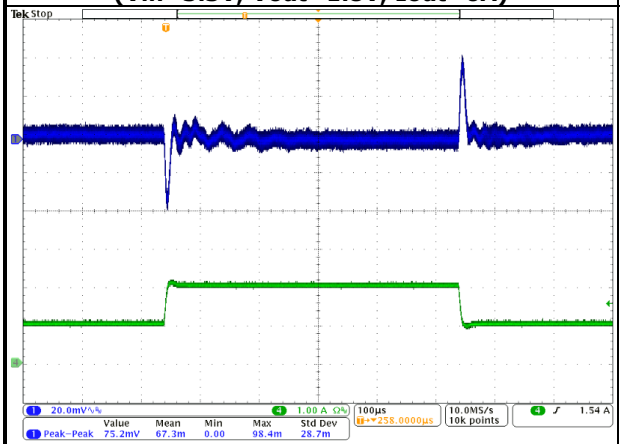


FIG.13 TRANSIENT RESPONSE
(Vin=3.3V, Vout=1.8V, Iout=1A to 2A load step)

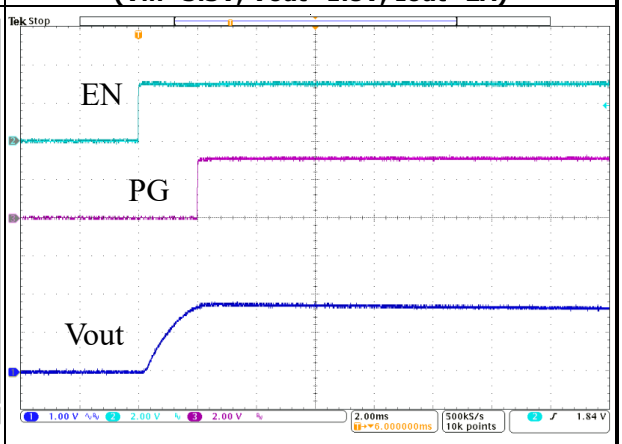


FIG.14 TURN-ON
(Vin=3.3V, Vout=1.8V, Iout=2A)

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 30mm×30mm×1.6mm, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin =22uF/6.3V/0805/X7R, Cout = 22uF/6.3V/0805/X7R, RFB_top = 100kΩ, CFB = 100pF.
The following figures provide the typical characteristic curves at 3.3Vout.

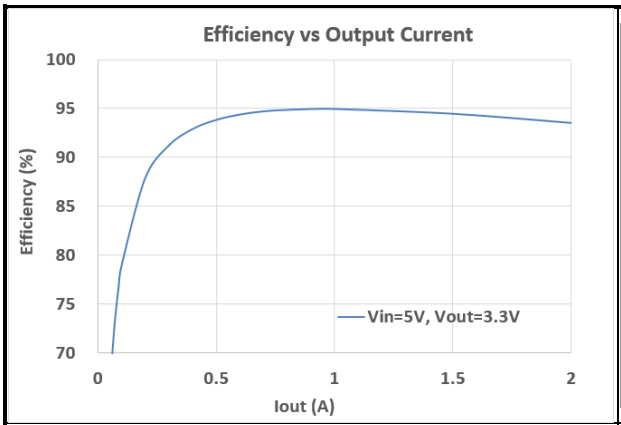


FIG.15 EFFICIENCY V.S. LOAD CURRENT

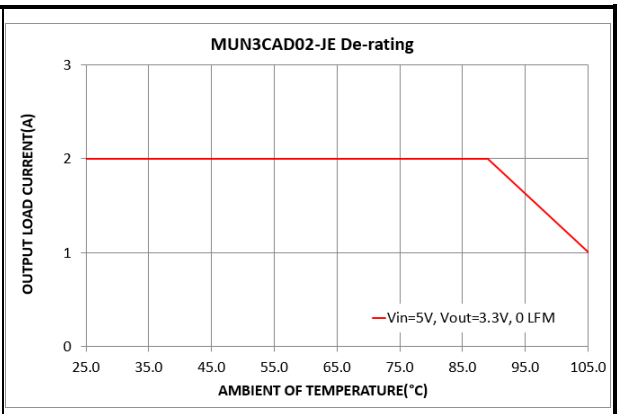


FIG.16 DE-RATING CURVE

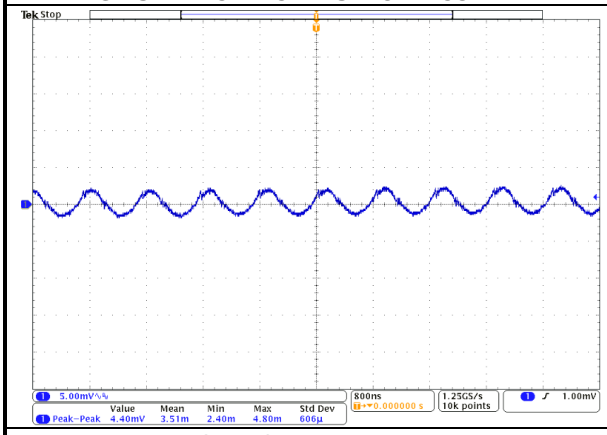


FIG.17 OUTPUT RIPPLE
(Vin=5V, Vout=3.3V, Iout=0A)

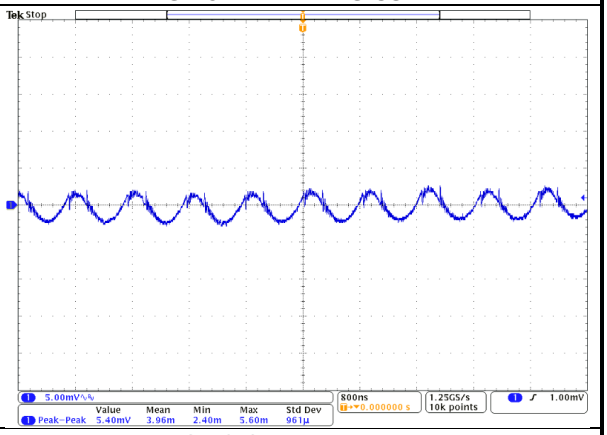


FIG.18 OUTPUT RIPPLE
(Vin=5V, Vout=3.3V, Iout=2A)

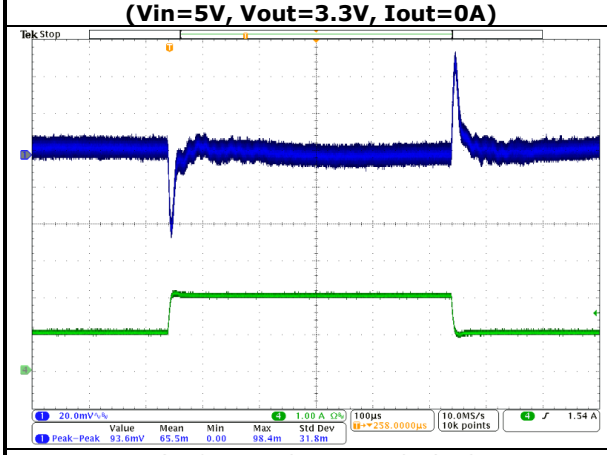


FIG.19 TRANSIENT RESPONSE
(Vin=5V, Vout=3.3V, Iout=1A to 2A load step)

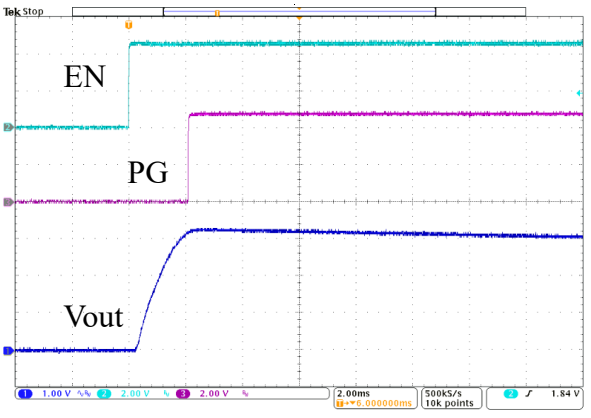


FIG.20 TURN-ON
(Vin=5V, Vout=3.3V, Iout=2A)

APPLICATIONS INFORMATION:

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected to as low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. Input capacitors must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response to as step load change, the additional capacitors at the output must be used. Low ESR ceramic, X5R or X7R capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The output voltage can be programmed by the dividing resistor RFB_top (recommended 10k~200kohm) and RFB_bot, Assume RFB_top set 100 Kohm, the output voltage can be calculated as shown in Equation 1 and the resistance according to typical output voltage is shown in TABLE 1.

$$\text{VOUT (V)} = 0.6 \times \left(1 + \frac{\text{RFB\_top}}{\text{RFB\_bot}}\right) \qquad \text{(EQ.1)}$$

VOUT (V)	RFB_top (kΩ)	RFB_bot(kΩ)
1.0	100	150
1.2	100	100
1.8	100	50
2.5	100	31.58
3.3	100	22.22

TABLE.1 RESISTOR VALUES FOR COMMON OUTPUT VOLTAGES

APPLICATIONS INFORMATION: (Cont.)

LOAD TRANSIENT RESPONSE INCREASE:

In some applications, adding a ceramic cap (CFB) in parallel with RFB-top may further speedy up the load transient responses, recommend capacitance 100pF~470pF.

THERMAL CONSIDERATIONS:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers 2oz. The case temperature of module sensing point is shown as FIG.21 Then Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

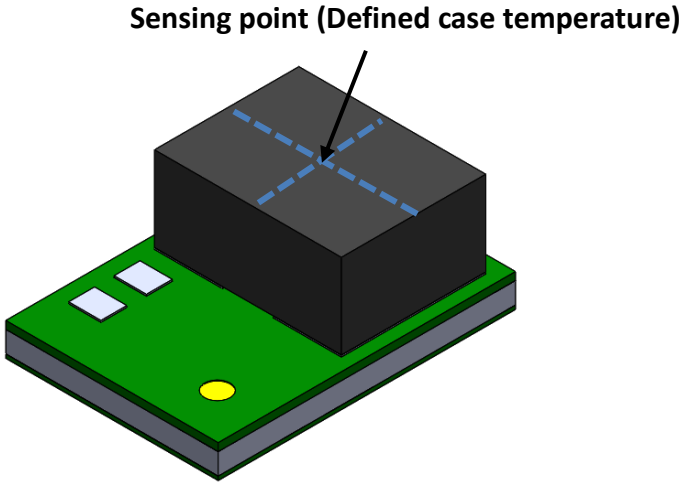


FIG.21 CASE TEMPERATURE SENSING POINT

APPLICATIONS INFORMATION: (Cont.)

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 22 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60~150 seconds to melt the solder and make the peak temperature at the range from 255°C to 260°C (Do not exceed 30 sec). It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

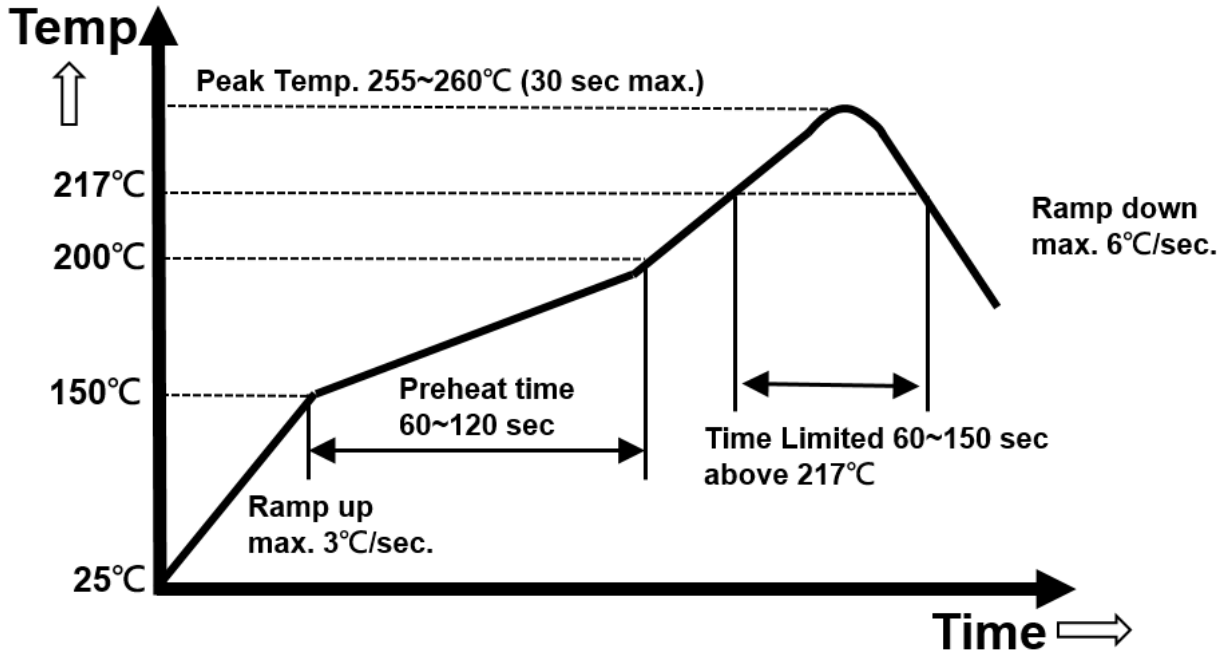
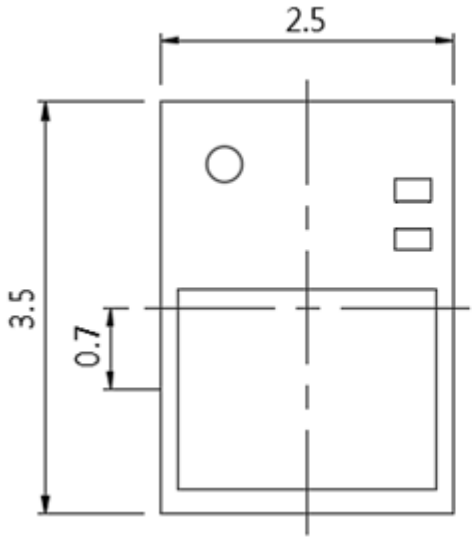


FIG.22 RECOMMENDATION REFLOW PROFILE

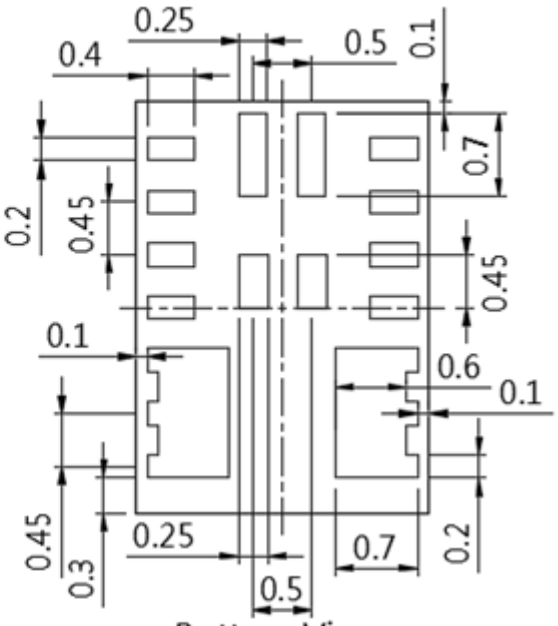
(Not to scale)

***Refer to the Classification Reflow Profile of J-STD-020.**

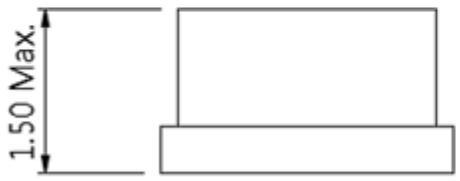
PACKAGE OUTLINE DRAW:



Top View



Bottom View

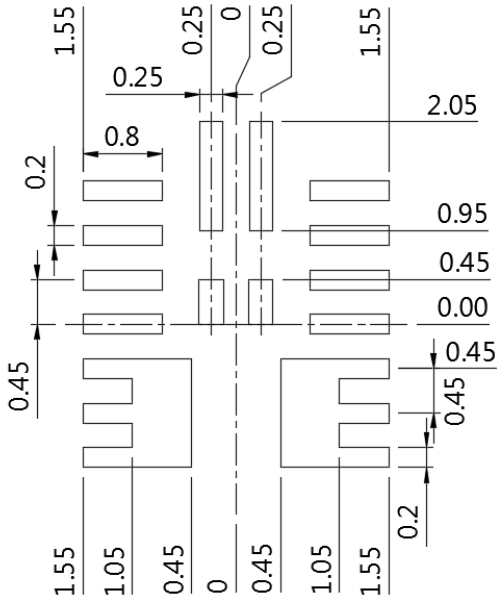


Side View

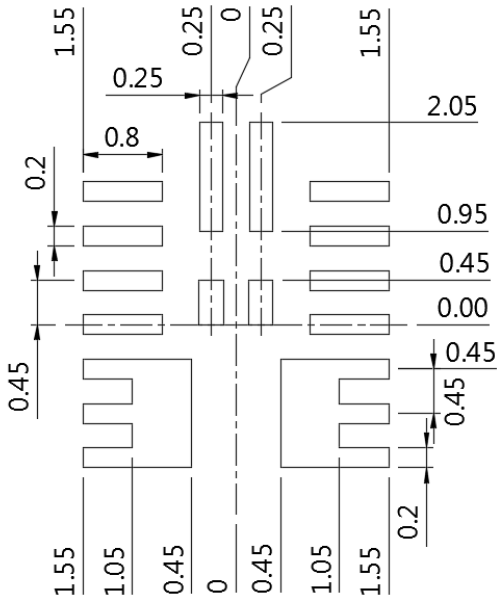
Unit : mm
General Tolerance: ±0.1mm

LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL PATTERN

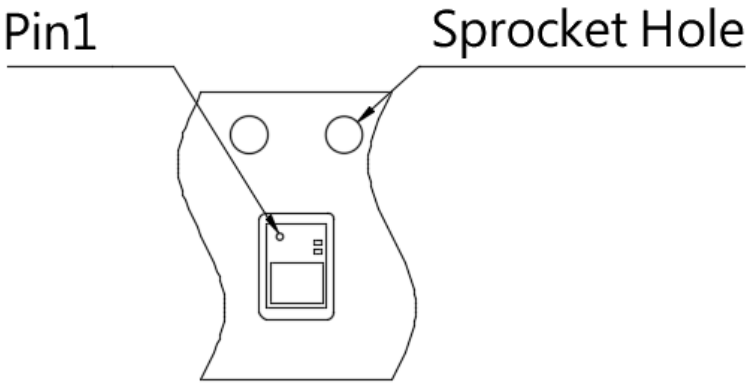
*Based on 0.1~0.15mm thickness stencil (Reference only)

*Recommended solder paste coverage 55~100%

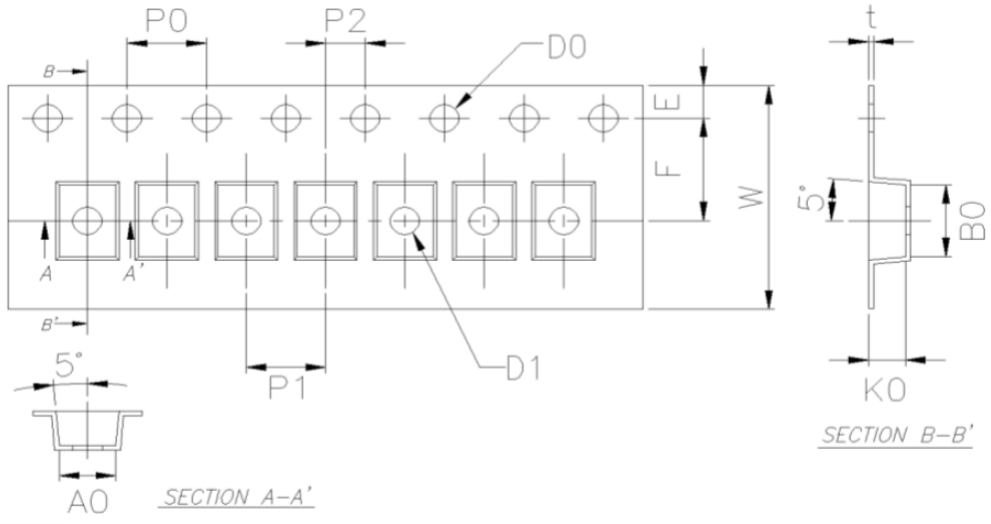
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension

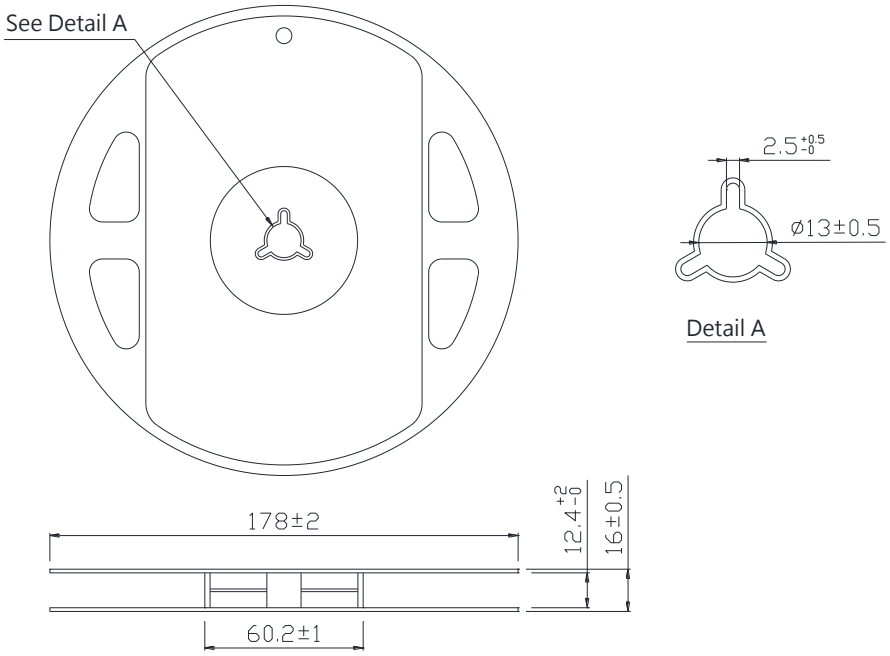


A0	2.85± 0.10	E	1.75 ± 0.10
B0	3.85 ± 0.10	K0	1.85 ± 0.10
F	5.50 ± 0.05	P0	4.00 ± 0.10
W	12.00 ±0.30	P1	4.00 ± 0.10
D0	φ1.55 ±0.05	P2	2.00 ± 0.05
D1	φ1.50± 0.10	t	0.25 ± 0.05

PACKING REFERENCE: (Cont.)

Unit: mm

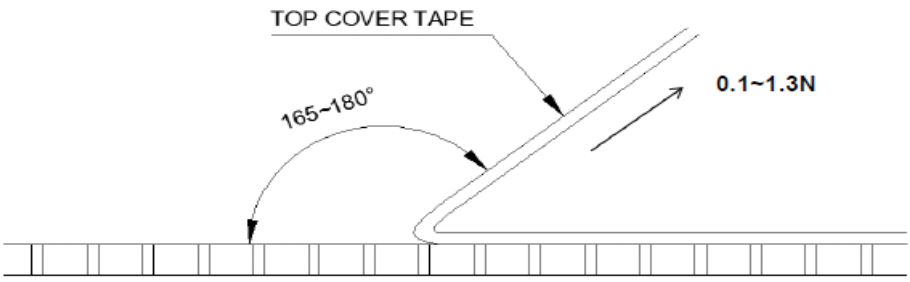
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape is between 0.1N to 1.3N



REVISION HISTORY:

Date	Revision	Changes
2021.01.04	P00	Release the preliminary specification.
2021.04.12	P01	1、Update Outline of Module. 2、Update package outline draw.
2021.09.06	P02	Update the typical performance characteristics.
2021.11.11	P03	Modify the package outline.
2022.03.07	P04	Update the electrical specifications.
2022.05.11	P05	Update carrier tape dimension and quantity per reel to 2000 EA. Modify the reflow parameters.
2022.12.23	P06	1、Page 11, update reflow parameters. 2、Page 13, change the thickness description of stencil. Add note and unit.