Datasheet

180V Three-phase Gate Driver
FD6187T

Fortior Technology (Shenzhen) Co., Ltd

Contents

180V Three-phase Gate Driver

1 System Introduction

1.1 Overview

FD6187T is an integrated circuit (IC) that integrates three independent half-bridge gate drivers. It is specially designed for high-voltage and high-speed MOSFET driver applications.

FD6187T supports under-voltage lockout (UVLO) feature, protecting the power tube from operating with insufficient voltage.

FD6187T also provides cross-conduction prevention and deadtime insertion to effectively protect the power IC and prevent both MOSFETs of each half-bridge from switching on at the same time.

FD6187T has built-in input signal filtering module to avoid input noise interference.

1.2 Package

TSSOP20

1.3 Features

- Fully operational to +180V
- Power supply: 5.0V ~ 22V
- Three independent half-bridge drivers
- Output current: +0.8A/-0.8A
- 3.3V/5V logic input compatible
- VCC UVLO
- Cross-conduction prevention logic
- Built-in deadtime module
- Built-in input filtering module
- High-side outputs in phase with inputs, and low-side outputs out of phase with inputs

1.4 Applications

- Electric vehicles, self-balancing vehicles, electric scooters, etc.
- Motor drive applications

1.5 Typical Application Diagram

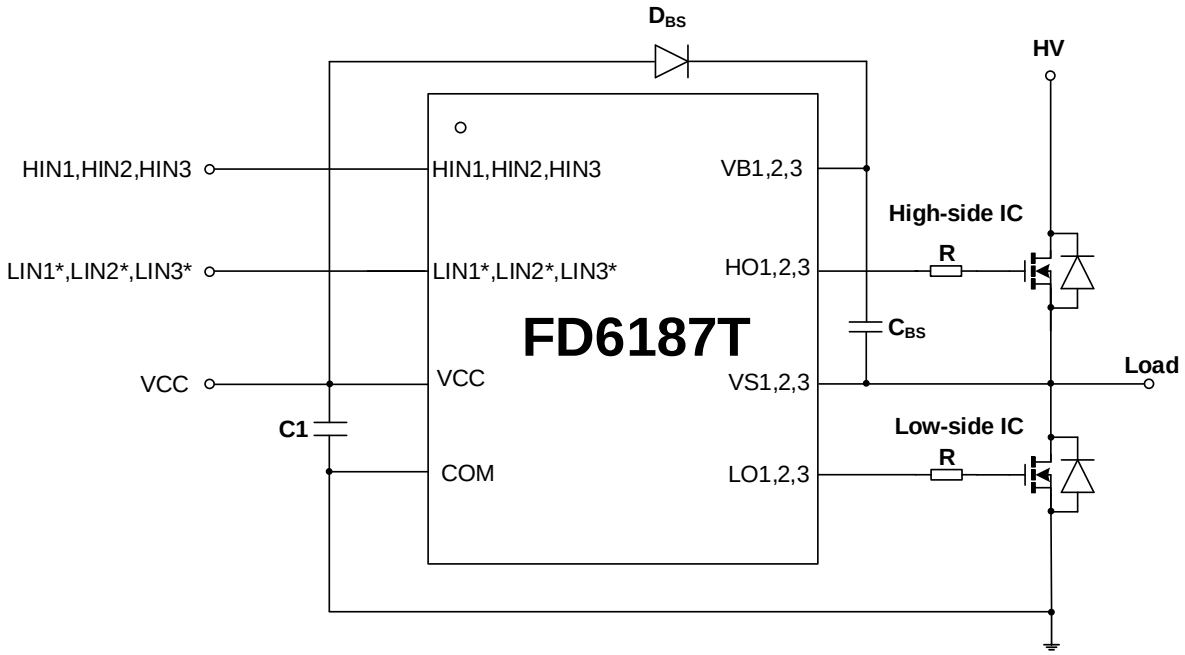


Figure 1-1 Typical Application Diagram of FD6187T

- C1: 10μF ~ 100μF power filter capacitor depending on the application circuit.
- R: Gate drive resistor. The resistance depends on deadtime and the device being driven.
- D_{BS}: Bootstrap diode. Those with high reverse breakdown voltage and short recovery time are preferred.
- C_{BS}: Bootstrap capacitor. 1μF ~ 100μF ceramic capacitor or tantalum capacitor is preferred.

Note: The above circuit and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.6 Functional Block Diagram

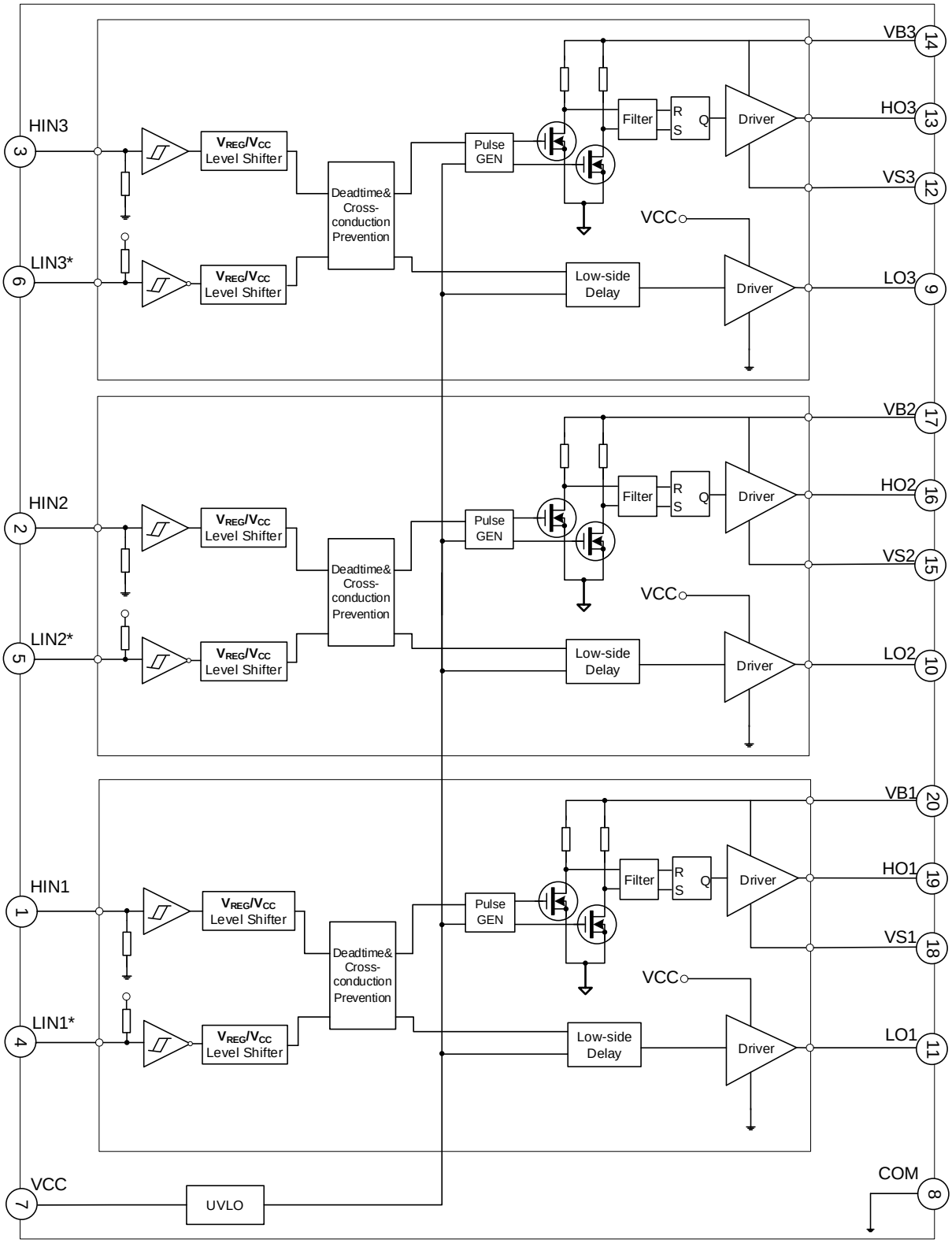


Figure 1-2 Functional Block Diagram of FD6187T

1.7 Pin Definitions

1.7.1 FD6187T TSSOP20 Pin Diagram

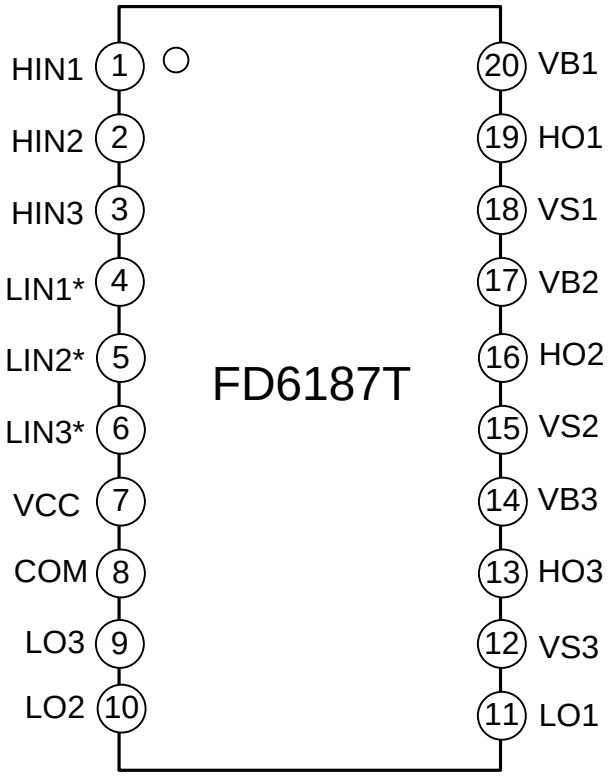


Figure 1-3 FD6187T TSSOP20 Pin Diagram

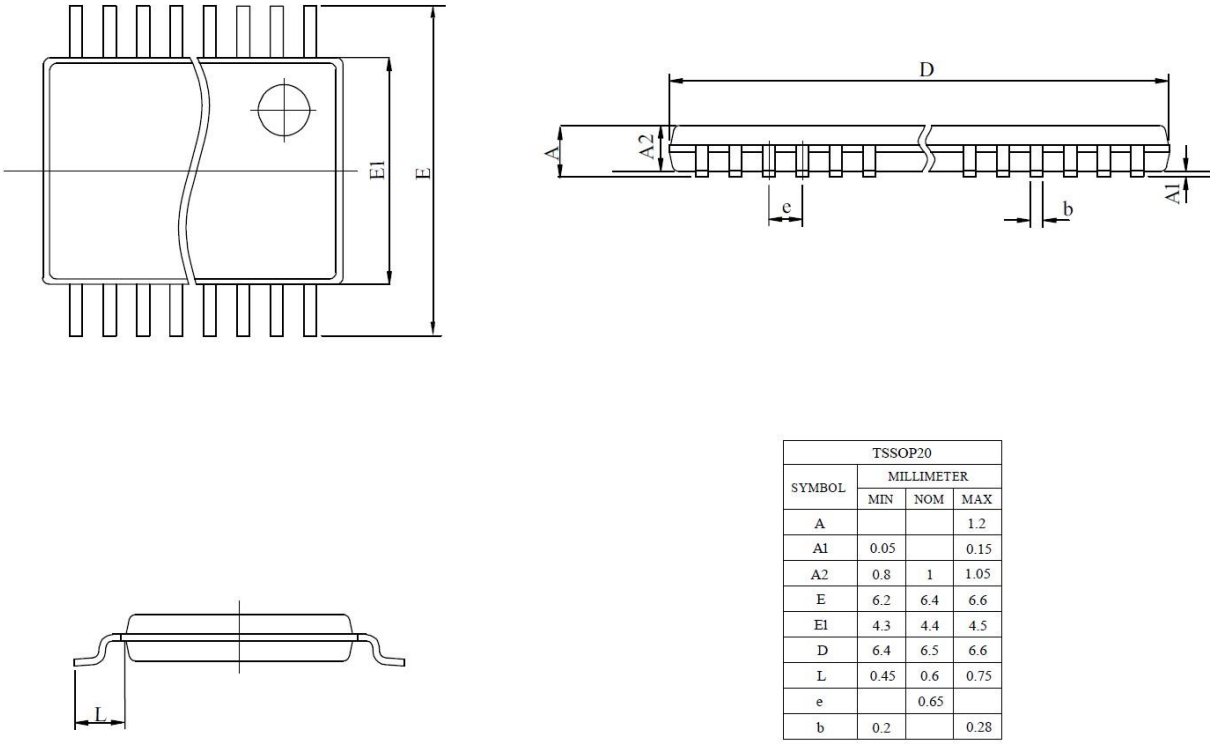
1.7.2 FD6187T TSSOP20 Pins

Table 1-1 FD6187T TSSOP20 Pin Descriptions

Pin	Name	Description
1, 2, 3	HIN1, HIN2, HIN3	High-side Input
4, 5, 6	LIN1*, LIN2*, LIN3*	Low-side Input
7	VCC	Low-side Supply Voltage
8	COM	Ground
9, 10, 11	LO3, LO2, LO1	Low-side Output
12, 15, 18	VS3, VS2, VS1	High-side Floating Offset Voltage
13, 16, 19	HO3, HO2, HO1	High-side Output
14, 17, 20	VB3, VB2, VB1	High-side Floating Absolute Voltage

2 Package Information

2.1 FD6187T TSSOP20



TSSOP20			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.2
A1	0.05		0.15
A2	0.8	1	1.05
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
D	6.4	6.5	6.6
L	0.45	0.6	0.75
e		0.65	
b	0.2		0.28

Figure 2-1 FD6187T TSSOP20 Package Drawings and Dimensions

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6187T	TSSOP20	FD6187T	Tape & Reel	4000

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter		Symbol	Min. ~ Max.	Unit
High-side Floating Absolute Voltage		$V_{B1,2,3}$	-0.3 ~ 205	V
High-side Floating Offset Voltage		$V_{S1,2,3}$	$V_{B1,2,3}$ - 25 ~ $V_{B1,2,3}$ + 0.3	V
High-side Output Voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3 ~ $V_{B1,2,3}$ + 0.3	V
Low-side Supply Voltage		V_{CC}	-0.3 ~ 25	V
Low-side Output Voltage		$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Logic Input Voltage (HIN, LIN*)		V_{IN}	-0.3 ~ V_{CC} + 0.3	V
Power Dissipation @ $T_A \leq 25C°$	TSSOP20	P_D	≤ 1.25	W
Junction-to-ambient Thermal Resistance	TSSOP20	R_{thJA}	≤ 100	℃/W
Junction Temperature		T_j	≤ 150	℃
Storage Temperature		T_{stg}	-55 ~ 150	℃

Notes:

- In any case, power dissipation shall not exceed P_D.
- The chip may get damaged if it operates at voltages exceeding those listed above.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

(All voltages are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ + 4.0	$V_{S1,2,3}$ + 22	V
High-side Floating Offset Voltage	$V_{S1,2,3}$	-5	180	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side Supply Voltage	V_{CC}	5.0	22	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic Input Voltage (HIN, LIN*)	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	℃

Note:

[1] Exposure to recommended operating conditions for extended periods may affect device reliability.

3.3 Electrical Characteristics

Table 3-3 Electrical Characteristics

(T_A = 25℃, V_{CC} = $V_{BS1,2,3}$ = 15V and $V_{S1,2,3}$ = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC} Quiescent Current	I_{QCC}	VIN = 0V or 5V	-	330	500	μA
V_{BS} Quiescent Current	I_{QBS}	VIN = 0V or 5V	-	70	120	μA
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 180V	-	0.1	5.0	μA
Input HIN/LIN*						
High-level Input Threshold Voltage	V_{IH}		2.7	2.1	-	V
Low-level Input Threshold Voltage	V_{IL}		-	1.4	0.8	V
LIN* High-level Input Bias Current	I_{LIN*+}	V_{LIN*} = 0V	-	25	50	μA
LIN* Low-level Input Bias Current	I_{LIN*-}	V_{LIN*} = 5V	-	-	4	μA
HIN High-level Input Bias Current	I_{HIN+}	V_{HIN} = 5V	-	25	50	μA
HIN Low-level Input Bias Current	I_{HIN-}	V_{HIN} = 0V	-	-	4	μA
HIN Input Pull-down Resistor	R_{HIN}		100	200	300	KΩ
LIN* Input Pull-up Resistor	R_{LIN*}		100	200	300	KΩ
UVLO						
V_{CC} UVLO Threshold Voltage	V_{CCUV+}		3.8	4.4	5.0	V
V_{CC} UVLO Release Voltage	V_{CCUV-}		3.5	4.1	4.7	V
V_{CC} UVLO Hysteresis Voltage	V_{CCUVH}		0.2	0.3	-	V
High-side/Low-side Output						
High-side Output Voltage	V_{OH}	I_O = 100mA	-	1.0	1.5	V
Low-side Output Voltage	V_{OL}	I_O = 100mA	-	0.5	0.75	V
High-level Output Short-circuit Pulsed Current	I_{OH}	V_O = 0V	0.5	0.8	-	A
Low-level Output Short-circuit Pulsed Current	I_{OL}	V_O = 15V	0.5	0.8	-	A
Time Parameters						
Turn-on Propagation Delay	t_{on}		-	180	300	ns
Turn-off Propagation Delay	t_{off}		-	70	130	ns
Turn-on Rise Time	t_r	C_L = 1000pF	-	30	70	ns
Turn-off Fall Time	t_f	C_L = 1000pF	-	30	70	ns
High-low Side Delay Match	MT		-	-	50	ns
Deadtime	DT		-	100	-	ns

4 Propagation Delay Test Standards

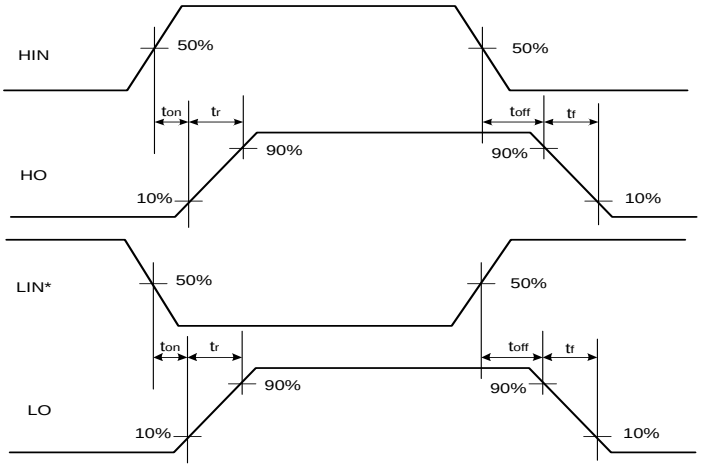


Figure 4-1 Propagation Delay Test Standards

5 Propagation Delay Matching Test Standards

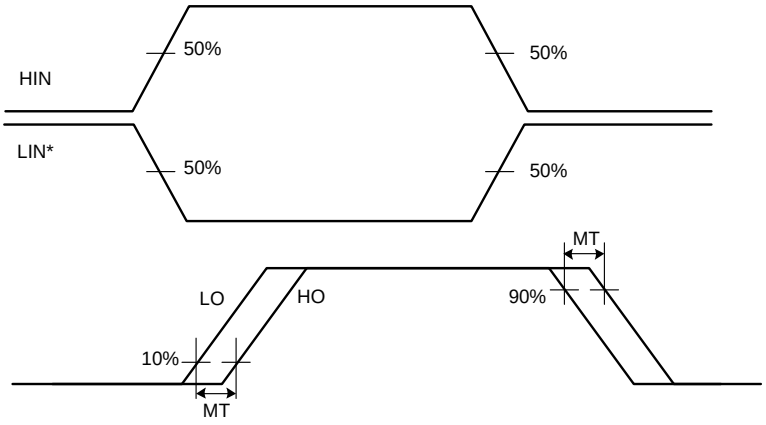


Figure 5-1 Propagation Delay Matching Test Standards

6 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs from damage when high-side and low-side input signals are interfered. The figure below shows how the protection circuit works.

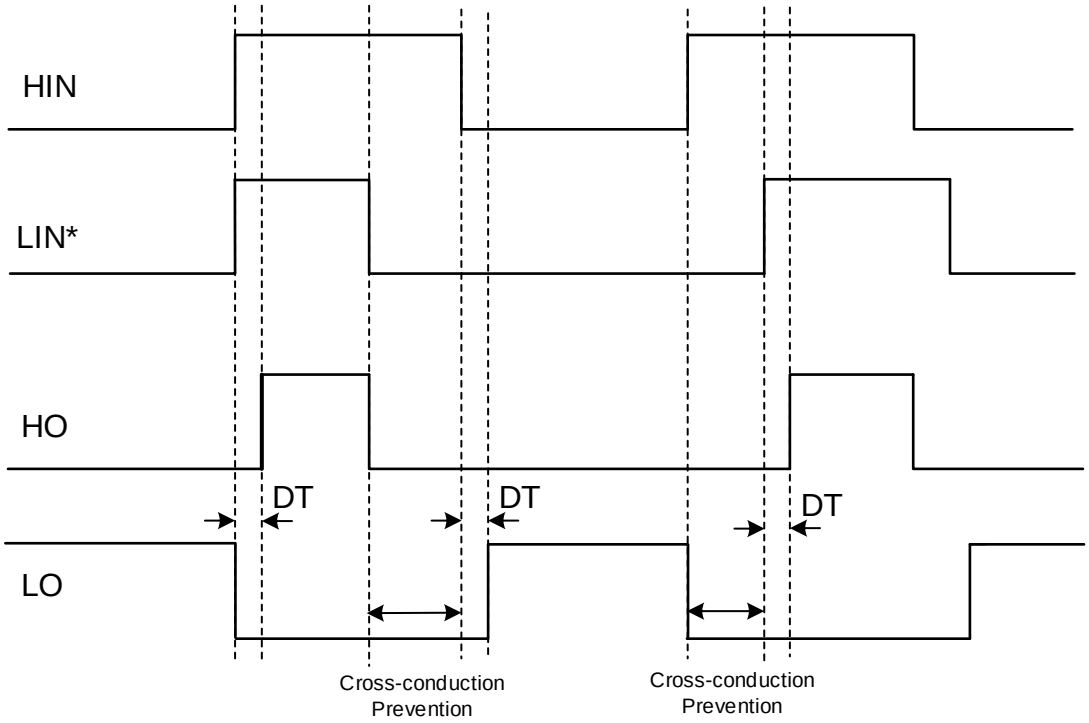


Figure 6-1 Schematic Diagram of Cross-conduction Prevention

7 Deadtime

The chip is designed with dedicated deadtime protection circuit. Both the high-side and low-side outputs are set to LOW during the deadtime. This feature prevents both MOSFETs of each half-bridge from switching on at the same time.

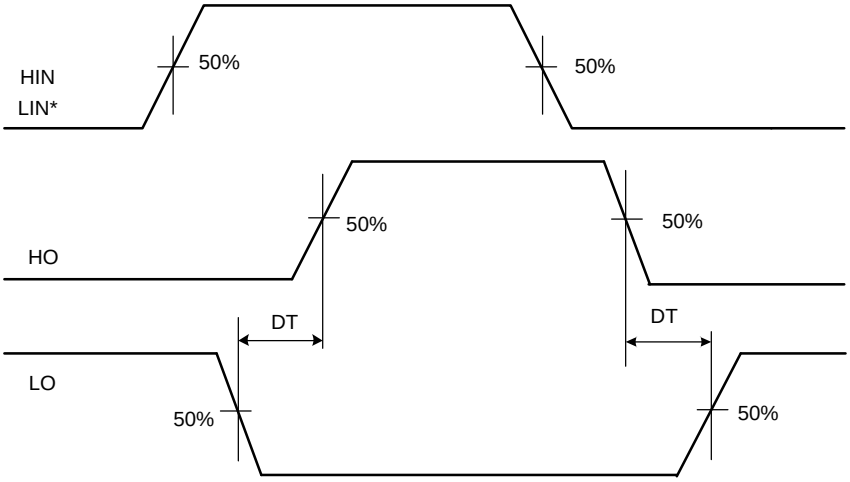


Figure 7-1 Schematic Diagram of Deadtime

8 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release, translated from Chinese version 1.0	2024/01/19	Eric Deng

Copyright Notice

Right to make changes — Fortior Technology (Shenzhen) Co., Ltd. reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. The information contained in this manual is provided for the general use by our customers. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. It is the policy of Fortior Technology (Shenzhen) Co., Ltd. to respect the valid patent rights of third parties and not to infringe upon or assist others to infringe upon such rights.

If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard.

Fortior Technology (Shenzhen) Co., Ltd.
Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com