FD6189T

140V 3-PHASE BRIDGE RIVER

Overview

FD6189T is a Half-bridge Gate Driver designed for driving high-voltage, high-speed N-type power MOSFET, and workable at 140V circuit.

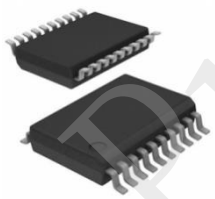
FD6189T has built-in under-voltage (UVLO) protection to prevent the power tube at low voltage to work, and also for improving efficiency.

FD6189T has also built-in input signal filtering to prevent input noise. It can also prevent the short-circuit turning on of MOSFETs, and thus protect effectively the power devices

Features

- Fully operational to +140V
- Gate driver supply range from 5.3V to 22V
- Output current: +0.8A/-0.8A
- Independent Three half-bridge drivers
- Input logic compatible: 3.3V/5V
- VCC Undervoltage protection (UVLO)
- Cross-conduction prevention logic
- Built-in 100ns dead time zone
- Matched propagation delay for both channels
- High side output is in phase with the high side input
- Low side output is out of phase with the low side input
- RoHS compliant

Packages



TSSOP-20

Applications

- Motor drives
- DC-AC inverter drives

1. Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air condition.

Definition	Symbol	Min~Max	Units
High side floating supply voltage	$V_{B1,2,3}$	-0.3～165	V
High side floating supply offset voltage	$V_{S1,2,3}$	$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
High side floating output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3～$V_{B1,2,3}$+0.3	V
Low side and logic fixed supply voltage	V_{CC}	-0.3～25	V
Low side output voltage	$V_{LO1,2,3}$	-0.3～V_{CC}+0.3	V
Logic input voltage（HIN,LIN*）	V_{IN}	-0.3～6.5	V
Package power dissipation @T_A≤25°C	P_D	≤1.25	W
Thermal resistance, junction to ambient	R_{thJA}	≤100	°C/W
Junction temperature	T_j	≤150	°C
Storage temperature	T_{stg}	-55～150	°C

Note1: In any case, power dissipation should not exceed P_D.

Note2: Voltages above the absolute maximum ratings may damage the chip.

2. Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15V differential.

Definition	Symbol	Min	Max	Units
High side floating supply voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+4	$V_{S1,2,3}$+22	V
High side floating supply offset voltage	$V_{S1,2,3}$	-	140	V
High side floating output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low side and logic fixed supply voltage	V_{CC}	5.3	22	V
Low side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic input voltage（HIN,LIN*）	V_{IN}	0	5.5	V
Ambient temperature	T_A	-40	125	°C

Note1: The long-term operation of the chip outside the recommended conditions may affect its reliability. It is not recommended to work in an environment that exceeds the recommended conditions.

3. Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) =15V and TA =25°C unless otherwise specified. All the parameters are referenced to COM.

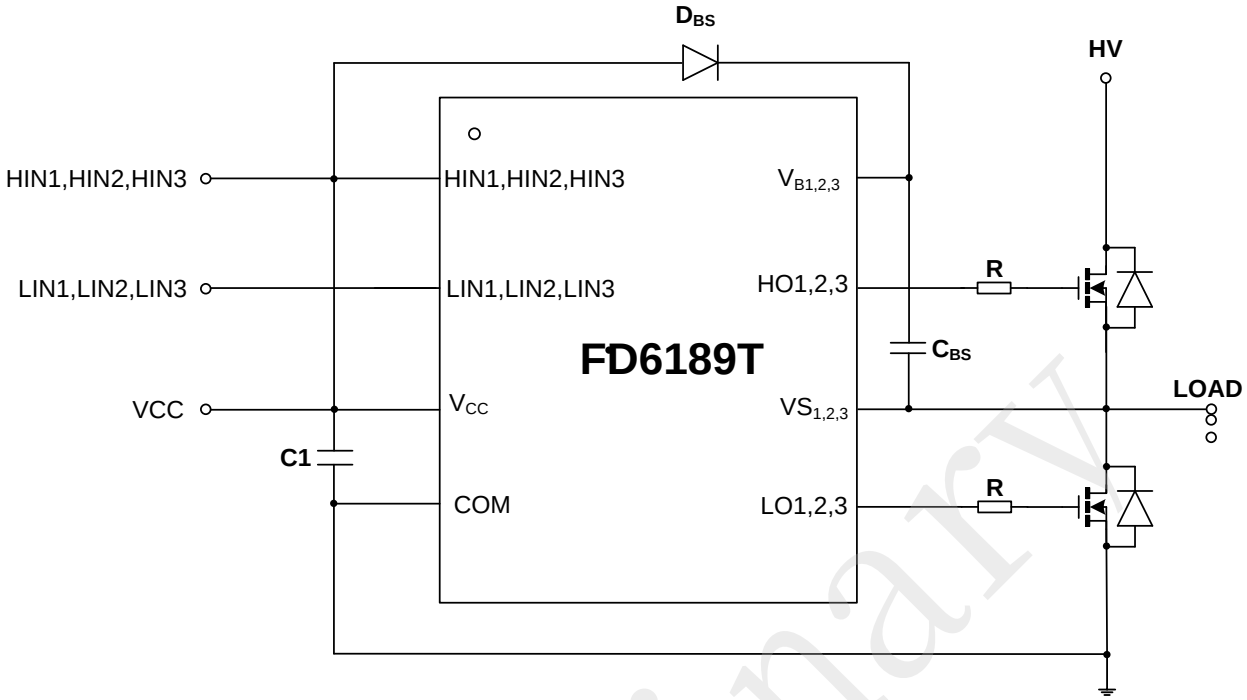
Definition	Symbol	Test conditions	Min.	Typ.	Max.	Units
Logic "1" input voltage	V_{IH}		2.7	2.0	--	V
Logic "0" input voltage	V_{IL}		--	1.3	0.8	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O=20mA	--	0.2	0.34	
low level output voltage, V_O	V_{OL}		--	0.1	0.17	
Offset supply leakage current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=140V	-	0.1	5.0	uA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN} =0V or 5V	-	45	90	
Quiescent V_{CC} supply current	I_{QCC}		-	800	1500	
Logic "1" input bias current	I_{LIN*+}	V_{LIN*}=0V	--	24	40	
	I_{HIN+}	V_{HIN}=5V	--	24	40	
Logic "0" input bias current	I_{LIN*-}	V_{LIN*}=5V				
	I_{HIN-}	V_{HIN}=0V	--	--	4	
V_{CC} supply undervoltage positive going threshold	V_{CCUV+}		4.3	4.8	5.3	V
V_{CC} supply undervoltage negative going threshold	V_{CCUV-}		4.0	4.5	5.0	
Output high short circuit pulsed current	I_{O+}	V_O=0V,PW≤10us	0.5	0.8	--	A
Output low short circuit pulsed current	I_{O-}	V_O=15V,PW≤10us	0.5	0.8	--	

4. Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) =15V, and TA =25°C, unless otherwise specified.

Definition	Symbol	Test conditions	Min.	Typ.	Max.	Units
Turn on propagation delay	ton		--	140	250	ns
Turn off propagation delay	toff		--	40	100	
Delay matching, HS & LS turn on/off	MT		--	--	50	
Turn on rise time	tr	C_L=1000pF	--	30	70	
Turn off fall time	tf	C_L=1000pF	--	30	70	
Deadtime , LS turn-off to HS turn-on & HS turn-off to LS turn-on	DT		--	100	--	

5. Typical application circuit



C1： Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

R： Gate drive resistor, and the resistance depends on the device being driven.

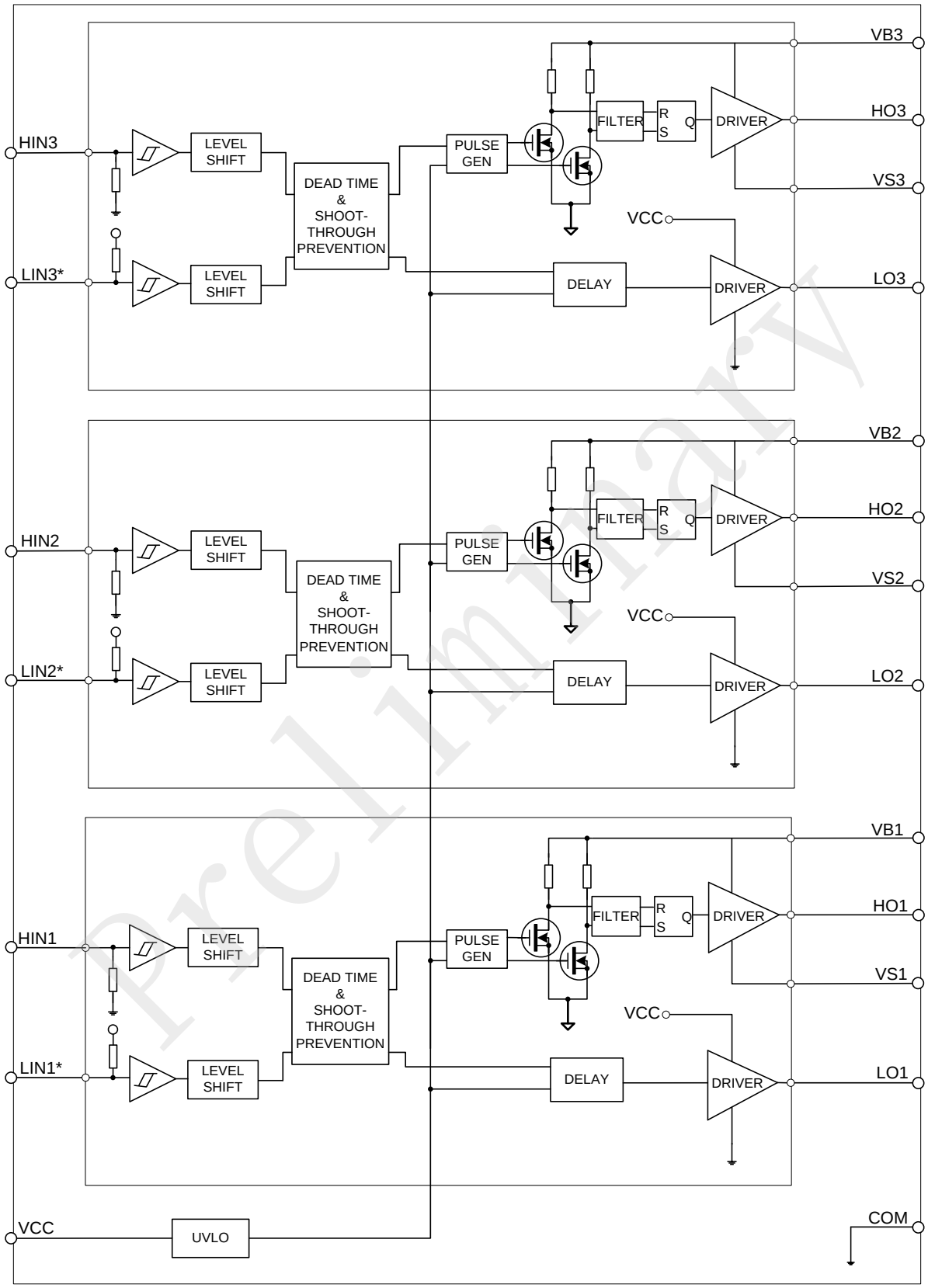
D_{BS}：Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

C_{BS}：Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose0. 22μF ~ 10μF. The capacitor should be as close as possible to the chip pin.

Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

6. Circuit Diagram



7. Chip pin configuration

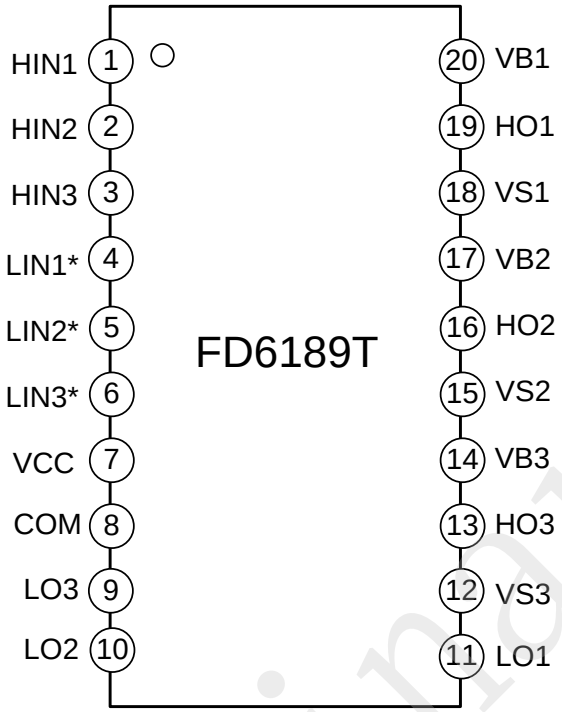
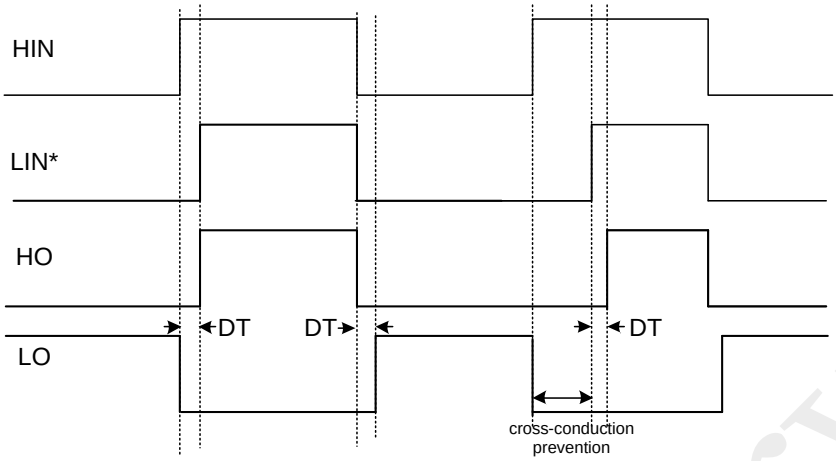


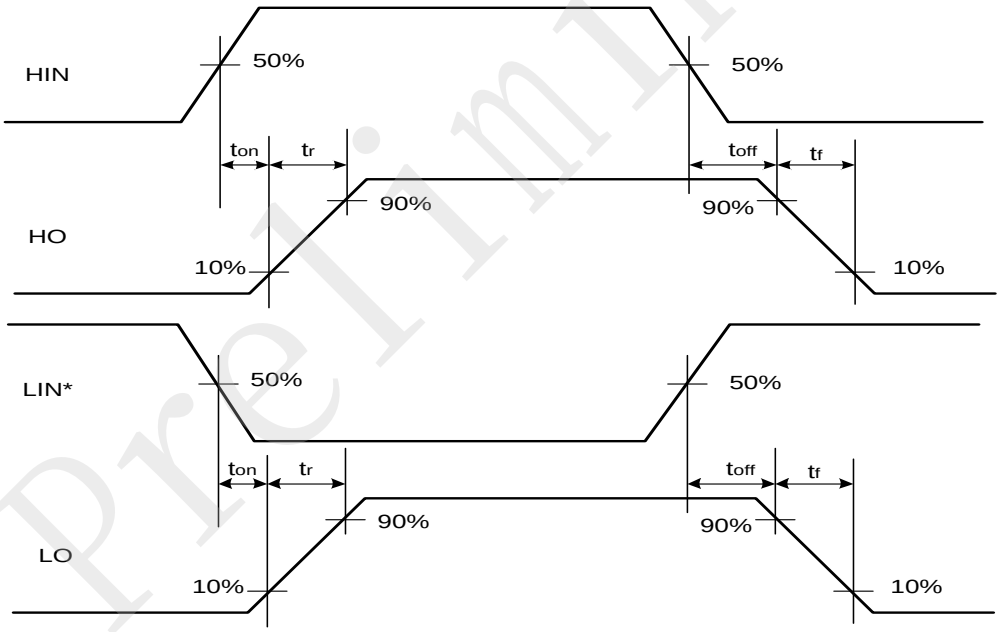
Table 7-1 Package pin

Symbol	Description
V_{CC}	Low side and logic fixed supply
HIN1,2,3	Logic input for high side gate driver output(HO),in phase
LIN1,2,3*	Logic input for low side gate driver output(LO), out of phase
COM	Low side return
LO1,2,3	Low side gate drive output
$V_{S1,2,3}$	High side floating supply return
HO1,2,3	High side gate drive output
$V_{B1,2,3}$	High side floating supply

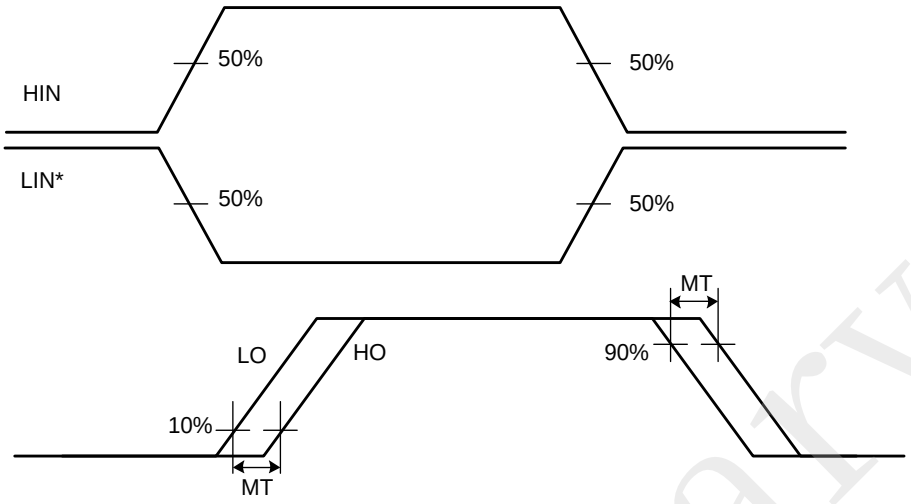
8. Logic Timing Diagram



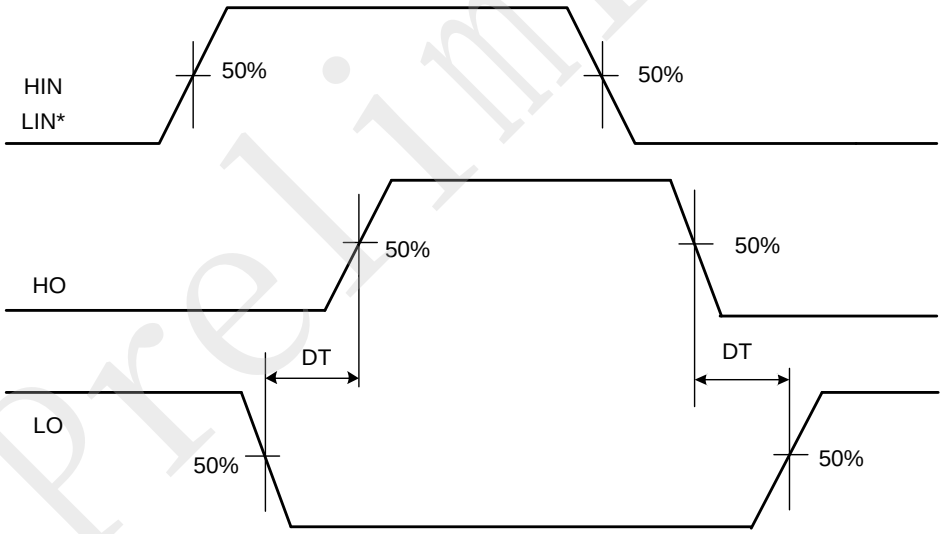
9. Switching Time test standards



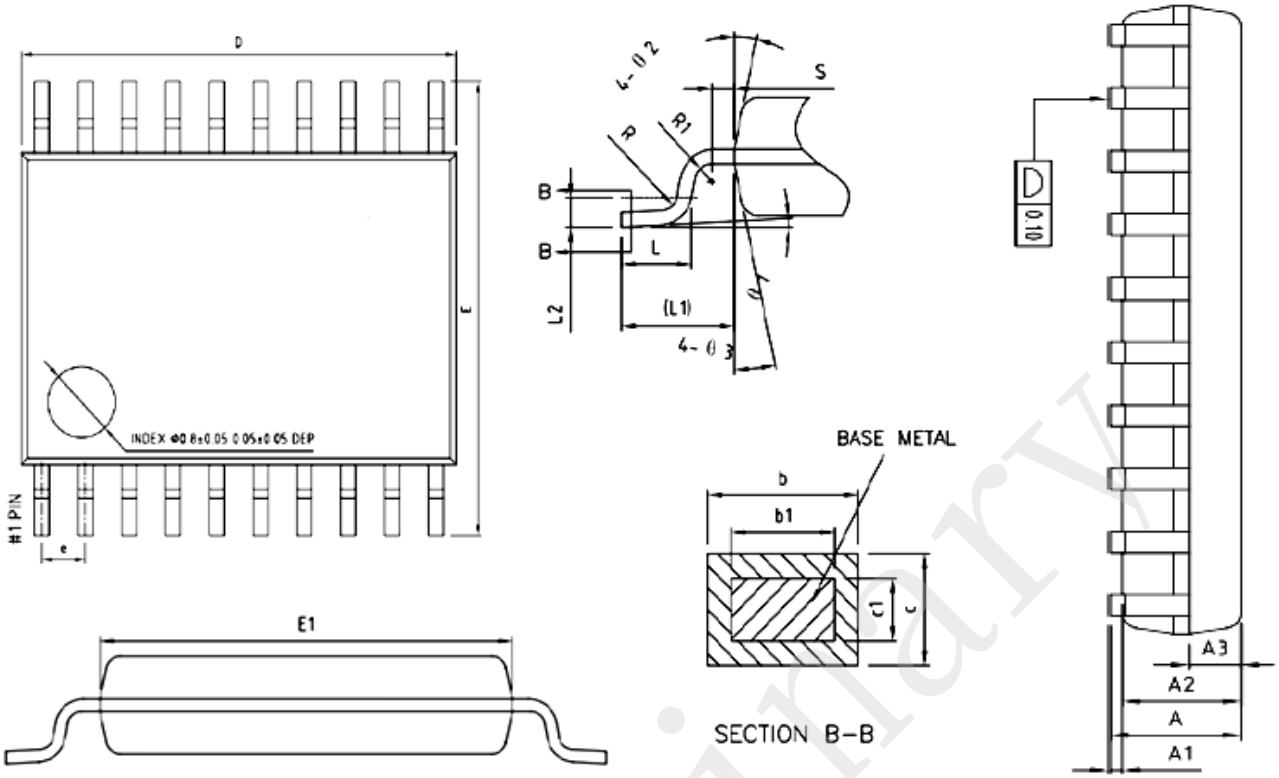
10. Transmission time matching test standards



11. Dead time test standards



12. Case outlines



	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Part Number	Package Type	Marking ID	Package Method	Quantity
FD6189T	TSSOP20	FD6189T	Tape&Reel	4000

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