Datasheet

250V Three-phase Gate Driver
FD6287T

Fortior Technology (Shenzhen) Co., Ltd

Contents

250V Three-phase Gate Driver

1 System Introduction

1.1 Overview

FD6287T is an integrated circuit (IC) that integrates three independent half-bridge gate drivers. It is specially designed for high-voltage and high-speed MOSFET driver applications, and can operate at a voltage up to +250V.

FD6287T supports VCC/VBS under-voltage lockout (UVLO) feature, protecting the power tube from operating with insufficient voltage.

FD6287T also provides cross-conduction prevention and deadtime insertion to effectively protect the power IC and prevent both MOSFETs of each half-bridge from switching on at the same time.

FD6287T has built-in input signal filtering module to avoid input noise interference.

1.2 Package

TSSOP20

1.3 Features

- Fully operational to +250V
- Power supply: 7.0V ~ 20V
- Three independent half-bridge drivers
- Output current: +1.5A/-1.8A
- 3.3V/5V logic input compatible
- VCC/VBS under-voltage lockout (UVLO)
- Cross-conduction prevention logic
- 200ns deadtime
- Built-in input filtering module
- High-low side delay matching
- High-side outputs in phase with inputs, and low-side outputs out of phase with inputs

1.4 Applications

Three-phase motor drive

1.5 Typical Application Diagram

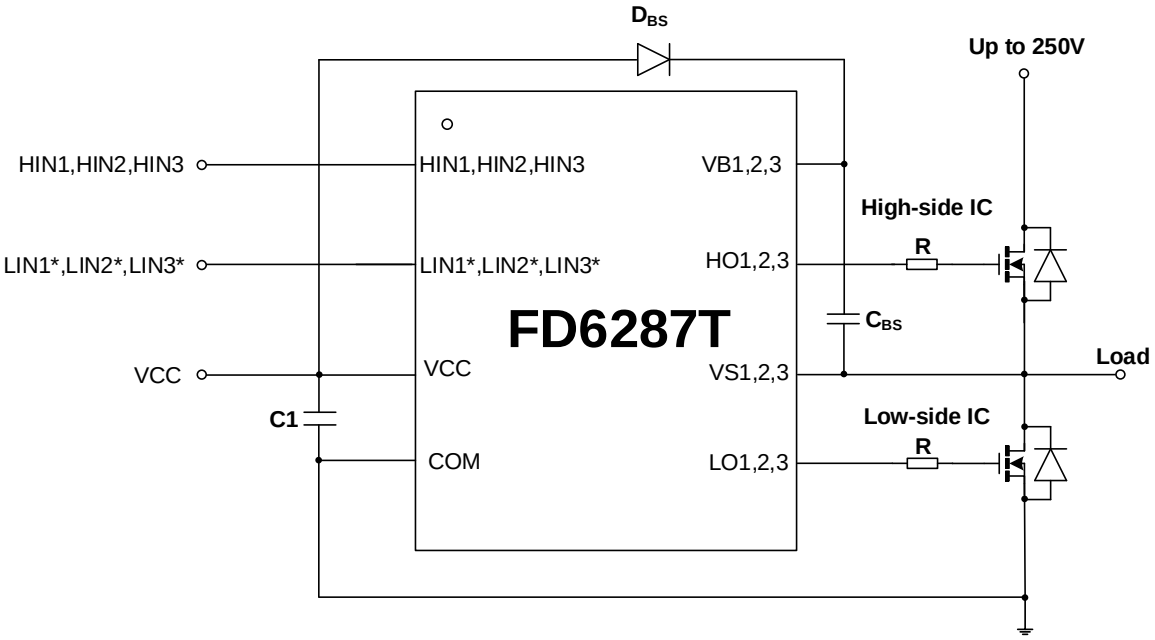


Figure 1-1 Typical Application Diagram of FD6287T

- C1: 10μF ~ 100μF power filter capacitor depending on the application circuit. It shall be mounted as close to the chip pin as possible.
- R: Gate drive resistor. The resistance depends on deadtime and the device being driven.
- D_{BS}: Bootstrap diode. Those Schottky diodes with high reverse breakdown voltage and short recovery time are preferred.
- C_{BS}: Bootstrap capacitor. 1μF ~ 50μF ceramic capacitor or tantalum capacitor is preferred. It shall be mounted as close to the chip pin as possible.

Note: The above circuit and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.6 Functional Block Diagram

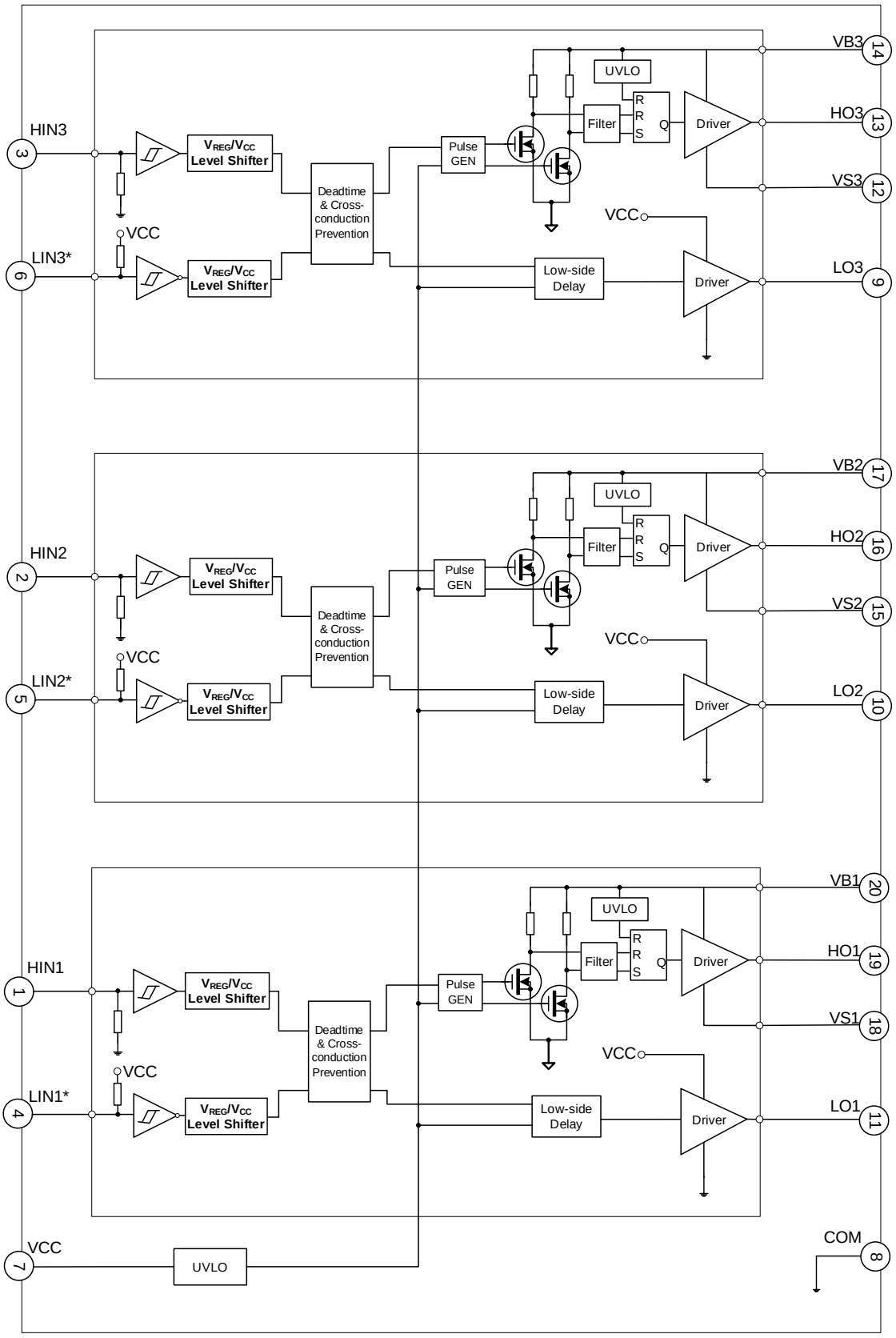


Figure 1-2 Functional Block Diagram of FD6287T

1.7 Pin Definitions

1.7.1 FD6287T TSSOP20 Pin Diagram

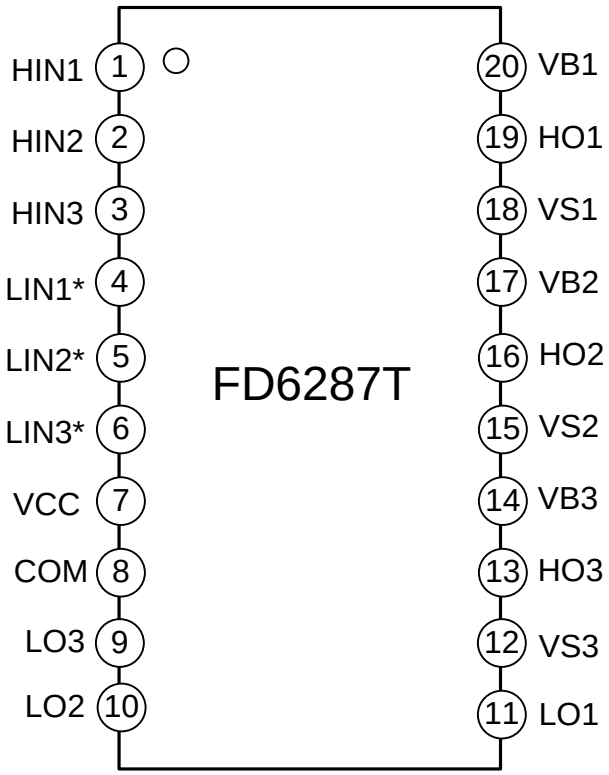


Figure 1-3 FD6287T TSSOP20 Pin Diagram

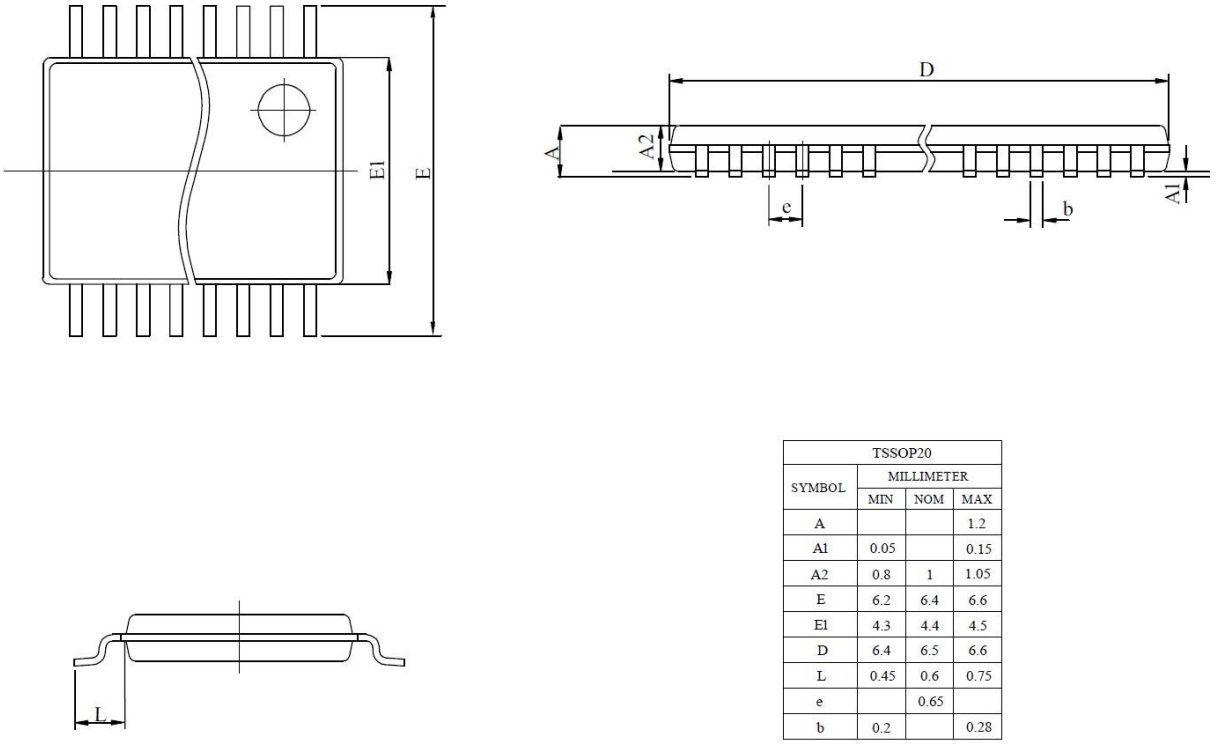
1.7.2 FD6287T TSSOP20 Pins

Table 1-1 FD6287T TSSOP20 Pin Descriptions

Pin	Name	Description
1, 2, 3	HIN1, HIN2, HIN3	High-side Input
4, 5, 6	LIN1*, LIN2*, LIN3*	Low-side Input
7	VCC	Low-side Supply Voltage
8	COM	Ground
9, 10, 11	LO3, LO2, LO1	Low-side Output
12, 15, 18	VS3, VS2, VS1	High-side Floating Offset Voltage
13, 16, 19	HO3, HO2, HO1	High-side Output
14, 17, 20	VB3, VB2, VB1	High-side Floating Absolute Voltage

2 Package Information

2.1 FD6287T TSSOP20



TSSOP20			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.2
A1	0.05		0.15
A2	0.8	1	1.05
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
D	6.4	6.5	6.6
L	0.45	0.6	0.75
e		0.65	
b	0.2		0.28

Figure 2-1 FD6287T TSSOP20 Package Drawings and Dimensions

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6287T	TSSOP20	FD6287T	Tape & Reel	3000

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter		Symbol	Range	Unit
High-side Floating Absolute Voltage		$V_{B1,2,3}$	-0.3 ~ 275	V
High-side Floating Offset Voltage		$V_{S1,2,3}$	$V_{B1,2,3}$ - 25 ~ $V_{B1,2,3}$ + 0.3	V
High-side Output Voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3 ~ $V_{B1,2,3}$ + 0.3	V
Low-side Supply Voltage		V_{CC}	-0.3 ~ 25	V
Low-side Output Voltage		$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Logic Input Voltage (HIN, LIN*)		V_{IN}	-0.3 ~ V_{CC} + 0.3	V
Slew Rate of Offset Voltage		dV_S/dt	≤ 50	V/ns
Power Dissipation @ T_A ≤ 25C°	TSSOP20	P_D	≤ 1.25	W
Junction-to-ambient Thermal Resistance	TSSOP20	R_{thJA}	≤ 100	℃/W
Junction Temperature		T_j	≤ 150	℃
Storage Temperature		T_{stg}	-55 ~ 150	℃

Notes:

- In any case, power dissipation shall not exceed P_D.
- The chip may get damaged if it operates at voltages exceeding those listed above.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

(All voltages are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ + 7	$V_{S1,2,3}$ + 20	V
Static High-side Floating Offset Voltage	$V_{S1,2,3}$	COM - 2[1]	250	V
Dynamic High-side Floating Offset Voltage	$V_{S1,2,3}$	-10[2]	250	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side Supply Voltage	V_{CC}	7	20	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic Input Voltage (HIN, LIN*)	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	℃

Notes:

[1] HO works normally when $V_{S1,2,3}$ ranges between (COM-2V) and 250V, and keeps its logical state when $V_{S1,2,3}$ ranges between (COM-2V) and (COM-V_{BS}).

[2] HO works normally when $V_{S1,2,3}$ is at (COM - 50V) with 50ns negative transient voltage.

[3] Exposure to recommended operating conditions for extended periods may affect device reliability. It is NOT recommended to use your device in conditions that go beyond the above stress ratings.

3.3 Electrical Characteristics

Table 3-3 Electrical Characteristics

(T_A = 25℃, VCC = $V_{BS1,2,3}$ = 15V and $V_{S1,2,3}$ = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 250V	-	0.1	5.0	μA
V_{BS} Quiescent Current	I_{QBS}	V_{IN} = 0V or 5V	-	180	270	μA
V_{BS} Dynamic Current	I_{PBS}	$f_{HIN1,2,3}$ = 20kHz	-	180	270	μA
V_{CC} Quiescent Current	I_{QCC}	V_{IN} = 0V or 5V	-	330	500	μA
V_{CC} Dynamic Current	I_{PCC}	$f_{LIN1,2,3}$ = 20kHz	-	330	500	μA
Input HIN/LIN*						
LIN* High-level Input Bias Current	I_{LIN+}	V_{LIN} = 0V	-	20	40	μA
LIN* Low-level Input Bias Current	I_{LIN-}	V_{LIN} = 5V	-	-	2	μA
HIN High-level Input Bias Current	I_{HIN+}	V_{HIN} = 5V	-	20	40	μA
HIN Low-level Input Bias Current	I_{HIN-}	V_{HIN} = 0V	-	-	2	μA
Input Pull-down Resistance	R_{IN}		200	260	320	KΩ
High-side Output Voltage	V_{OH}	I_O = 100mA	-	0.6	0.9	V
Low-side Output Voltage	V_{OL}	I_O = 100mA	-	0.3	0.45	V
High-level Output Short-circuit Pulsed Current	I_{OH}	V_O = 0V, V_{IN} = 5V, PWD ≤ 10μs	1.1	1.5	1.9	A
Low-level Output Short-circuit Pulsed Current	I_{OL}	V_O = 15V, V_{IN} = 0V, PWD ≤ 10μs	1.3	1.8	2.3	A
V_S Static Negative Voltage	V_{SN}		-	-6.0	-	V
UVLO						
V_{CC} UVLO Lockout Voltage	V_{CCUV+}		5.8	6.4	7.0	V
V_{CC} UVLO Release Voltage	V_{CCUV-}		5.4	6.0	6.6	V
V_{CC} UVLO Hysteresis Voltage	V_{CCUVH}		0.3	0.4	-	V
V_{BS} UVLO Lockout Voltage	V_{BSUV+}		5.8	6.4	7.0	V
V_{BS} UVLO Release Voltage	V_{BSUV-}		5.4	6.0	6.6	V
V_{BS} UVLO Hysteresis Voltage	V_{BSUVH}		0.3	0.4	-	V
High-side/Low-side Output						
High-level Input Threshold Voltage	V_{IH}		2.7	-	-	V
Low-level Input Threshold Voltage	V_{IL}		-	-	0.8	V
Time Parameters						
Turn-on Propagation Delay	t_{on}		-	300	450	ns

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-off Propagation Delay	t_{off}		-	100	160	ns
Output Rise Time	t_r	C_L = 1000pF	-	12	-	ns
Output Fall Time	t_f	C_L = 1000pF	-	12	-	ns
High-low Side Delay Matching	MT		-	-	50	ns
Deadtime	DT		100	200	300	ns

4 Propagation Delay Test Standards

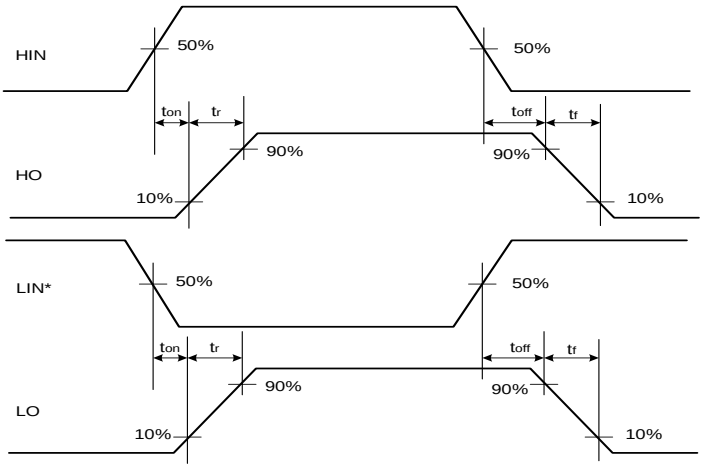


Figure 4-1 Propagation Delay Test Standards

5 Propagation Delay Matching Test Standards

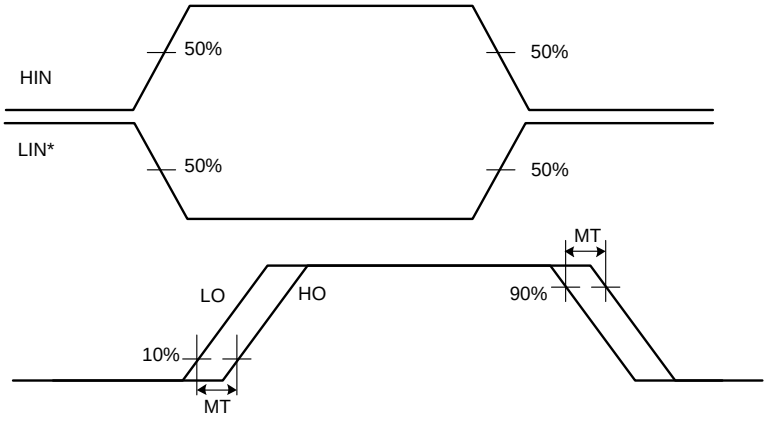


Figure 5-1 Propagation Delay Matching Test Standards

6 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs from damage when high-side and low-side input signals are interfered. The figure below shows how the protection circuit works.

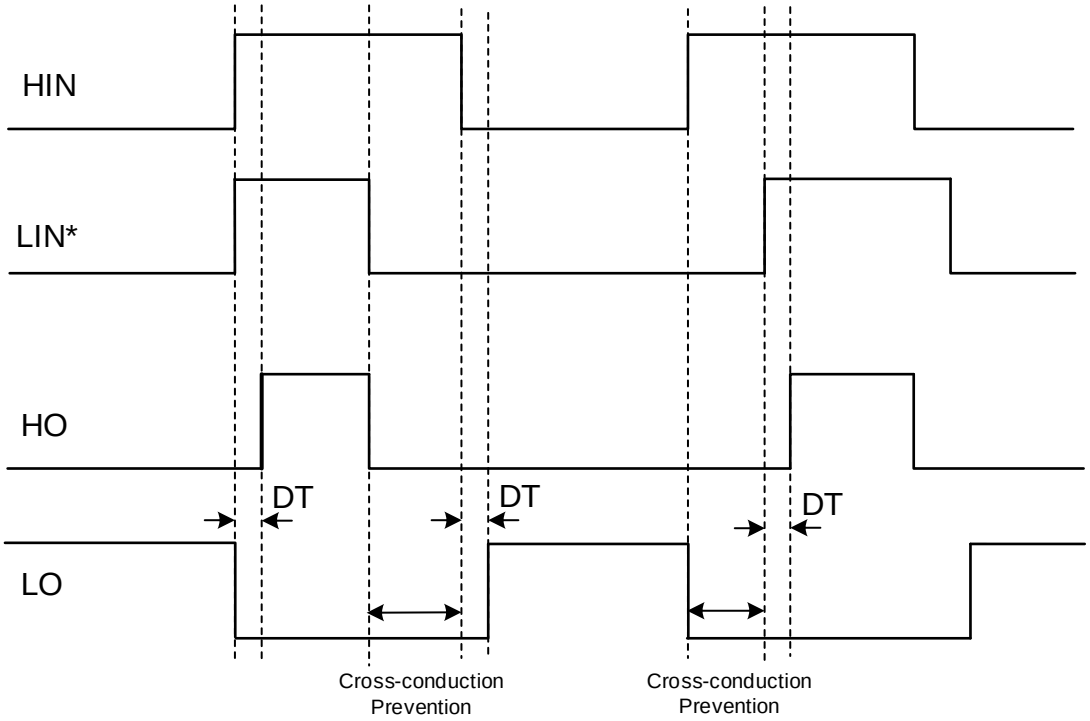


Figure 6-1 Schematic Diagram of Cross-conduction Prevention

7 Deadtime

The chip is designed with dedicated deadtime protection circuit. Both the high-side and low-side outputs are set to LOW during the deadtime. This feature prevents both MOSFETs of each half-bridge from switching on at the same time. The following figure shows timing relationship between deadtime, input signal and driver output signal.

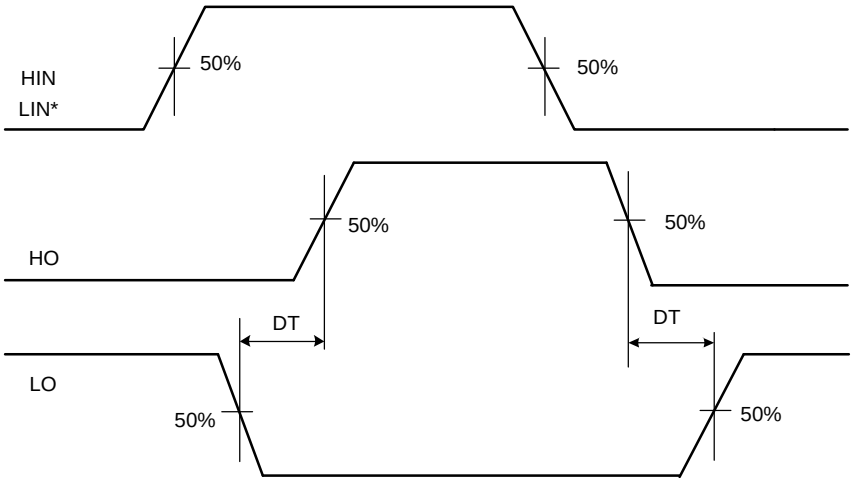


Figure 7-1 Schematic Diagram of Deadtime

8 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release, translated from Chinses version 1.0	2024/03/01	Eric Deng

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