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DATASHEET

FD6288Q1

250V Three-phase Gate Driver

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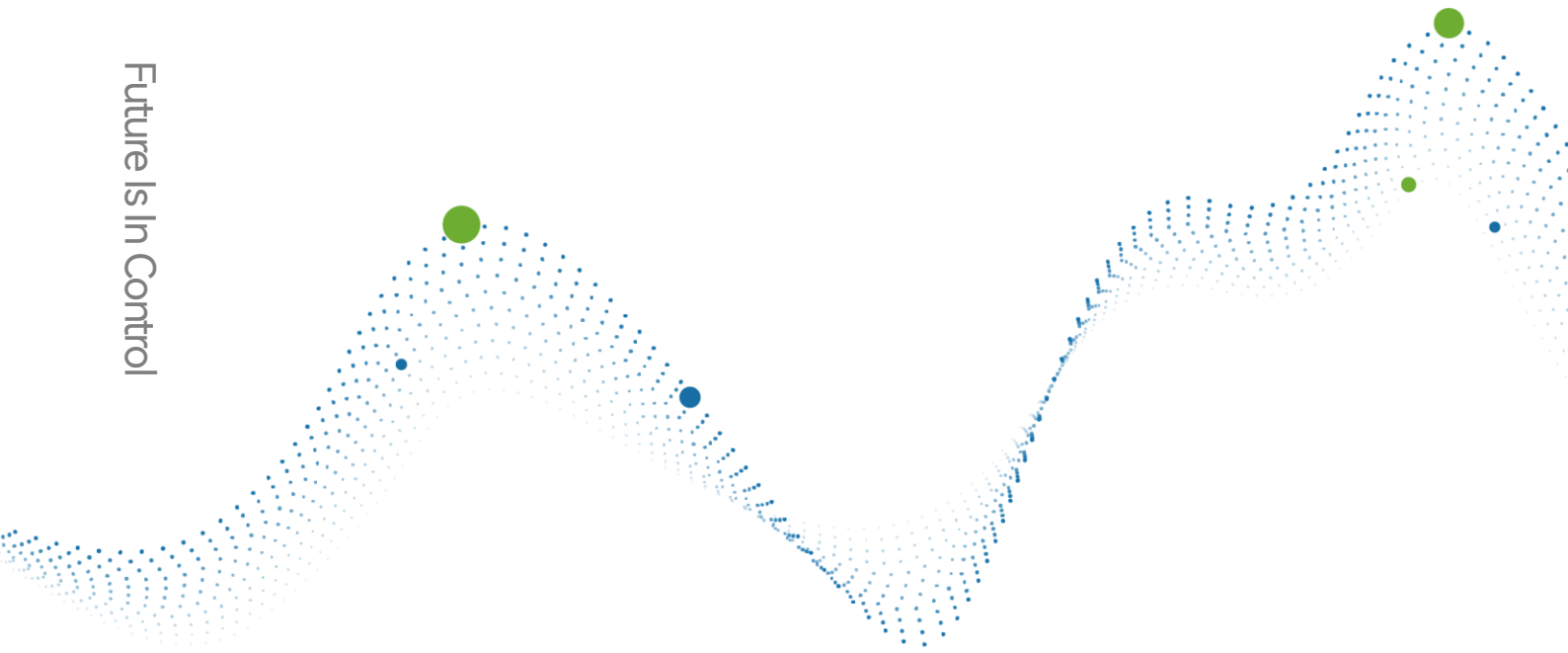

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FD6288Q1 250V Three-phase Gate Driver

1 System Introduction

1.1 Overview

FD6288Q1 is a triple half-bridge gate driver that drives 3 high-side and 3 low-side N-channel MOSFETs. It is suitable for high-voltage and high-speed MOSFET driver applications, and can operate at a voltage up to +250V.

FD6288Q1 supports VCC/VBS under-voltage lockout (UVLO) feature, protecting the power transistor from operating with insufficient voltage.

FD6288Q1 also provides shoot-through protection and deadtime to effectively protect the power IC and prevent both MOSFETs of each half-bridge from switching on at the same time.

FD6288Q1 has built-in input signal filtering module to avoid input noise interference.

1.2 Applications

Automotive electronics, refrigerators

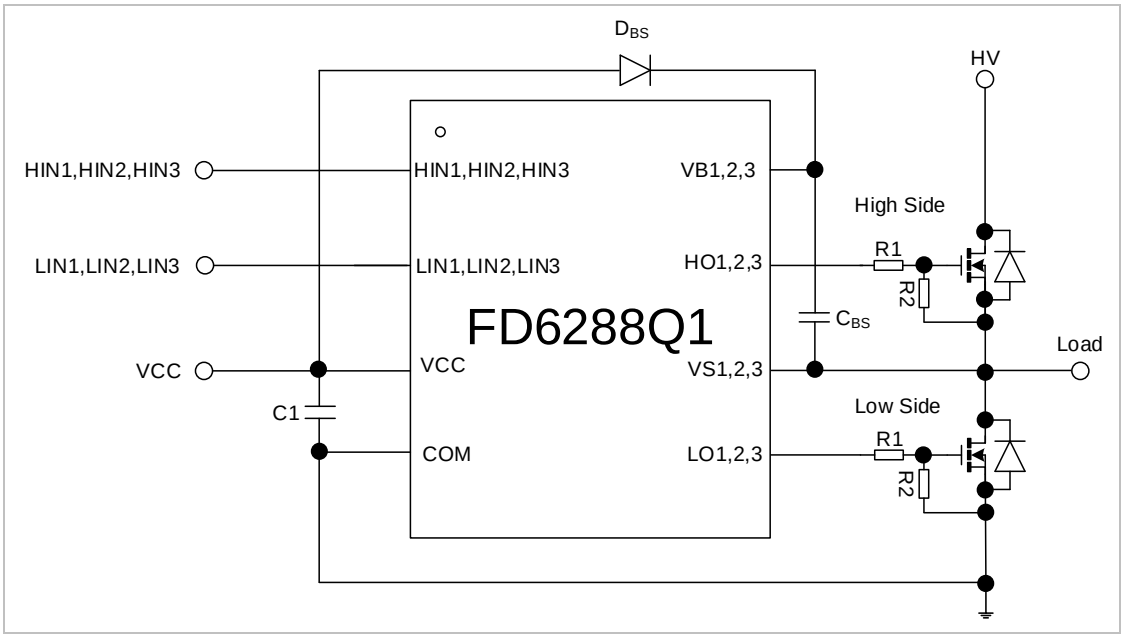
Figure 1-1 FD6288Q1

1.3 Features

- Fully operational to +250V
- Power supply: 5.0V ~ 20V
- Three independent half-bridge drivers
- Output current: +1.5A/-1.8A
- Compatible with 3.3V/5V logic input
- VCC/VBS UVLO
- Shoot-through protection
- 200ns deadtime
- Built-in input filtering module
- High-low side channels matching
- Outputs in phase with inputs

1.4 Typical Application Diagram

Figure 1-2 Typical Application Diagram



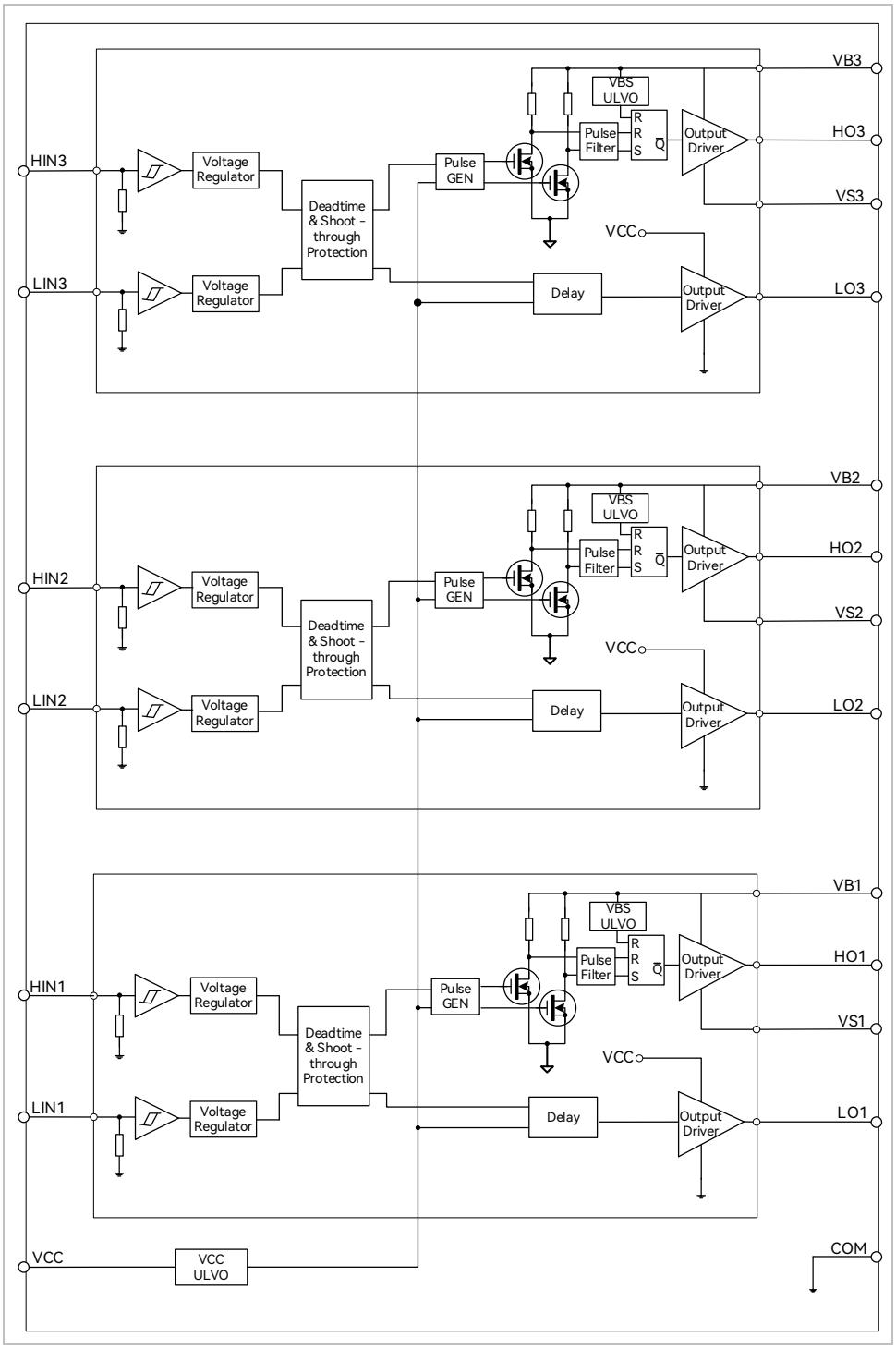
- C1: 10μF power filter capacitor. It shall be mounted as close to the chip pin as possible.
- R1: Gate drive resistor. The resistance depends on deadtime and the device being driven.
- R2: MOS gate-to-source resistor.
- D_{BS}: Bootstrap diode. Those Schottky diodes with high reverse breakdown voltage and short recovery time are preferred.
- C_{BS}: Bootstrap capacitor. Ceramic capacitor or tantalum capacitor is preferred. It shall be mounted as close to the chip pin as possible.

Note:

The above circuit and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.5 Functional Block Diagram

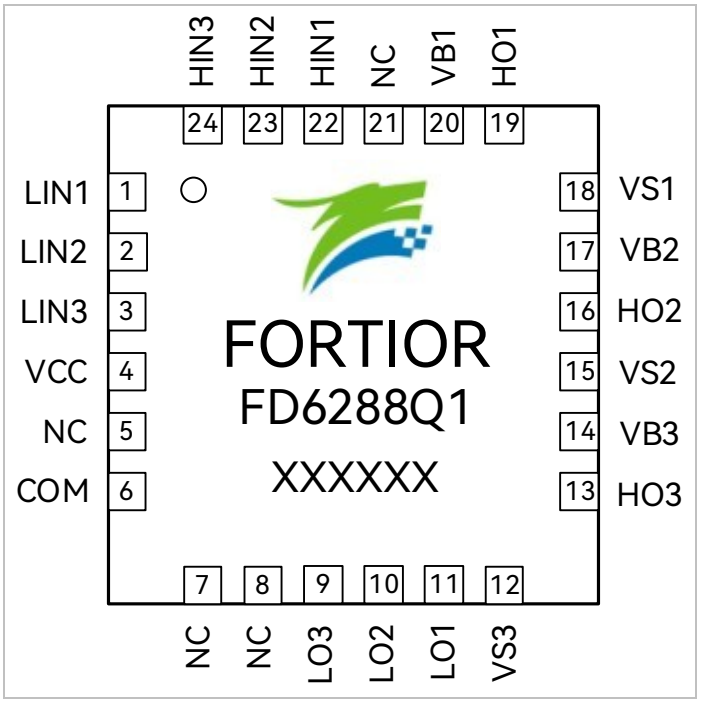
Figure 1-3 Functional Block Diagram



1.6 Pin Definitions

1.6.1 FD6288Q1 QFN24 Pinout Diagram

Figure 1-4 FD6288Q1 QFN24 Pinout Diagram



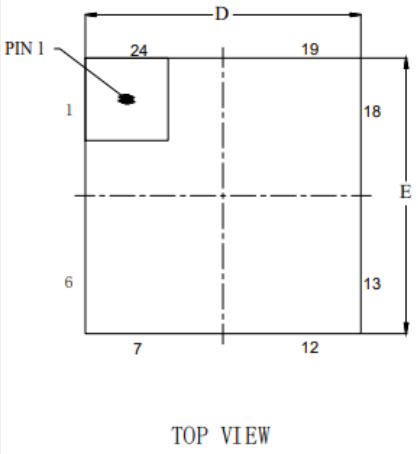
1.6.2 FD6288Q1 QFN24 Pins

Table 1-1 FD6288Q1 QFN24 Pins

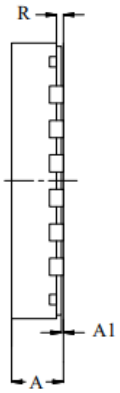
Pin	FD6288Q1 QFN24	Description
LIN1, LIN2, LIN3	1, 2, 3	Low-side input
VCC	4	Low-side power supply
NC	5, 7, 8, 21	Not connected
COM	6	Ground
LO3, LO2, LO1	9, 10, 11	Low-side output
VS3, VS2, VS1	12, 15, 18	High-side floating offset voltage
HO3, HO2, HO1	13, 16, 19	High-side output
VB3, VB2, VB1	14, 17, 20	High-side floating absolute voltage
HIN1, HIN2, HIN3	22, 23, 24	High-side input

2 Package Information

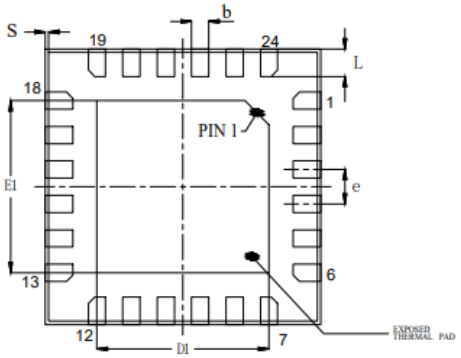
Figure 2-1 FD6288Q1 QFN24_4 X4 Package Dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW

QFN24L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
Al	0	—	0.05
D	3.9	4	4.1
E	3.9	4	4.1
Dl	2.45	2.5	2.55
El	2.45	2.5	2.55
L	0.35	0.40	0.45
e	—	0.50	—
b	0.18	0.25	0.3
S	0.001	0.05	0.09
R	0.05	0.10	0.15

3 Ordering Information

Table 3-1 Ordering Information

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6288Q1	QFN24_4 X4 (mm)	FD6288Q1	Tape & Reel	3000

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter	Symbol	Range	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	-0.3 ~ 275	V
High-side Floating Offset Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$ - 25 ~ $V_{B1,2,3}$ + 0.3	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3 ~ $V_{B1,2,3}$ + 0.3	V
Low-side Power Supply	V_{CC}	-0.3 ~ 25	V
Low-side Output Voltage	$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Logic Input Voltage (HIN, LIN)	V_{IN}	-0.3 ~ V_{CC} + 0.3	V
Slew Rate of Offset Voltage	dV_S/dt	≤ 50	V/ns
Power Dissipation @ T_A ≤ 25C°	P_D	≤ 3	W
Junction-to-ambient Thermal Resistance	R_{thJA}	≤ 42	°C/W
Junction Temperature	T_J	≤ 150	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

Caution:

- In any case, power dissipation shall not exceed P_D.
- The chip may get damaged if it operates at voltages exceeding those listed above.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions[1]

(All pins are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ + 5.0	$V_{S1,2,3}$ + 20	V
High-side Floating Offset Voltage[2]	$V_{S1,2,3}$	-4[3]	250	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side Power Supply	V_{CC}	5	20	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	VCC	V
Logic Input Voltage (HIN, LIN)	V_{IN}	0	VCC	V
Ambient Temperature	T_A	-40	125	°C

Note:

[1] Exposure to recommended operating conditions for extended periods may affect device reliability. It is NOT recommended to use your device under conditions exceeding the above stress ratings.

[2] The high-side floating offset voltage VS1, 2, 3 is tested with 12V bias voltage.

[3] HO1, 2, 3 works normally when VS1, 2, 3 ranges between -4V and 250V.

4.3 Power Supply Current

Table 4-3 Power Supply Current

(T_A = 25C, V_{BIAS} (VCC, VB1, 2, 3) = 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3} = V_{S1,2,3} = 250V$	-	0.1	5	μA
VB1, 2, 3 Dynamic Current	I_{PBS}	$f_{HIN1,2,3} = 20kHz$	-	0.11	0.27	mA
VB1, 2, 3 Quiescent Current	I_{QBS}	V_{IN} = 0V or 5V	-	0.11	0.27	mA
VCC Dynamic Current	I_{PCC}	$f_{HIN1,2,3} = f_{LIN1,2,3} = 20kHz$	-	0.22	0.5	mA
VCC Quiescent Current	I_{QCC}	V_{IN} = 0V or 5V	-	0.22	0.5	mA

4.4 Input HIN/LIN

Table 4-4 Input HIN/LIN

(T_A = 25C, V_{BIAS} (VCC, VB1, 2, 3) 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Threshold Voltage	V_{IH}		2.8	-	-	V
Low-level Input Threshold Voltage	V_{IL}		-	-	0.8	V
LIN High-level Input Bias Current	I_{LIN+}	V_{LIN} = 5V	-	25	50	μA
LIN Low-level Input Bias Current	I_{LIN-}	V_{LIN} = 0V	-	-	1	μA
HIN High-level Input Bias Current	I_{HIN+}	V_{HIN} = 5V	-	25	50	μA
HIN Low-level Input Bias Current	I_{HIN-}	V_{HIN} = 0V	-	-	1	μA

4.5 Under-voltage Lockout (UVLO)

Table 4-5 UVLO

(T_A = 25C, V_{BIAS} (VCC, VB1, 2, 3) = 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Exit Voltage	V_{CCUV+}		3.9	4.5	5.0	V
VCC UVLO Trigger Voltage	V_{CCUV-}		3.8	4.3	4.8	V
VCC UVLO Hysteresis Voltage	V_{CCUVH}		0.15	0.2	-	V
VB1, 2, 3 UVLO Exit Voltage	V_{BSUV+}		3.9	4.5	5.0	V
VB1, 2, 3 UVLO Trigger Voltage	V_{BSUV-}		3.8	4.3	4.8	V
VB1, 2, 3 UVLO Hysteresis Voltage	V_{BSUVH}		0.15	0.2	-	V

4.6 Negative Offset Voltage

Table 4-6 Negative Offset Voltage

(T_A = 25C, V_{BIAS} (VCC, VBS1, 2, 3) = 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VS1, 2, 3 Static Negative Voltage	V_{SN}		-	-5.0	-	V

4.7 High-side/Low-side Output

Table 4-7 High-side/Low-side Output

(T_A = 25C, V_{BIAS} (VCC, VBS1, 2, 3) = 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-side Output Voltage	V_{OH}	I_O = 10mA, V_{BIAS} - V_O	-	0.05	0.11	V
Low-side Output Voltage	V_{OL}	I_O = 10mA	-	0.03	0.06	V
High-level Output Short-circuit Pulsed Current	I_{OH}	V_O = 0V, V_{IN} = 5V, PW ≤ 10μs	0.7	1.15	1.6	A
Low-level Output Short-circuit Pulsed Current	I_{OL}	V_O = 15V, V_{IN} = 0V, PW ≤ 10μs	0.9	1.3	1.7	A

4.8 Time Parameters

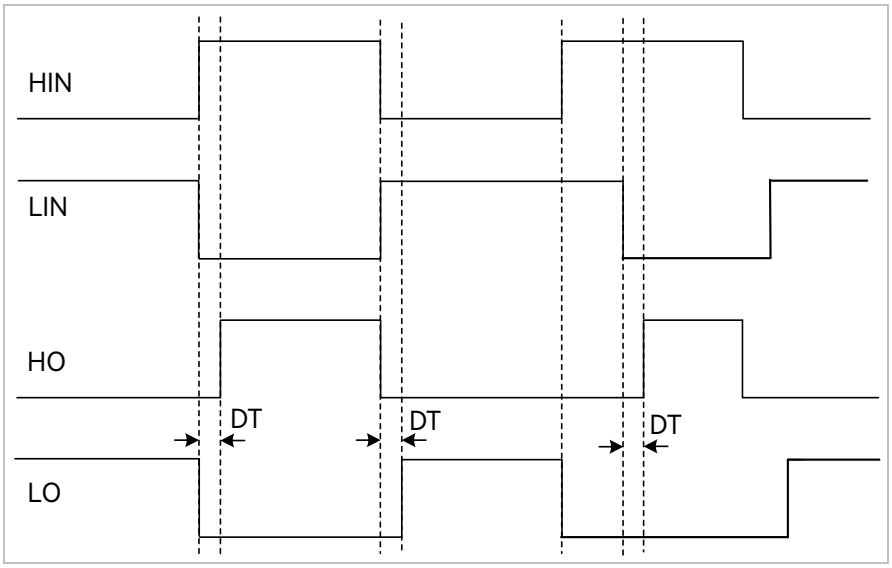
Table 4-8 Time Parameters

(T_A = 25C, V_{BIAS} (VCC, VBS1, 2, 3) = 12V and VS1, 2, 3 = COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Propagation Delay	t_{on}		-	300	450	ns
Turn-off Propagation Delay	t_{off}		-	100	160	ns
Turn-on Rise Time	t_r	C_L = 1000pF	-	12	25	ns
Turn-off Fall Time	t_f	C_L = 1000pF	-	12	25	ns
Deadtime	DT		100	200	300	ns
High-low Side Delay Matching	MT		-	-	50	ns

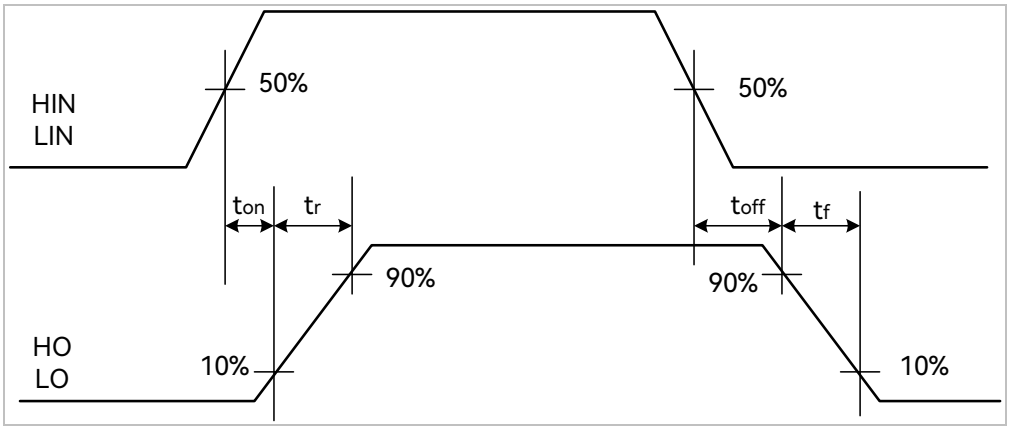
5 Logic Timing Diagram

Figure 5-1 Logic Timing Diagram



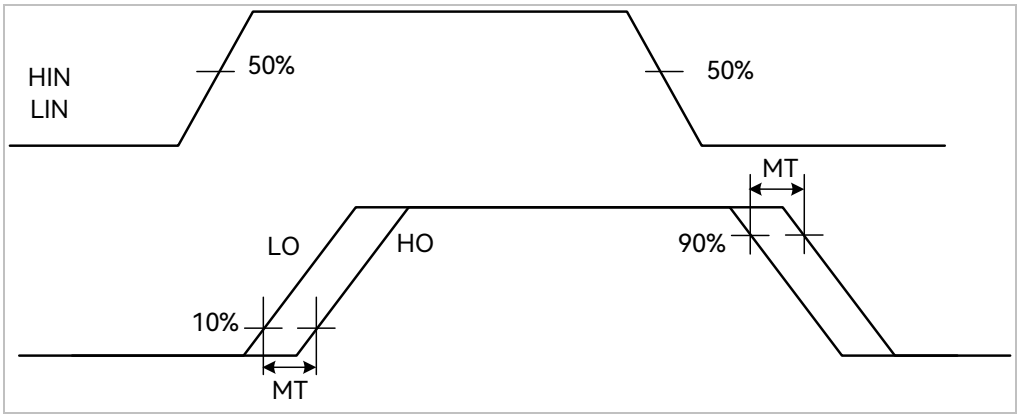
6 Propagation Delay Matching Test Standard

Figure 6-1 Propagation Delay Matching Test Standard Diagram



7 Propagation Delay Matching Test Standard

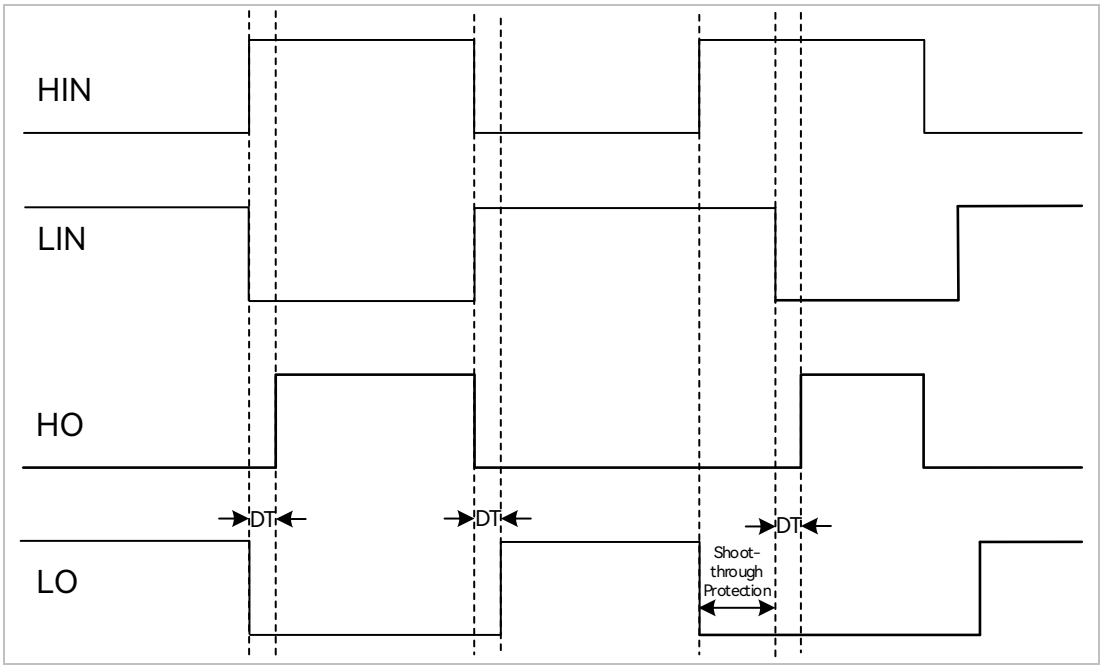
Figure 7-1 Propagation Delay Matching Test Standard Diagram



8 Shoot-through Protection

FD6288Q1 incorporates a dedicated shoot-through protection circuit. This feature safeguards the power transistor against damage from interference in the high-side and low-side input signals. The figure below shows how the protection circuit works.

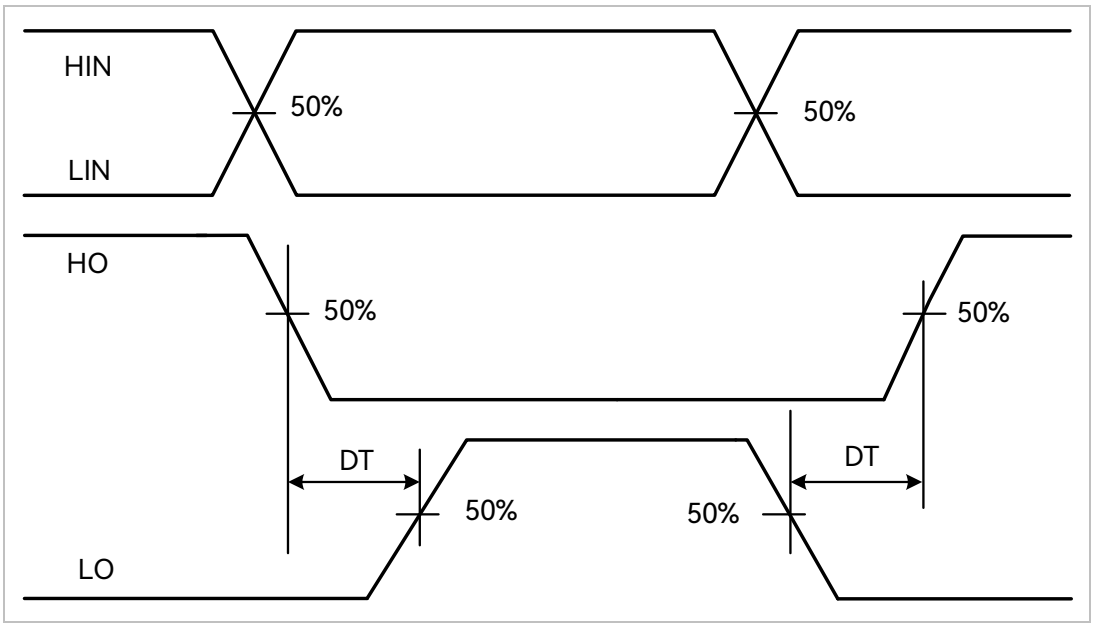
Figure 8-1 Shoot-through Protection Diagram



9 Deadtime

FD6288Q1 integrates a fixed deadtime protection circuit. During the deadtime, both high-side and low-side outputs are held low. The programmed deadtime ensures that one power transistor is turned off before the other is turned on, effectively preventing shoot-through.

Figure 9-1 Deadtime Insertion Diagram



10 Revision History

Rev.	Description	Date	Prepared By
V1.0	Initial release	2026/01/23	Lydia Zhu
V1.1	1. Modified Test Condition of VCC Dynamic Current from $f_{HIN1,\ 2,\ 3}$ = 20kHz to $f_{HIN1,\ 2,\ 3}$ = $f_{LIN1,2,3}$ = 20kHz; removed U/V/W from Parameters VB1, 2, 3 Dynamic and Quiescent Currents in section 4.3 Power Supply Current; 2. Modified Parameters VCC and VB1,2,3 UVLO Threshold Voltages to VCC and VB1,2,3 UVLO Exit Voltage; modified VCC and VB1,2,3 Release Voltages to VCC and VB1,2,3 UVLO Trigger Voltages in section 4.5 Under-voltage Lockout (UVLO).	2026/07/13	Lydia Zhu

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