Datasheet

600V Three-phase Half-bridge Gate Driver
FD6636S

Fortior Technology (Shenzhen) Co., Ltd

Contents

600V Three-phase Half-bridge Gate Driver

1 System Introduction

1.1 Overview

FD6636S is an integrated circuit (IC) that integrates three independent half-bridge gate drivers. It is specially designed for high-voltage and high-speed MOSFET/IGBT driver applications, and can operate at a voltage up to +600V.

FD6636S provides deadtime insertion and cross-conduction prevention to effectively protect power IC and prevent both MOSFETs/IGBTs of each half-bridge from switching on at the same time.

FD6636S supports VCC/VBS under-voltage lockout (UVLO) feature, protecting the power tube from operating with insufficient voltage.

FD6636S has built-in input signal filtering module to avoid input noise interference.

FD6636S integrates over-current protection circuit, which disables six-channel output when detecting under-voltage or over-current fault state.

FD6636S also supports logic input (Enable pin) to shut down six-channel output at the same time.

1.2 Package

SOP28

1.3 Features

- Fully operational to +600V
- Three independent half-bridge drivers
- Output current: +0.21A/-0.36A
- 3.3V/5V logic input compatible
- VCC/VBS under-voltage lockout (UVLO)
- High-low side channels matching
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Built-in deadtime module
- Built-in input filtering module
- Logic input (Enable pin) for shutdown
- Over-current protection circuit disables six-channel output
- Clear time configured by external settings

1.4 Applications

- Three-phase motors
- DC-AC converters

1.5 Typical Application Diagram

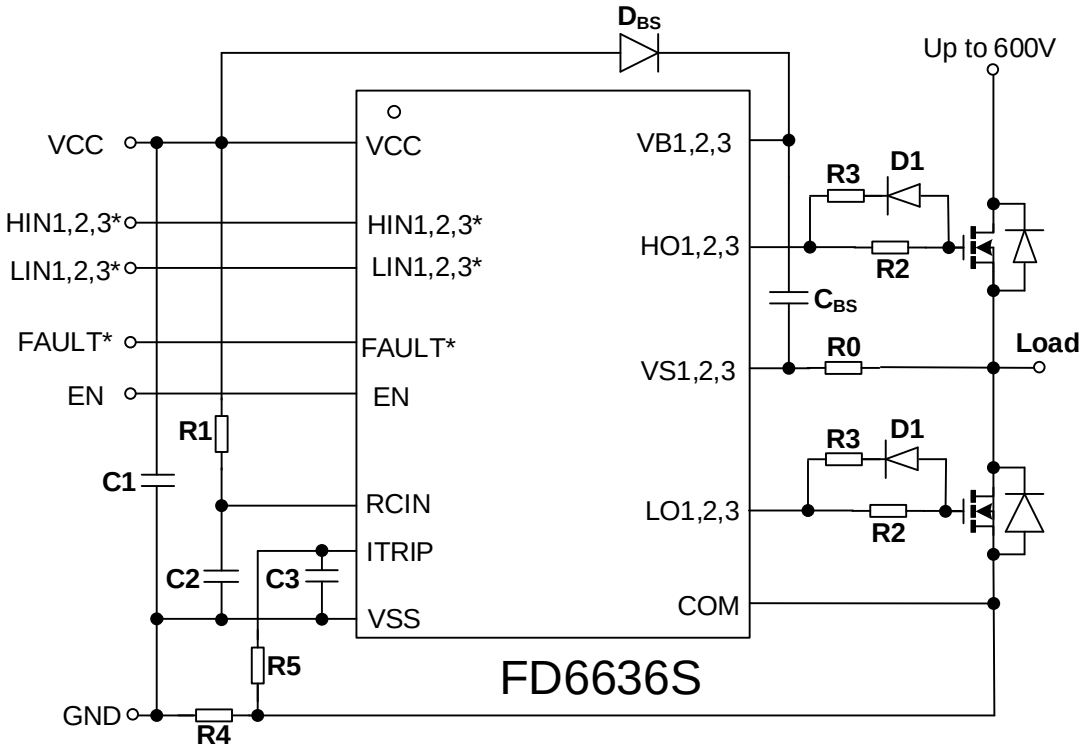


Figure 1-1 Typical Application Diagram of FD6636S

- C1: 10μF power filter capacitor is recommended. It shall be mounted as close to the chip pin as possible.
- R0: 1Ω ~ 6Ω resistor is recommended.
- R1: 2MΩ resistor is recommended.
- C2: RCIN reset capacitor. 1nF capacitor is recommended.
- C3: 10nF capacitor is recommended.
- D_{BS}: Bootstrap diode. Those with high reverse breakdown voltage (> 600V) and short recovery time are preferred.
- C_{BS}: Bootstrap capacitor. Ceramic capacitor or tantalum capacitor is preferred. The minimum capacitance is calculated as follows:

$$\boldsymbol{Cbs \geq 15 * \frac{2 * [2 * Q_g + Q_{period} + \frac{I_{bs(static)}}{f} + \frac{I_{bs(leak)}}{f}]}{Vcc - V_F - V_{ds(L)}}}$$

Where,

- Q_g refers to high-side gate charge.
- Q_{period} refers to the charge required by level switching circuit in each cycle, which is about 10nC.
- $I_{bs(static)}$ refers to static current of the high-side drive circuit.

- $I_{bs(leak)}$ refers to leak current of bootstrap capacitor.
- *f* refers to operating frequency of the circuit.
- V_{CC} refers to low-side supply voltage.
- V_F refers to forward voltage drop of bootstrap diode.
- $V_{ds(L)}$ refers to low-side voltage drop.

Note: The above circuit and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.6 Functional Block Diagram

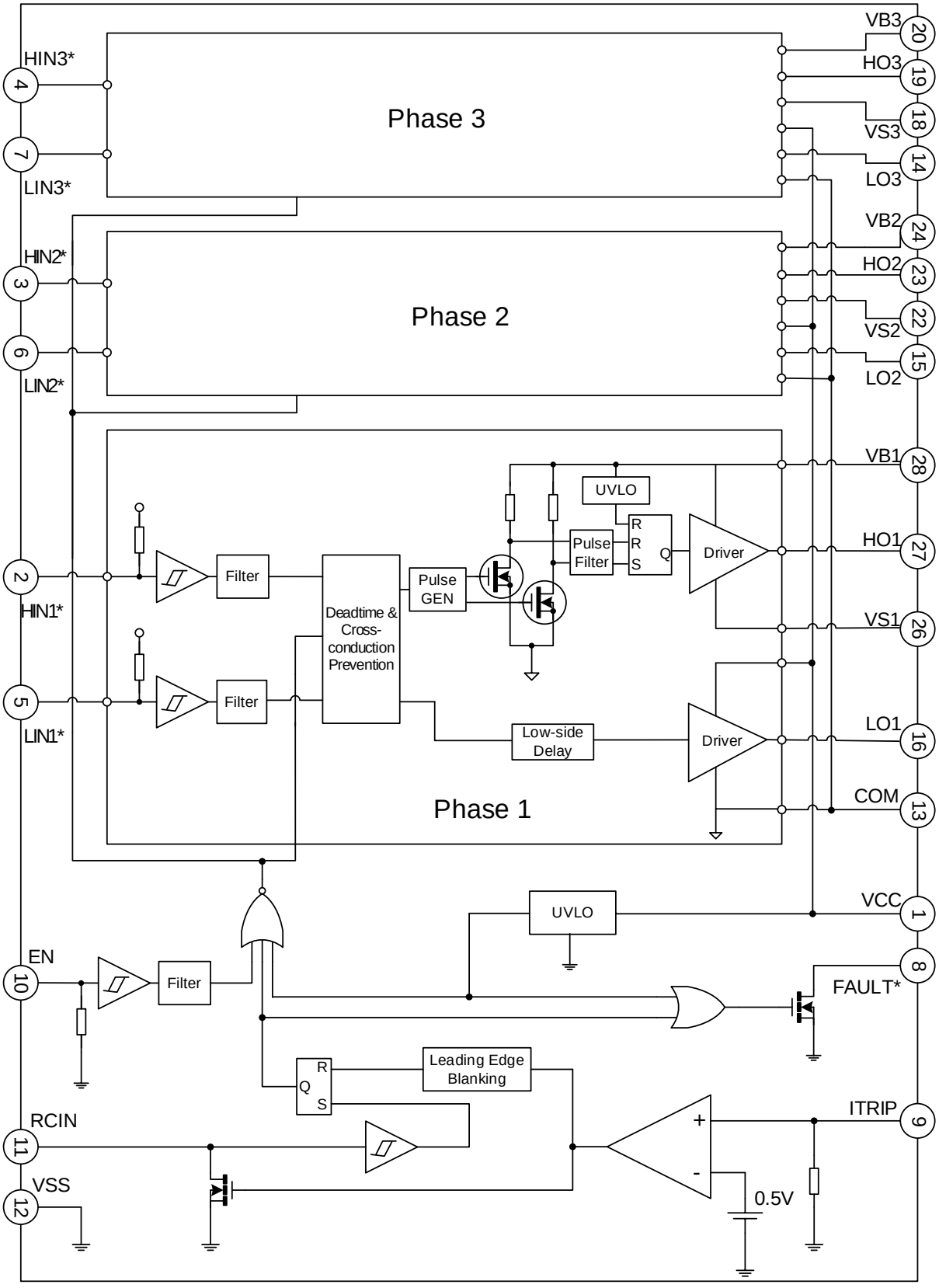


Figure 1-2 Functional Block Diagram of FD6636S

1.7 Pin Definitions

1.7.1 FD6636S SOP28 Pinout Diagram

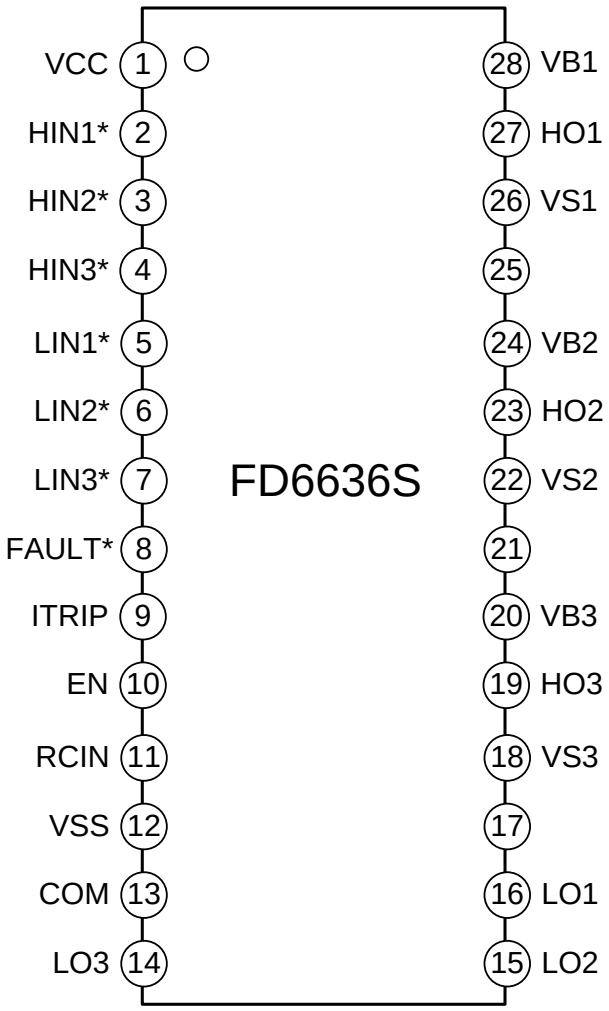


Figure 1-3 FD6636S SOP28 Pinout Diagram

1.7.2 FD6636S SOP28 Pins

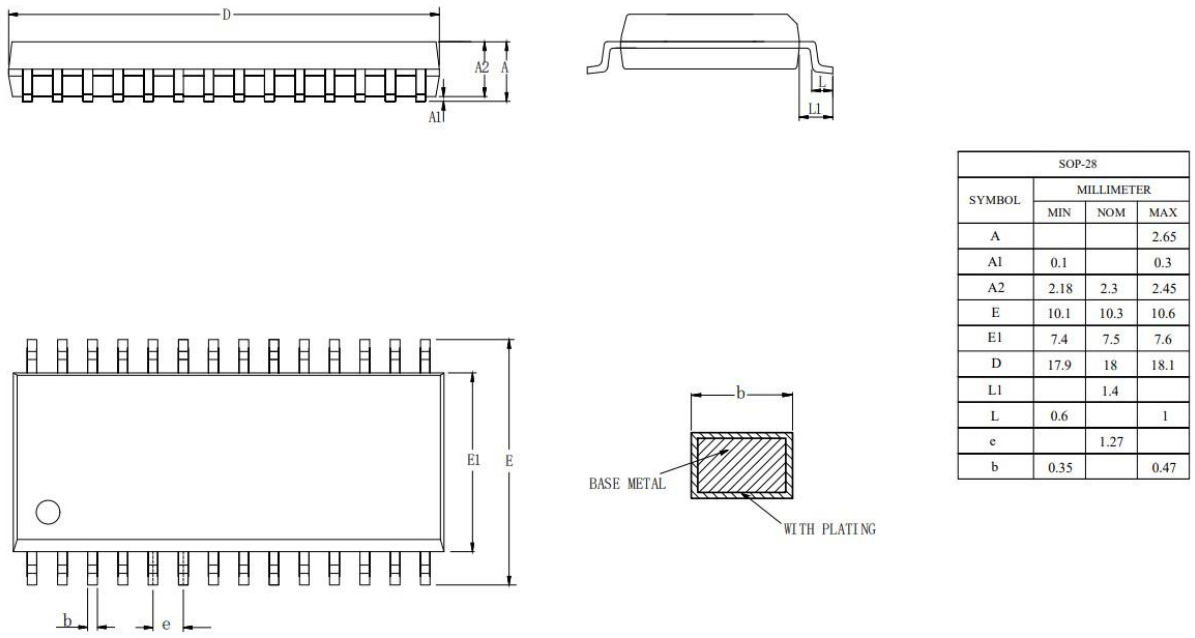
Table 1-1 FD6636S SOP28 Pin Descriptions

Pin	Name	Description
1	VCC	Low-side supply voltage
2, 3, 4	HIN1*, HIN2*, HIN3*	High-side input (negative logic)
5, 6, 7	LIN1*, LIN2*, LIN3*	Low-side input (negative logic)
8	FAULT*	Fault indication of over-current or low-side UVLO (negative logic)
9	ITRIP	Logic input for over-current protection
10	EN	Enable pin
11	RCIN	External RC input to define fault clear delay
12	VSS	Logic ground
13	COM	Common pin for low-side gate drive

Pin	Name	Description
14, 15, 16	LO3, LO2, LO1	Low-side output
18, 22, 26	VS3, VS2, VS1	High-side floating offset voltage
19, 23, 27	HO3, HO2, HO1	High-side output
20, 24, 28	VB3, VB2, VB1	High-side floating absolute voltage
17, 21, 25	NC	Not connected

2 Package Information

2.1 FD6636S SOP28



SOP-28			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			2.65
A1	0.1		0.3
A2	2.18	2.3	2.45
E	10.1	10.3	10.6
E1	7.4	7.5	7.6
D	17.9	18	18.1
L1		1.4	
L	0.6		1
e		1.27	
b	0.35		0.47

Figure 2-1 FD6636S SOP28 Package Drawings and Dimensions

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6636S	SOP28	FD6636S	Tape & Reel	1000
FD6636S	SOP28	FD6636S	Tube	25

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter		Symbol	Range	Unit
High-side Floating Absolute Voltage		$V_{B1,2,3}$	-0.3 ~ 625	V
High-side Floating Offset Voltage		$V_{S1,2,3}$	$V_{B1,2,3}$ - 25 ~ $V_{B1,2,3}$ + 0.3	V
High-side Output Voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3 ~ $V_{B1,2,3}$ + 0.3	V
Low-side Supply Voltage		V_{CC}	-0.3 ~ 25	V
Logic Ground		V_{SS}	V_{CC} - 25 ~ V_{CC} + 0.3	V
Low-side Output Voltage		$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Logic Input Voltage (HIN*, LIN*, ITRIP, EN)		V_{IN}	V_{SS} - 0.3 ~ V_{CC} + 0.3	V
RCIN Input Voltage		V_{RCIN}	V_{SS} - 0.3 ~ V_{CC} + 0.3	V
FAULT* Output Voltage		V_{FLT}	V_{SS} - 0.3 ~ V_{CC} + 0.3	V
Slew Rate of Offset Voltage		dV_S/dt	≤ 50	V/ns
Power Dissipation @ T_A ≤ 25C°	SOP28	P_D	≤ 1.8	W
Junction-to-ambient Thermal Resistance	SOP28	R_{thJA}	≤ 70	℃/W
Junction Temperature		T_j	≤ 150	℃
Storage Temperature		T_{stg}	-55 ~ 150	℃

Notes:

- In any case, power dissipation shall not exceed P_D.
- The chip may get damaged if it operates at voltages exceeding those listed above.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

(All voltages are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
High-side Floating Offset Voltage	$V_{S1,2,3}$	See Note [2]	600	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side Supply Voltage	V_{CC}	10	20	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic Ground	V_{SS}	-5	5	V
FAULT* Output Voltage	V_{FLT}	V_{SS}	V_{CC}	V
RCIN Input Voltage	V_{RCIN}	V_{SS}	V_{CC}	V
ITRIP Input Voltage	V_{ITRIP}	V_{SS}	V_{CC}	V
Logic Input Voltage (HIN*, LIN*, EN)	V_{IN}	V_{SS}	V_{CC}	V
Ambient Temperature	T_A	-40	125	℃

Notes:

[1] Exposure to recommended operating conditions for extended periods may affect device reliability. It is NOT recommended to use your device in conditions that go beyond the above stress ratings.

[2] HO works normally when $V_{S1,2,3}$ ranges between (COM - 2V) and 250V. and keeps its logical state when $V_{S1,2,3}$ ranges between (COM-2V) and (COM-V_{BS}).

3.3 Electrical Characteristics

Table 3-3 Electrical Characteristics

(T_A = 25℃, V_{CC} = $V_{BS1,2,3}$ = 15V, C_L = 1000pF and $V_{S1,2,3}$ = COM = V_{SS} unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Power Supply						
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600V	-	0.1	5.0	μA
V_{BS} Quiescent Current	I_{QBS}	VIN = 0V or 5V	-	90	150	μA
V_{CC} Quiescent Current	I_{QCC}	VIN = 0V or 5V	-	0.9	1.6	μA
Input Signal						
HIN*/LIN* High-level Input Threshold Voltage	V_{IH}		2.7	-	-	V
HIN*/LIN* Low-level Input Threshold Voltage	V_{IL}		-	-	0.8	V
EN High-level Input Threshold Voltage	$V_{EN,TH+}$		2.7	-	-	V
EN Low-level Input Threshold Voltage	$V_{EN,TH-}$		-	-	0.8	V
ITRIP Over-current Protection Detection Voltage	$V_{IT,TH+}$		0.38	0.46	0.54	V
ITRIP Over-current Protection Hysteresis Voltage	$V_{IT,HYS}$		-	0.08	-	V
RCIN Detection Voltage	$V_{RCIN,TH+}$		-	8	-	V
RCIN Hysteresis Voltage	$V_{RCIN,HYS+}$		-	3	-	V
LIN* High-level Input Bias Current	I_{LIN*+}	V_{LIN*} = 5V	-	70	100	μA
LIN* Low-level Input Bias Current	I_{LIN*-}	V_{LIN*} = 0V	-	110	150	μA
HIN* High-level Input Bias Current	I_{HIN*+}	V_{HIN*} = 5V	-	70	100	μA
HIN* Low-level Input Bias Current	I_{HIN*-}	V_{HIN*} = 0V	-	110	150	μA
ITRIP High-level Input Bias Current	I_{ITRIP+}	V_{ITRIP} = 5V	-	300	500	μA
ITRIP Low-level Input Bias Current	I_{ITRIP-}	V_{ITRIP} = 0V	-	0	1	μA
EN High-level Input Bias Current	I_{EN+}	V_{EN} = 5V	-	300	500	μA
EN Low-level Input Bias Current	I_{EN-}	V_{EN} = 0V	-	0	1	μA
RCIN Input Bias Current	I_{RCIN}	VRCIN = 0V or 15V	-	0	1	μA
UVLO						
V_{CC} UVLO Lockout Voltage	V_{CCUV+}		8.1	9.0	9.9	V

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
V_{CC} UVLO Release Voltage	V_{CCUV-}		7.5	8.4	9.3	V
V_{CC} UVLO Hysteresis Voltage	V_{CCUVH}		0.4	0.6	-	V
V_{BS} UVLO Lockout Voltage	V_{BSUV+}		8.0	8.9	9.8	V
V_{BS} UVLO Release Voltage	V_{BSUV-}		7.3	8.1	8.9	V
V_{BS} UVLO Hysteresis Voltage	V_{BSUVH}		0.5	0.8	-	V
Output						
HO High-level Output Voltage	V_{OH-H}	I_O = 20mA	VBS-1.0	VBS-0.6	-	V
HO Low-level Output Voltage	V_{OL-H}	I_O = 20mA	-	0.2	0.35	V
HO High-level Output Voltage	V_{OH-L}	I_O = 20mA	VCC-1.0	VCC-0.6	-	V
LO Low-level Output Voltage	V_{OL-L}	I_O = 20mA	-	0.2	0.35	V
High-level Output Short-circuit Pulsed Current	I_{OH}	V_O = 0V, V_{IN}=0V, PWD ≤ 10μs	0.14	0.21	-	A
Low-level Output Short-circuit Pulsed Current	I_{OL}	V_O = 15V, V_{IN} =5V, PWD ≤ 10μs	0.24	0.36	-	A
RCIN Drain-source On-state Resistance	R_{ON_RCIN}		-	50	75	Ω
FAULT* Drain-source On-state Resistance	R_{ON_FAULT*}		-	50	75	Ω
V_S Static Negative Voltage	V_{SN}		-	-6.5	-5.0	V
Time Parameters						
Turn-on Propagation Delay	t_{on}	C_L = 1000pF	200	300	400	ns
Turn-off Propagation Delay	t_{off}	C_L = 1000pF	200	300	400	ns
Output Rise Time	t_r	C_L = 1000pF	-	110	180	ns
Output Fall Time	t_f	C_L = 1000pF	-	45	70	ns
Enable Low to Output Shutdown Propagation Delay	t_{EN}	V_{EN} = 0V	200	300	400	ns
ITRIP Over-current Protection Propagation Delay	t_{ITRIP}	V_{ITRIP} = 5V	275	400	525	ns
ITRIP Leading Edge Blanking Time	t_{bl}	V_{IN} = 0V, V_{ITRIP} = 5V	100	150	-	ns
ITRIP to FAULT* Propagation Delay	t_{FLT}	V_{IN} = 0V, V_{ITRIP} = 5V	200	325	450	ns
Input Filter Time (HIN*, LIN*)	t_{FILIN*}	V_{IN} = 0V	100	200	-	ns
RCIN Fault Clear Time (R = 2M, C = 1nF)	t_{FLTCLR}	V_{IN} = 0V, V_{ITRIP} = 0V	1.3	1.65	2.0	ms
Deadtime	DT	VIN = 0V or 5V	200	300	400	ns
High-low Side Delay Matching	MT		-	40	75	ns
Three Channel Turn-on and Turn-off Delay Matching	MDT		-	25	70	ns

Parameter	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Input and Output Pulse Widths Matching	PM	|pwin-pwout|	-	40	75	ns

Note: For high-side PWM input, HIN1, 2, 3* input pulse width must be ≥ 1μs.

4 Truth Table of Signals

Table 4-1 Truth Table of Signals

V_{CC}	V_{BS}	ITRIP	EN	FAULT	LO	HO
< V_{CCUV-}	X	X	X	0[1]	0	0
15V	< V_{BSUV-}	0V	5V	High Impedance	LIN1,2,3	0
15V	15V	0V	5V	High Impedance	LIN1,2,3	HIN1,2,3
15V	15V	> $V_{IT,TH+}$	5V	0[2]	0	0
15V	15V	0V	0V	High Impedance	0	0

Notes:

[1] When V_{CC} > V_{CCUV-}, the output is not locked and FAULT output changes from 0 to high impedance.

[2] FAULT output changes to high impedance when ITRIP < $V_{IT,TH-}$ and RCIN voltage is larger than 8V (@VCC = 15V).

5 Logic Timing Diagram

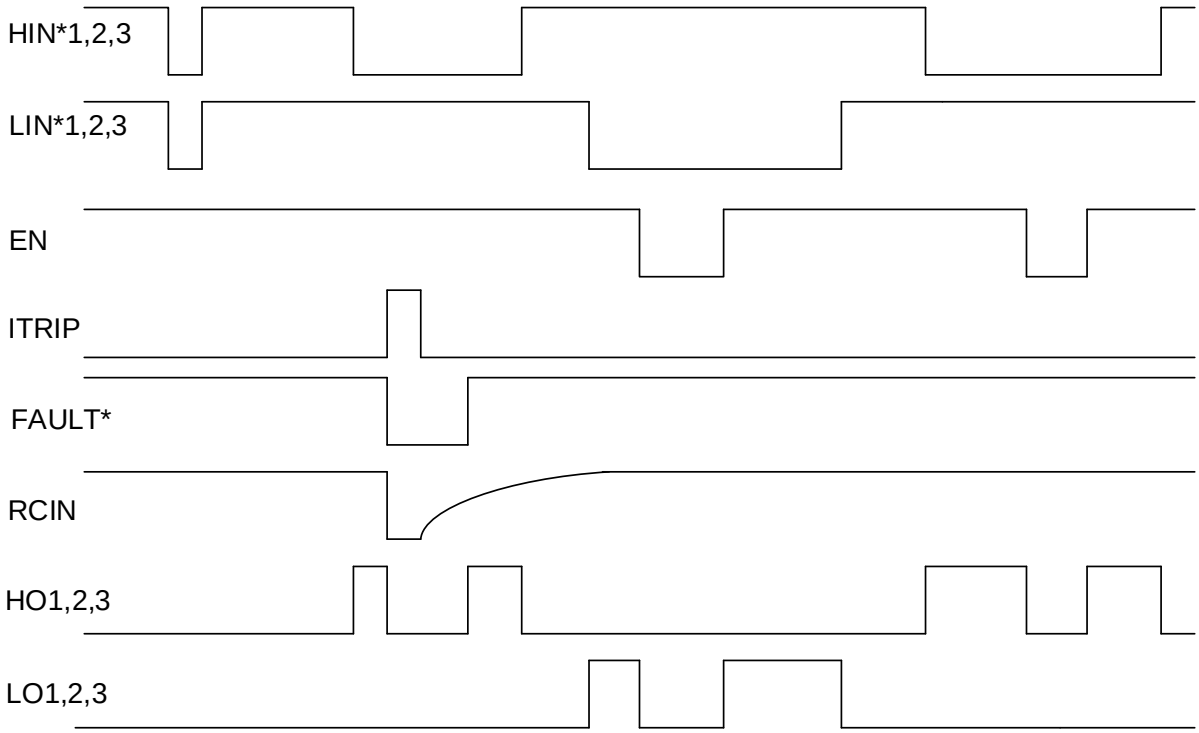


Figure 5-1 Logic Timing Diagram

6 Switching Time Waveform Definitions

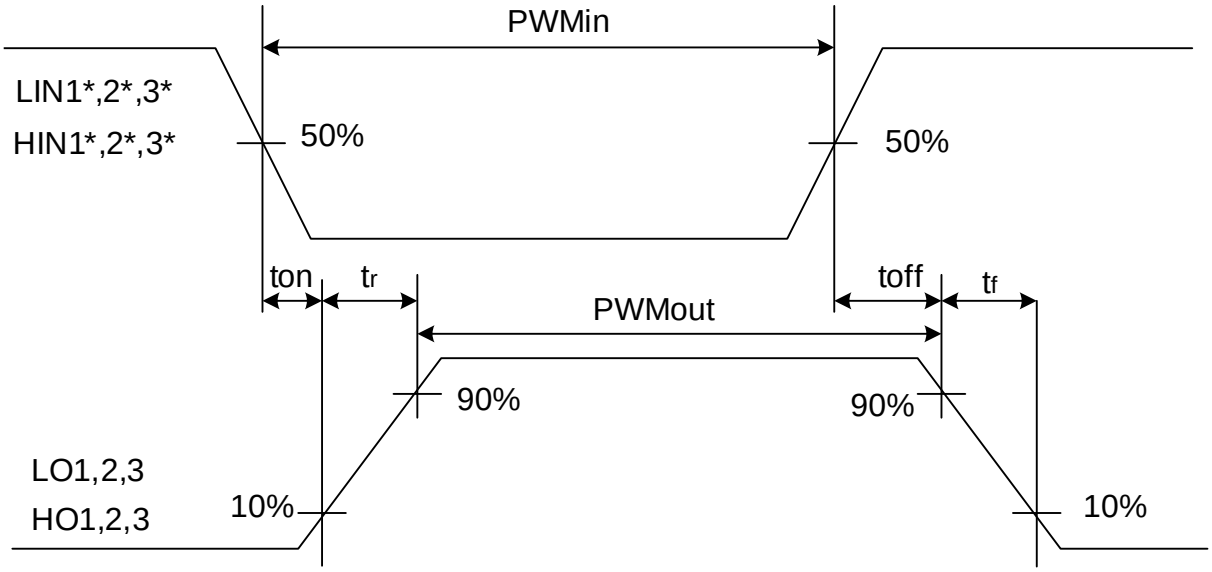


Figure 6-1 Switching Time Waveform Definitions

7 Enable Low to Output Shutdown Waveform Definitions

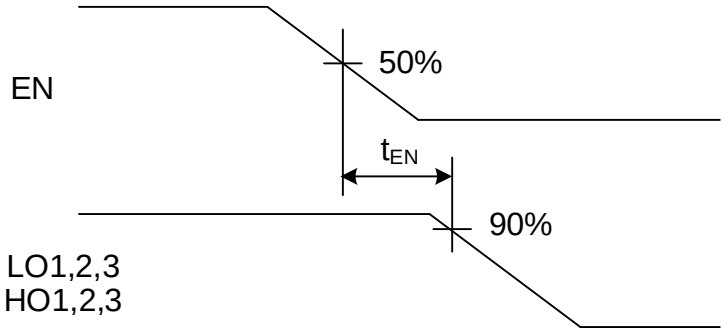


Figure 7-1 Enable Low to Output Shutdown Waveform Definitions

8 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs from damage when high-side and low-side input signals are interfered. The figure below shows how the protection circuit works.

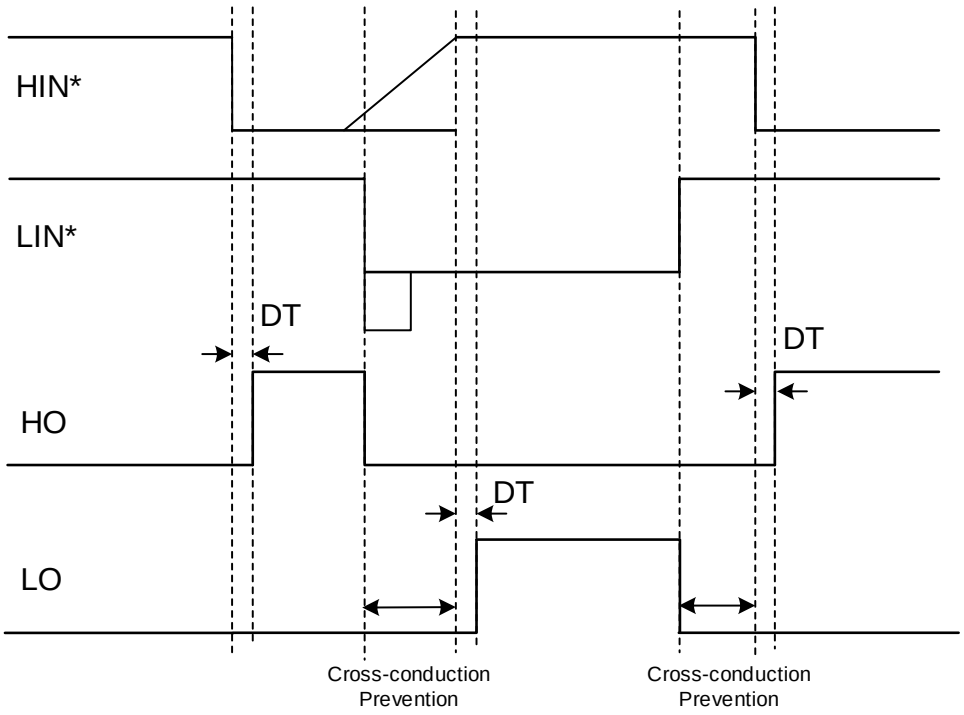


Figure 8-1 Schematic Diagram of Cross-conduction Prevention

9 Deadtime Waveform Definitions

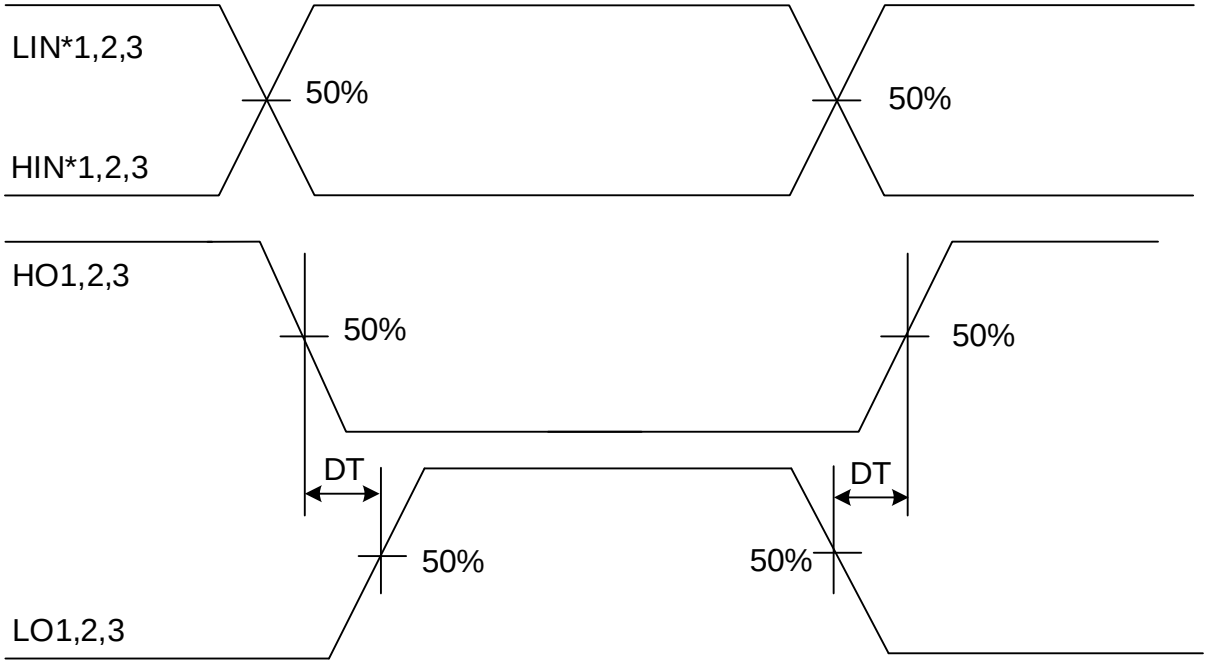


Figure 9-1 Deadtime Waveform Definitions

10 ITRIP/RCIN Waveform Definitions

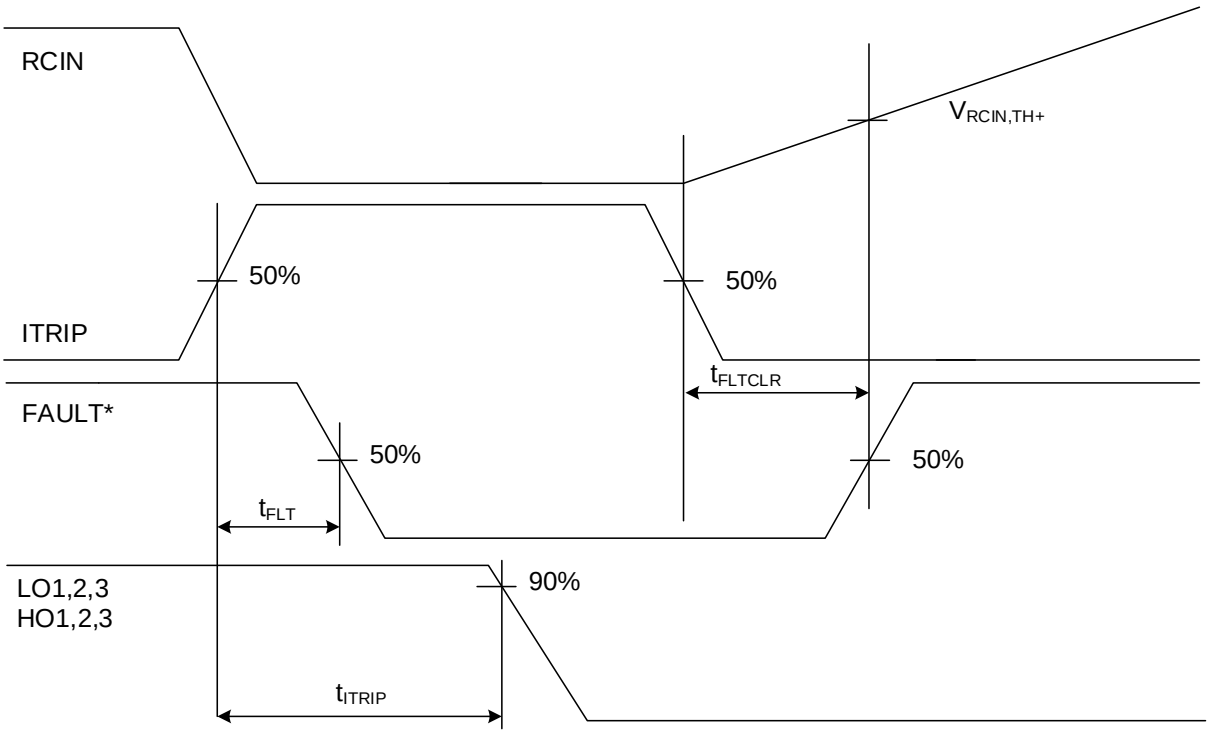


Figure 10-1 ITRIP/RCIN Waveform Definitions

11 Input Filter Waveform

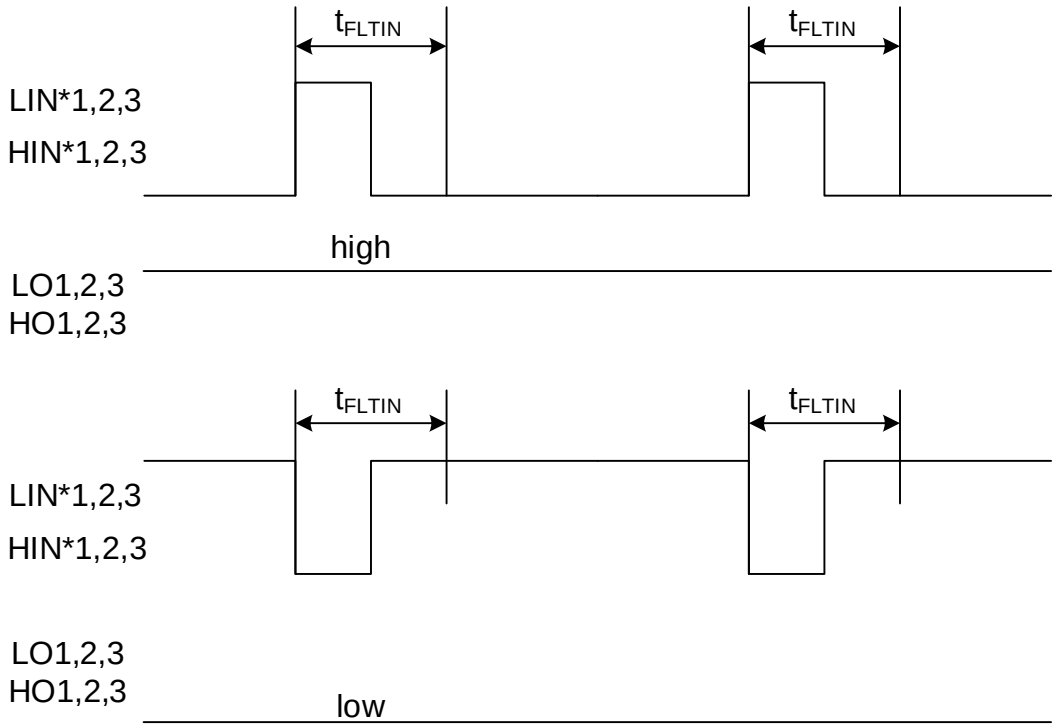


Figure 11-1 Input Filter Waveform

12 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release, translated from Chinese version 1.0	2024/03/05	Eric Deng

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