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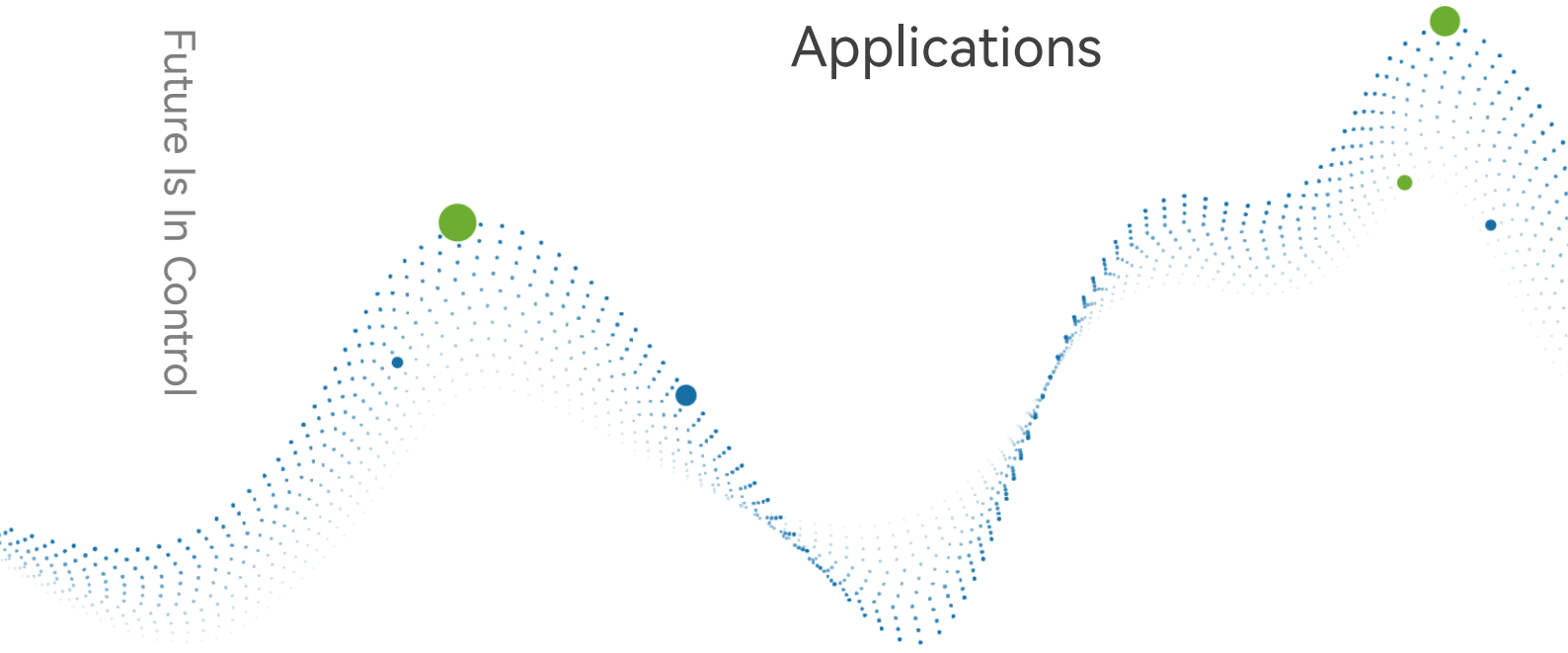
FE0551AAS

Three-Phase IPM for High-voltage Applications



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Contents

1 System Introduction

1.1 Overview

FE0551AAS is a three-phase intelligent power module (IPM) especially designed for high-voltage applications. It integrates three high-voltage half-bridge gate driver chips and six power fast-recovery MOS. Due to a high level of integration, few peripheral components are required during application. FE0551AAS contains VCC/VBS under-voltage lockout (UVLO) circuitry, protecting the power tube from operating with insufficient voltage. Also, the power module provides separate negative DC terminals for each phase to measure the current independently. Moreover, FE0551AAS supports cross-conduction prevention and deadtime insertion to effectively protect the power IC. With strong insulation, high thermal conductivity and low electromagnetic interference, the power module is housed in a compact package and suitable for built-in motors and other space constraint applications.

1.2 Applications

Ceiling fans

FE0551AAS

1.3 Features

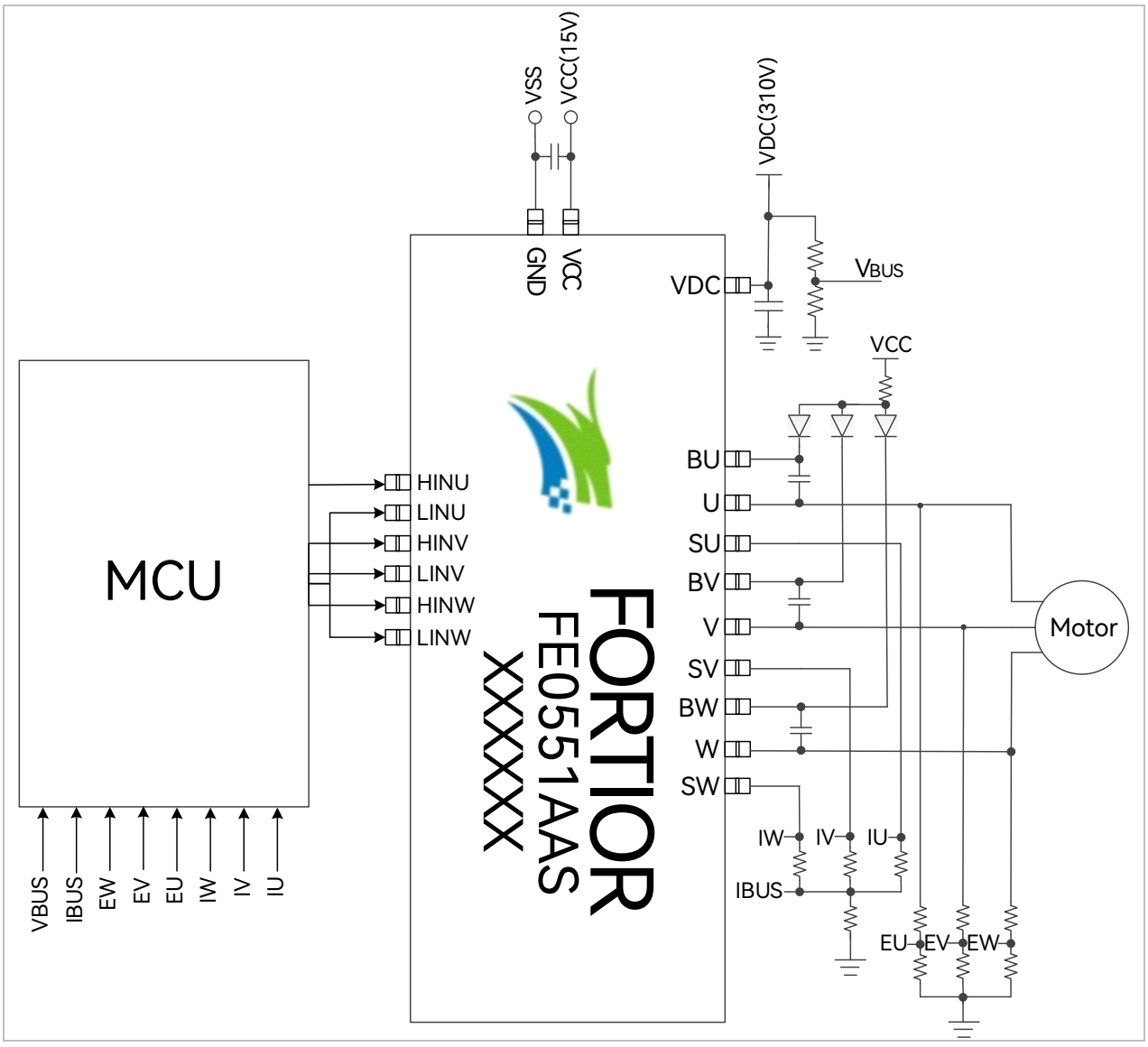
- 500V 5A fast-recovery power MOS
- VCC range: 13V ~ 20V
- Integrated control, drive and high-voltage power MOS
- Support high-level signals, and compatible with 3.3V/5V MCU
- Low electromagnetic interference design
- Support UVLO feature
- Built-in deadtime module
- Withstand isolation voltage: 2000V
- RoHS compliant

1.4 Key Parameters

- MOSFET Output Voltage: 500V
- Single MOS Drive Current (DC): ± 5A (Max.)
- Single MOS Drive Current (Pulse): ± 20A (Max.)
- MOSFET DC Output Resistance: 1.2Ω (Typ.)
- Max. Junction Temperature: +150°C
- Power Dissipation: 3.00W

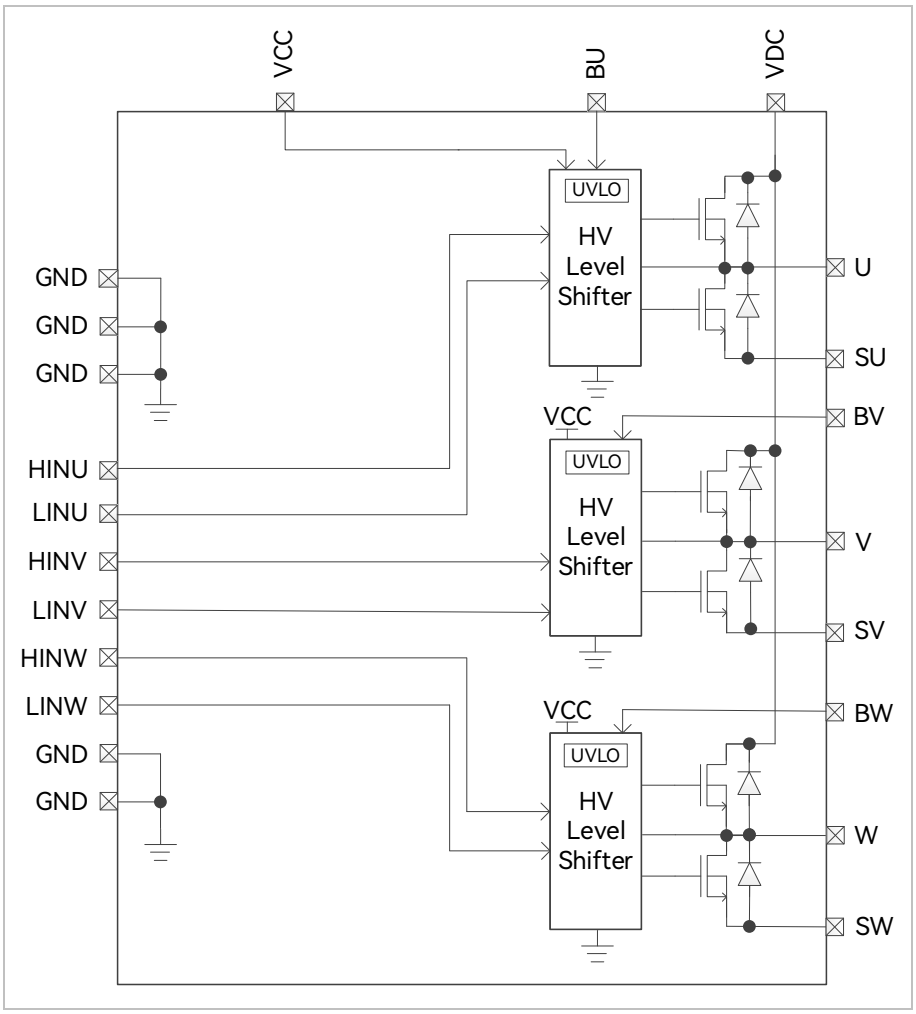
1.5 Typical Application Diagram

Figure 1-1 Typical Application Diagram of FE0551AAS



1.6 Functional Block Diagram

Figure 1-2 Functional Block Diagram of FE0551AAS



1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.1 FE0551AAS SSOP A54-38 Pinout Diagram

Figure 1-3 FE0551AAS SSOP A54-38 Pinout Diagram

1.7.2 FE0551AAS SSOP A54-38 Pins

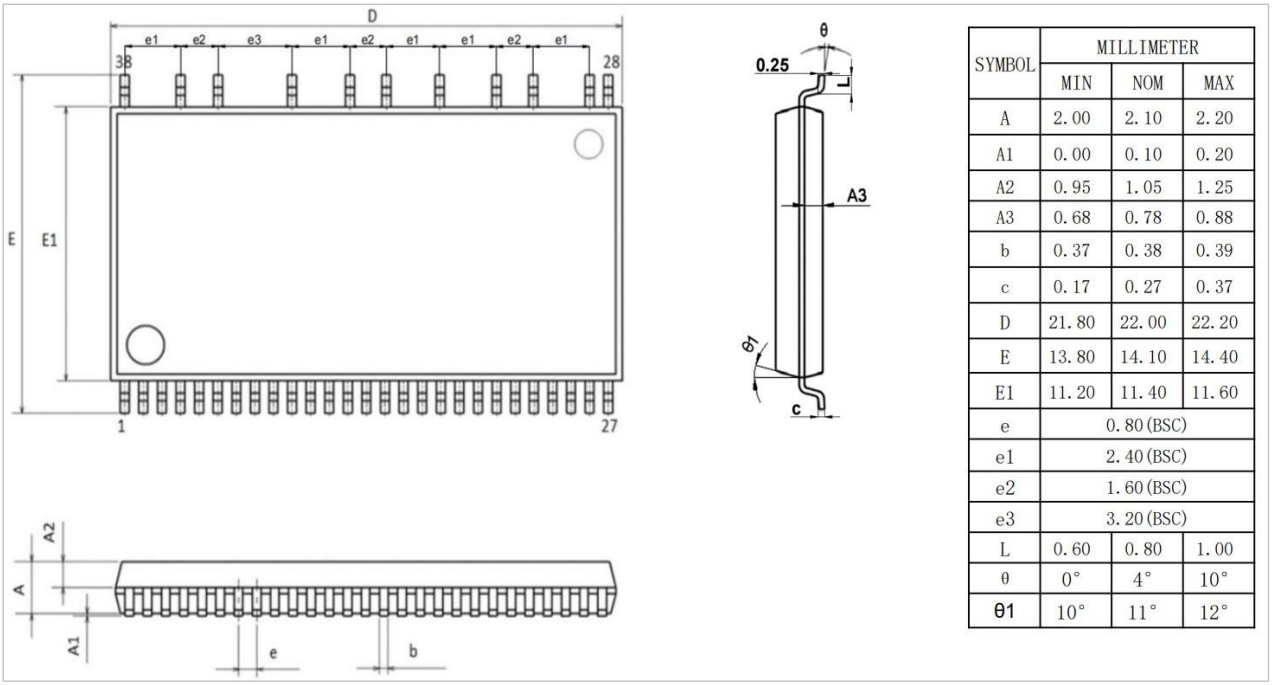
Table 1-1 FE0551AAS SSOP A54-38 Pin Descriptions

Pin	FE0551AAS SSOP A54-38	IO Type	Description
VCC	1	P	Power input
GND	2	P	Ground
GND	3	P	Ground
GND	4	P	Ground
NC	5	-	Not connected
LINW	6	DI	Low-side signal input for phase W
NC	7	-	Not connected
HINW	8	DI	High-side signal input for phase W
NC	9	-	Not connected
NC	10	-	Not connected
NC	11	-	Not connected
NC	12	-	Not connected
LINV	13	DI	Low-side signal input for phase V
NC	14	-	Not connected
HINV	15	DI	High-side signal input for phase V
NC	16	-	Not connected
NC	17	-	Not connected
NC	18	-	Not connected
NC	19	-	Not connected
NC	20	-	Not connected
LINU	21	DI	Low-side signal input for phase U
NC	22	-	Not connected
HINU	23	DI	High-side signal input for phase U
NC	24	-	Not connected
GND	25	P	Ground
GND	26	P	Ground
VCC	27	P	Power input
VDC	28	P	High-voltage power supply
VDC	29	P	High-voltage power supply
BU	30	P	U-phase floating power supply. The voltage floats with respect to phase U.
U	31	DO	U-phase output

Pin	FE0551AAS SSOP A54-38	IO Type	Description
SU	32	P	U-phase ground
BV	33	P	V-phase floating power supply. The voltage floats with respect to phase V.
V	34	DO	V-phase output
SV	35	P	V-phase ground
BW	36	P	W-phase floating power supply. The voltage floats with respect to phase W.
W	37	DO	W-phase output
SW	38	P	W-phase ground

2 Package Information

Figure 2-1 FE0551AAS SSOP A54-38 Package Drawings and Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.00	2.10	2.20
A1	0.00	0.10	0.20
A2	0.95	1.05	1.25
A3	0.68	0.78	0.88
b	0.37	0.38	0.39
c	0.17	0.27	0.37
D	21.80	22.00	22.20
E	13.80	14.10	14.40
E1	11.20	11.40	11.60
e	0.80 (BSC)		
e1	2.40 (BSC)		
e2	1.60 (BSC)		
e3	3.20 (BSC)		
L	0.60	0.80	1.00
θ	0°	4°	10°
θ1	10°	11°	12°

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Rdson(High Side+Low Side) (Ω)	Single MOS Continuous Drain Current (A)	Control Function	Protection Features		Operating Junction Temperature T_J (°C)	Lead-free	Package	Package Method	Quantity
				Driver Type	Under-voltage Protection Features	Cross-conduction Prevention					
FE0551AAS	13 ~ 20	2.4	5	N + N	√	√	-40 ~ 150	√	SSOP A54-38	Tape & Reel	1000

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Drive Circuit					
MOSFET Drain-to-Source Voltage V_{DSS}		500	-	-	V
Continuous Drain Current $I_{DMAX(DC)}$ of Single MOS	T_C = 25℃	-	-	5[2]	A
Pulsed Drain Current $I_{DMAX(PLS)}$ of Single MOS	T_C = 25℃	-	-	20[2][3]	A
Continuous Diode Forward Current I_F	T_C = 25℃	-	-	5[2]	A
Short Circuit Withstand Time T_{SC}	V_{GS} = 15V, V_{CC} ≤ 400V, T_J ≤ 175℃			5	μs
Controller					
High-side Floating Absolute Voltage V_{BU}, V_{BV}, V_{BW}		-0.3	-	625[2]	V
High-side Floating Offset Voltage V_S		V_B - 25	-	V_B + 0.3	V
High-side Output Voltage V_{HO}		V_S - 25	-	V_B + 0.3	V
Low-side Supply Voltage V_{CC}		-0.3	-	25	V
Low-side Output Voltage V_{LO}		-0.5	-	V_{CC} + 0.3	V
Logic Input Voltage (HIN,LIN) V_{IN}		-0.5	-	V_{CC} + 0.3	V
Offset Voltage Transient dVS/dt		-	≤ 50	-	V/ns
Overall System					
Storage Temperature T_{STG}		-40	-	125	℃
Case Temperature T_C	-40℃ ≤ T_J ≤ 150℃	-30	-	125	℃
Withstand Isolation Voltage V_{ISO}	60Hz, Sine Wave, 60s, The pin is connected to the substrate	-	-	2000	Vrms
Junction Temperature T_J[4]		-40	-	150	℃

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Power Dissipation P_d		-	-	3[5]	W

Caution:

[1] Stress values greater than Table 4-1 Absolute Maximum Ratings listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

[2] Power dissipation shall not exceed P_d or ASO.

[3] Pw ≤ 10μs and duty cycle ≤ 1%.

[4] The maximum junction temperature T_J for the IPM is 150℃ (@case temperature T_C ≤ 100℃). However, it shall be limited to $T_{J(av)}$ ≤ 125℃ (@case temperature Tc ≤ 100℃) to ensure the IPM operates safely and reliably.

[5] The power dissipation is 24mW/℃ at operating temperature of 25℃ or above when the chip is mounted on a 70mm × 70mm × 1.6mm FR4 glass-epoxy circuit board with less than 3% copper foil.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{DC}		-	310	400	V
Supply Voltage V_{CC}	Between V_{CC} and GND	13.5	15	16.5	V
High-side Bias Voltage V_{BS}	Between V_B and V_S	13.5	15	16.5	V
PWM Switching Frequency F_{PWM}	T_J ≤ 150℃	-	-	20	kHz
Logic Input Voltage (HIN, LIN)V_{IN}		0	-	Vcc	V
Ambient Temperature T_A		-40	-	85	℃

Note

All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25℃ and V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Driver					
MOSFET Output					

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage $V_{(BR)DSS}$		500	-	-	V
Drain-to-Source Leakage Current I_{DSS}	Single MOS	-	-	100	μA
Static Drain-to-Source On Resistance $R_{DS(ON)}$	I_D = 2.5A	-	1.2	1.7	Ω
Source-to-Drain Diode Forward Voltage V_{SD}	I_D = 2.5A	-	-	1.4	V
Power Supply					
V_{CC} Quiescent Current I_{QCC}	V_{IN} = 0V / 5V	240	480	720	μA
V_B Quiescent Current I_{BBS}		30	75	120	μA
V_{CC} Under-voltage Lockout (UVLO)					
V_{CC} Release Voltage V_{CCUVH}		11.5	12.1	12.7	V
V_{CC} Lockout Voltage V_{CCUVL}		10.5	11.1	11.7	V
V_B Under-voltage Lockout (UVLO)					
V_B UVLO Release Voltage V_{BUVH}	$V_{BX} - V_X$	9.5	10.1	10.7	V
V_B UVLO Lockout Voltage V_{BUVL}	$V_{BX} - V_X$	8.5	9.1	9.7	V
Input Signal					
High-level Input Voltage V_{IH}		2.8	-	-	V
Low-level Input Voltage V_{IL}		-	-	0.8	V
High-level Input Bias Current I_{IN+}	V_{IN} = 5V	12	24	36	μA
High-level Input Bias Current I_{IN-}	V_{IN} = 0V	-	-	1	μA
Deadtime DT		260	480	700	ns

4.4 Package Thermal Resistance

Table 4-4 SSOP A54-38 Package Thermal Resistance

Parameter	Test Conditions	Max.	Unit
Junction-to-ambient Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	42.5	℃/W
Junction-to-package-top Thermal Resistance Ψ_{JT}	JEDEC standard, 2S2P PCB	12.5	℃/W

Note

[1] The actual measurements may vary depending on the conditions.

5 Function Descriptions

5.1 Under-voltage Lockout (UVLO)

Figure 5-1 Under-voltage Lockout (Low-side)

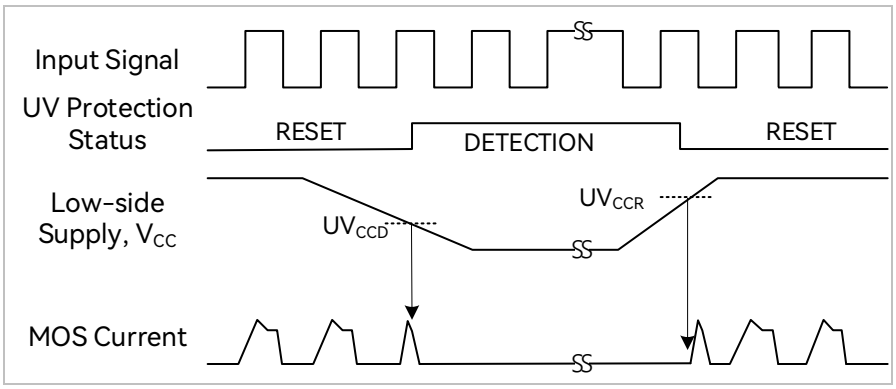
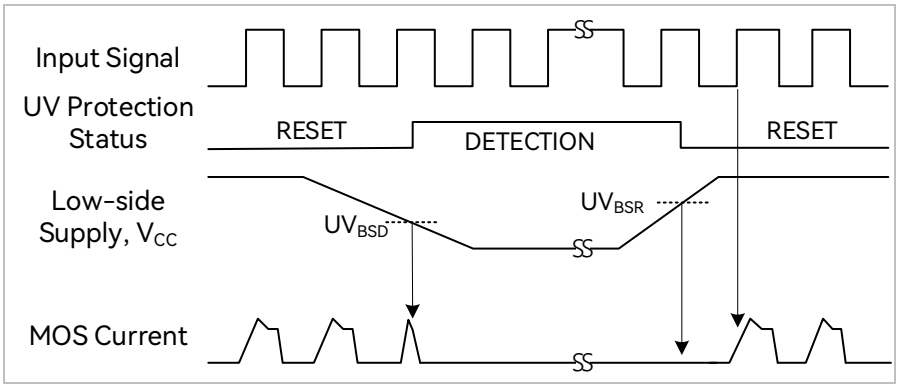


Figure 5-2 Under-voltage Lockout (High-side)



6 Revision History

Rev.	Description	Date	Prepared By
V1.1	First release, translated from the Chinese version V1.1	2025/01/22	Freya Fu
V1.2	Modified “3.5V/5V MCU” as “3.3V/5V MCU” in sector 1.3 Features	2025/05/14	Freya Fu
V1.3	Reviewed the Test Conditions and Parameters of VCC Quiescent Current IQCC and VBB Quiescent Current IBBS	2025/06/05	Freya Fu

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