Datasheet

Three-Phase IPM for High-voltage Applications FE0661AAS

Fortior Technology (Shenzhen) Co., Ltd

Contents

1 System Introduction

1.1 Overview

FE0661AAS is a three-phase intelligent power module (IPM) especially designed for high-voltage applications. It integrates three high-voltage half-bridge gate driver chips, six low-loss IGBTs and six fast-recovery diodes. Due to a high level of integration, few peripheral components are required during application. FE0661AAS contains VCC/VBS under-voltage lockout (UVLO) circuitry, protecting the power tube from operating with insufficient voltage. Also, the power module provides separate negative DC terminals for each phase to measure the current independently. Moreover, FE0661AAS supports cross-conduction prevention and deadtime insertion to effectively protect the power IC. With strong insulation, high thermal conductivity and low electromagnetic interference, the power module is housed in a compact package and suitable for built-in motors and other space constraint applications.

1.2 Applications

Range hoods, high-voltage fans, pumps, etc.

FE0661AAS

1.3 Features

- 650V 6A Trench IGBT (T_C = 100°C)
- VCC range: 13V ~ 20V
- Separate negative IGBT terminals to measure the current of the inverter
- Support high-level signals, and compatible with 3.3V/5V MCU
- Low electromagnetic interference design
- Support UVLO feature
- Built-in deadtime module
- Withstand isolation voltage: 2000V
- RoHS compliant

1.4 Key Parameters

- IGBT VCE Voltage: 650V
- Single IGBT Drive Current (DC): ± 6A (Max)
- Single IGBT Drive Current (Pulse): ± 12A (Max)
- IGBT Saturation Voltage VCE (sat): 1.73V (Typ)
- Max. Junction Temperature: +150°C
- Power Dissipation: 3.00W

1.5 Typical Application Diagram

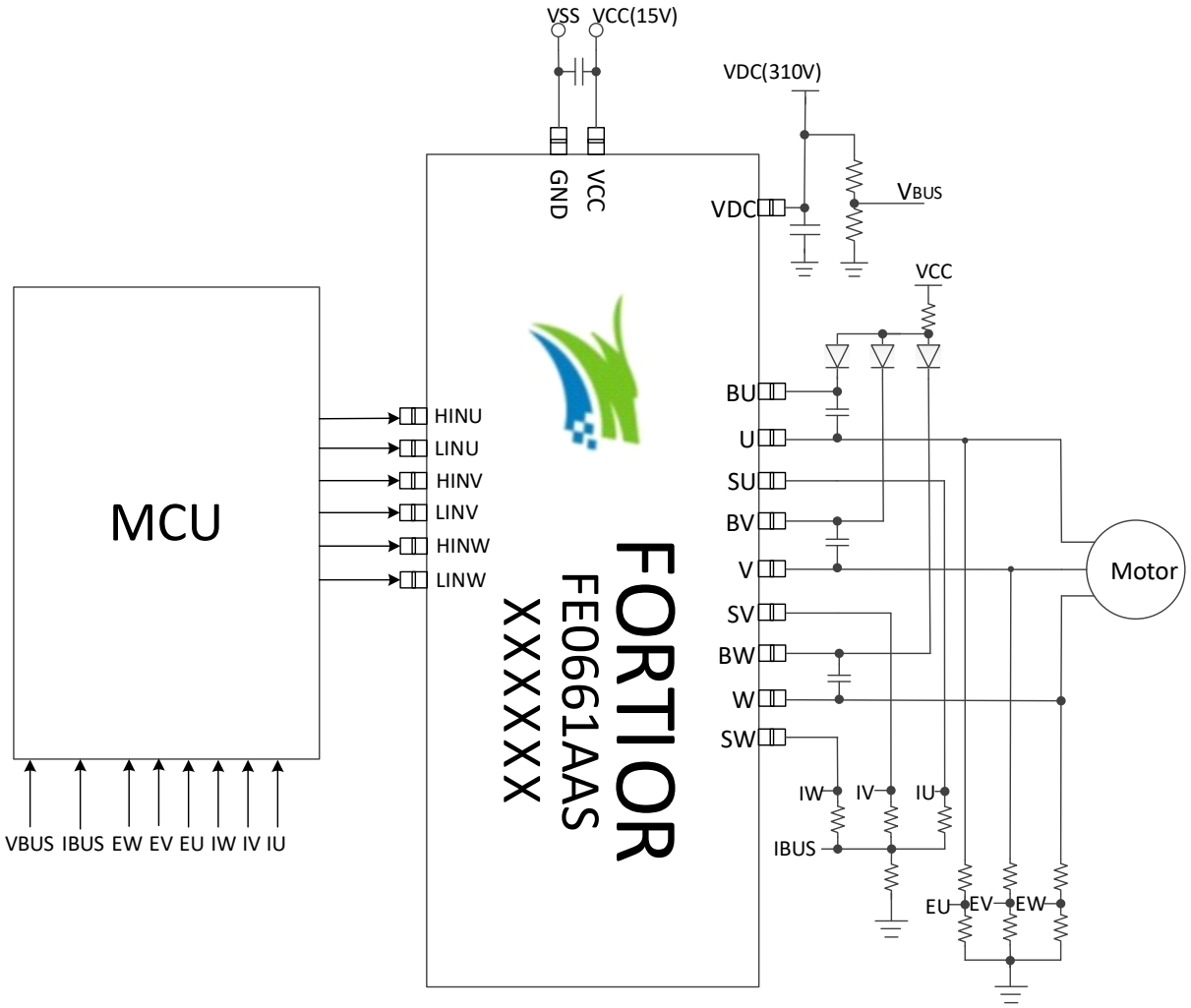


Figure 1-1 Typical Application Diagram of FE0661AAS

1.6 Functional Block Diagram

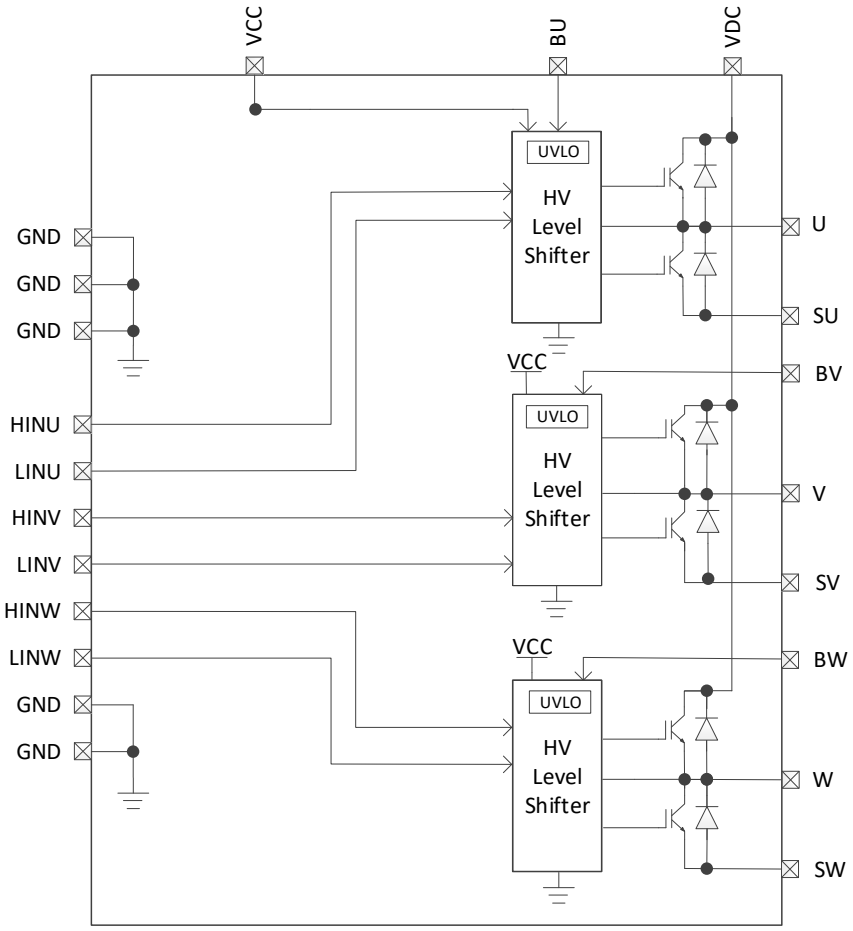


Figure 1-2 Functional Block Diagram of FE0661AAS

1.7 Pinout Diagram

1.7.1 FE0661AAS SSOP A54-38 Pinout Diagram

Figure 1-3 FE0661AAS SSOP A54-38 Pinout Diagram

1.8 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DB = Digital Bidirectional
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.8.1 FE0661AAS SSOP A54-38 Pins

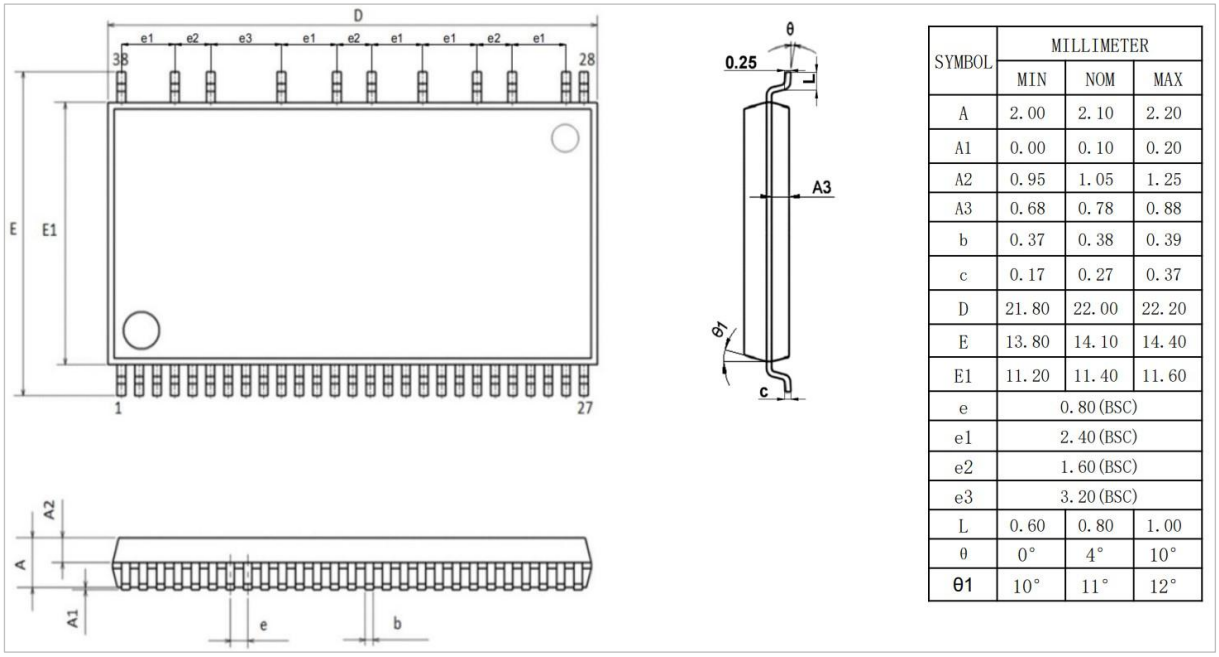
Table 1-1 FE0661AAS SSOP A54-38 Pin Descriptions

Pin	FE0661AAS SSOP A54-38	IO Type	Function Descriptions
VCC	1	P	Power input
GND	2	P	Ground
GND	3	P	Ground
GND	4	P	Ground
NC	5	-	Not connected
LINW	6	DI	Low-side signal input for phase W
NC	7	-	Not connected
HINW	8	DI	High-side signal input for phase W
NC	9	-	Not connected
NC	10	-	Not connected
NC	11	-	Not connected
NC	12	-	Not connected
LINV	13	DI	Low-side signal input for phase V
NC	14	-	Not connected
HINV	15	DI	High-side signal input for phase V
NC	16	-	Not connected
NC	17	-	Not connected
NC	18	-	Not connected
NC	19	-	Not connected
NC	20	-	Not connected
LINU	21	DI	Low-side signal input for phase U
NC	22	-	Not connected
HINU	23	DI	High-side signal input for phase U
NC	24	-	Not connected
GND	25	P	Ground
GND	26	P	Ground
VCC	27	P	Power input

Pin	FE0661AAS SSOP A54-38	IO Type	Function Descriptions
VDC	28	P	High-voltage power supply
VDC	29	P	High-voltage power supply
BU	30	P	U-phase floating power supply. The voltage floats with respect to phase U.
U	31	DO	U-phase output
SU	32	P	U-phase ground
BV	33	P	V-phase floating power supply. The voltage floats with respect to phase V.
V	34	DO	V-phase output
SV	35	P	V-phase ground
BW	36	P	W-phase floating power supply. The voltage floats with respect to phase W.
W	37	DO	W-phase output
SW	38	P	W-phase ground

2 Package Information

2.1 FE0661AAS SSOP A54-38



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.00	2.10	2.20
A1	0.00	0.10	0.20
A2	0.95	1.05	1.25
A3	0.68	0.78	0.88
b	0.37	0.38	0.39
c	0.17	0.27	0.37
D	21.80	22.00	22.20
E	13.80	14.10	14.40
E1	11.20	11.40	11.60
e	0.80(BSC)		
e1	2.40(BSC)		
e2	1.60(BSC)		
e3	3.20(BSC)		
L	0.60	0.80	1.00
θ	0°	4°	10°
θ1	10°	11°	12°

Figure 2-1 FE0661AAS SSOP A54-38 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Saturation Voltage (High Side + Low Side) (V)	Single IGBT Average Drive Current (A)	Control Features	Protection Features		Operating Junction Temperature T_J(℃)	Lead-free	Package	Package Method	Quantity
				Drive Type	Under-voltage Lockout	Cross-conduction Prevention					
FE0661AAS	13 ~ 20	3.46	6	N + N	√	√	-40 ~ 150	√	SSOP A54-38	Tape & Reel	1000

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings[1]

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IGBT					
IGBT Collector-to-Emitter Voltage V_{CEMAX}		650	-	-	V
Continuous Collector Current $I_{CEMAX(DC)}$ of Single IGBT	T_C = 100°C	-	-	6[2]	A
Continuous Collector Current $I_{CEMAX(PLUS)}$ of Single IGBT	T_C = 25°C	-	-	12[2]	A
Pulsed Collector Current I_{CM} of Single IGBT	T_{JMAX}	-	-	18[2][3]	A
SOA Turn-off Current I_{LM} of Single IGBT	$V_{CE} \leq 650V, T_{JMAX}$	-	-	18[2][3]	A
Continuous Diode Forward Current I_F	T_C = 25°C	-	-	12[2]	A
	T_C = 100°C	-	-	6[2]	A
Short Circuit Withstand Time T_{SC}	V_{GE} = 15V,VCC ≤ 400V, $T_J \leq 175°C$	-	-	5	μs
Controller					
High-side Floating Absolute Voltage V_{BU}, V_{BV}, V_{BW}		-0.3	-	625[2]	V
High-side Floating Offset Voltage V_S		V_B - 25	-	V_B + 0.3	V
High-side Output Voltage V_{HO}		V_S - 25	-	V_B + 0.3	V
Low-side Supply Voltage V_{CC}		-0.3	-	25	V
Low-side Output Voltage V_{LO}		-0.5	-	V_{CC} + 0.3	V
Logic Input Voltage (HIN,LIN) V_{IN}		-0.5	-	V_{CC} + 0.3	V
Offset Voltage Transient dVS/dt		-	≤ 50	-	V/ns
Overall System					
Storage Temperature T_{STG}		-40	-	125	℃
Case Temperature T_C	-40°C ≤ T_J ≤ 150°C	-30	-	125	°C
Withstand Isolation Voltage V_{ISO}	60Hz, Sine Wave, 60s, The pin is connected to the substrate	-	-	2000	V_{rms}
Junction Temperature T_J[4]		-40	-	150	°C
Power Dissipation P_d		-	-	3[5]	W

Notes:

[1] Stress values greater than Table 4-1 Absolute Maximum Ratings[1] listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

[2] Power dissipation shall not exceed P_d or ASO.

[3] Pw ≤ 10μs and duty cycle ≤ 1%.

[4] The maximum junction temperature T_J for the IPM is 150°C (@case temperature T_C ≤ 100°C). However, it shall be limited to T_J(av) ≤ 125°C (@case temperature T_C ≤ 100°C) to ensure the IPM operates safely and reliably.

[5] The power dissipation is 24mW/°C at operating temperature of 25°C or above when the chip is mounted on a 70mm × 70mm × 1.6mm FR4 glass-epoxy circuit board with less than 3% copper foil.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{DC}		-	310	400	V
Supply Voltage V_{CC}	Between V_{CC} and GND	13.5	15	16.5	V
High-side Bias Voltage V_{BS}	Between V_B and V_S	13.5	15	16.5	V
PWM Switching Frequency F_{PWM}	T_J ≤ 150°C	-	-	20	kHz
Logic Input Voltage (HIN, LIN)V_{IN}		0	-	V_{cc}	V
Ambient Temperature T_A		-40	-	85	°C

Note:

All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25°C and V_{CC} = 15V unless otherwise specified)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Driver						
IGBT Output						
Collector-to-Emitter Saturation Voltage $V_{CE(SAT)}$	V_D = V_{DB} = 15V, V_{IN} = 15V, I_C = 6A	T_J = 25°C	-	1.73	2.2	V
		T_J = 125°C	-	2.05	-	V
FWD Forward Voltage V_{EC}	V_{IN} = 0V, I_C = -6A		-	1.9	2.4	V

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current I_{CES}	V_{CE} = 650	T_J = 25°C	-	-	10	μA
		T_J = 125°C	-	-	100	μA
Power Supply						
V_{CC} Quiescent Current I_{QCC}	VIN = 0V / 5V		240	480	720	μA
V_B Quiescent Current I_{BBS}			30	75	120	μA
V_{CC} Under-voltage Lockout (UVLO)						
V_{CC} Release Voltage V_{CCUVH}			11.5	12.1	12.7	V
V_{CC} Lockout Voltage V_{CCUVL}			10.5	11.1	11.7	V
V_B Under-voltage Lockout (UVLO)						
V_B UVLO Release Voltage V_{BUVH}	$V_{BX} - V_X$		9.5	10.1	10.7	V
V_B UVLO Lockout Voltage V_{BUVL}	$V_{BX} - V_X$		8.5	9.1	9.7	V
Input Signal						
High-level Input Voltage V_{IH}			2.8	-	-	V
Low-level Input Voltage V_{IL}			-	-	0.8	V
High-level Input Bias Current I_{IN+}	V_{IN} = 5V		12	24	36	μA
High-level Input Bias Current I_{IN-}	V_{IN} = 0V		-	-	1	μA
Deadtime DT			260	480	700	ns

4.4 Package Thermal Resistance

Table 4-4 SSOP A54-38 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
θ_{JA} Junction-to-ambient Thermal Resistance[1]		42.5	℃/W
Junction-to-package-top Thermal Resistance Ψ_{JT}		12.5	℃/W

Note:

The actual measurements may vary depending on the conditions.

5 Function Descriptions

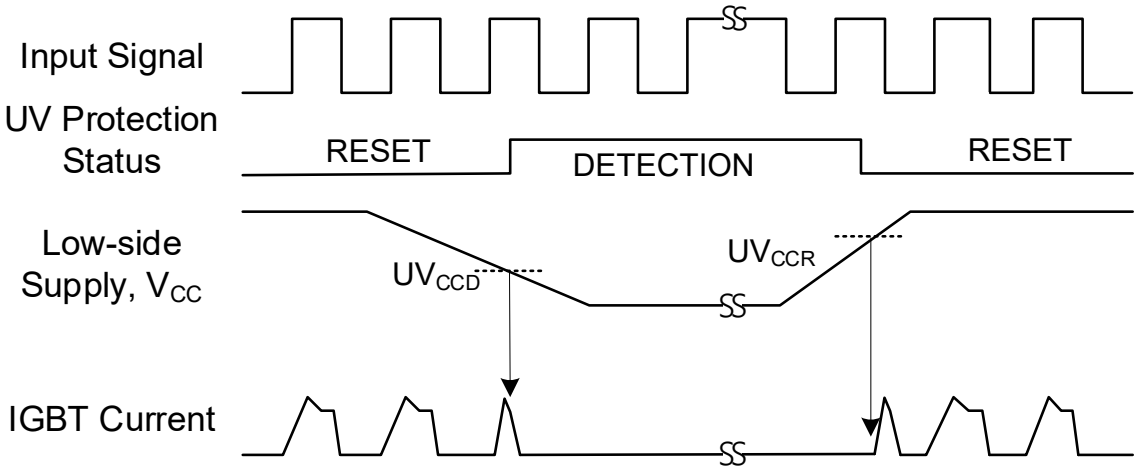


Figure 5-1 Under-voltage Lockout (Low-side)

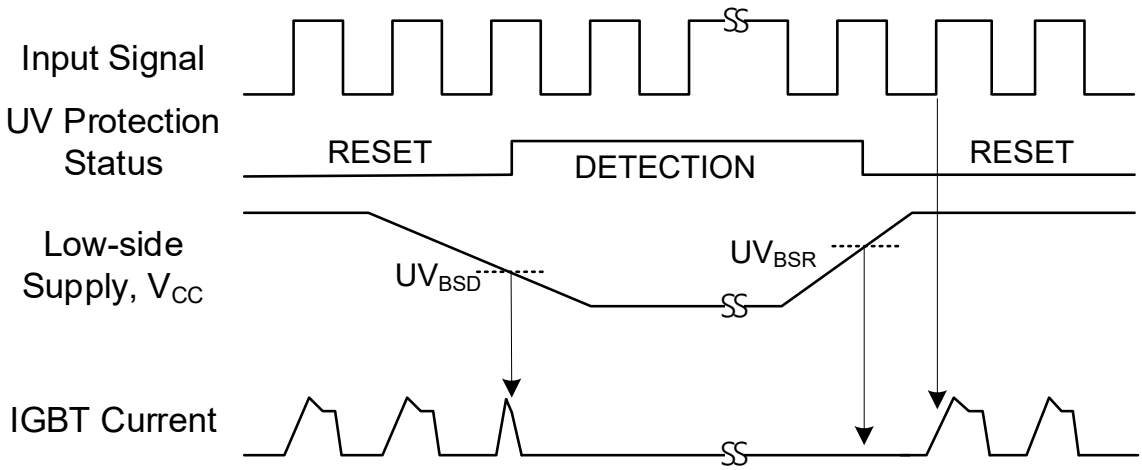


Figure 5-2 Under-voltage Lockout (High-side)

6 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release	2024/09/06	Eric Deng
V1.1	1. Updated 1.6 Functional Block Diagram; 2. Updated 2 Package Information; 3. Modified "Inverter" as "IGBT" in 4.1 Absolute Maximum Ratings.	2024/10/15	Freya Fu
V1.2	1. Modified the voltage "12.5V ~ 20V" as "13V ~ 20V" in 1.3 Features; 2. Reviewed the "Power Supply" from 3 "12.5V ~ 20V" to "13V ~ 20V" "Power Supply" in 3 Ordering Information; 3. Added "T_A = 25℃ unless otherwise specified" in 4.1 Absolutely Maximum Ratings; 4. Refiewed the Typ. of "Supply Voltage V_{CC}" from "300V" to "310V" in 4.2 Recommended Operating Conditions; 5. Modified the Test Conditions of "V_{CC} Quiescent Current I_{QCC}" and "V_B Quiescent Current I_{BBS}" as "V_{IN} = 0V" and updated parameters in 4.3 Global Electrical Characteristics.	2024/12/06	Freya Fu
V1.3	1. Modified "600V 6A Trench IGBT" as "650V 6A Trench IGBT" in 1.3 Features; Reviewed the key parameter of "IGBT VCE Voltage" from 600V to 650V; 2. Modified the Min. of "IGBT Collector-to-Emitter Voltage V_{CEMAX}" as 650V and modified the Test Conditions of "SOA Turn-off Current I_{LM} of Single IGBT" as "$V_{CE} \leq 650V$" in 4.1 Absolute Maximum Ratings.	2024/12/24	Freya Fu
V1.4	Modified "3.5V/5V MCU" as "3.3V/5V MCU" in sector 1.3 Features	2025/05/14	Freya Fu
V1.5	Reviewed the Test Conditions and Parameters of V_{CC} Quiescent Current I_{QCC} and V_{BB} Quiescent Current I_{BBS}	2025/06/05	Freya Fu

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Fortior Technology (Shenzhen) Co., Ltd.

Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com

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