Datasheet

Three-phase BLDC Motor Controller with Built-in Pre-driver

FT8213Q

Fortior Technology (Shenzhen) Co., Ltd

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FT8213Q Three-phase BLDC Motor Controller with Built-in Pre-driver

1 System Introduction

1.1 Overview

FT8213Q is an IC with built-in MOS and pre-driver designed for three-phase BLDC motor driver applications. It supports sensorless FOC and designs with a 1Ω internal Rdson. Due to a high level of integration, the chip has few peripheral components and features with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode are stored in EFUSE. PWM, analog voltage input or I²C interface is available for motor speed regulation. Moreover, the chip integrates speed indicator to read motor speed in real time via FG pin or I²C interface. Constant speed control mode, constant air flow control mode, constant current control mode or open-loop control mode is optional. In addition, the chip is secured with a wide range of protection features, including phase loss protection, over-voltage lockout (OVLO), over-current protection (OCP), under-voltage lockout (UVLO), current-limiting protection (CLP), temperature sensor detect (TSD), motor lock protection (MLP), etc. Sleep-mode current of the chip is about 45μA.

1.2 Applications

Refrigerator fans, cooling fans, water pumps, etc.

1.3 Features

- Input supply voltage: 5 ~ 18V
- Rdson: 1Ω (high-side MOS + low-side MOS）
- Drive current: 1A
- No Hall-based sensor is required
- FOC control to reduce motor noise and vibration
- Motor parameters, startup control parameters and speed regulation mode are stored in EFUSE.
- I²C, PWM or analog voltage input interface for motor speed regulation
- Constant speed control mode, constant air flow control mode, constant current control mode or open-loop control mode is optional
- Forward or reverse rotation selectable
- Motor speed indication or motor block indication is configurable
- Sleep-mode current: 45μA
- Wake-up through SPEED pin or I²C interface
- Configurable I²C address
- Phase loss protection
- Over-voltage lockout (OVLO)
- Over-current protection (OCP)
- Under-voltage lockout (UVLO)
- Current-limiting protection (CLP)
- Temperature sensor detect (TSD)
- Motor lock protection (MLP)

1.4 Typical Application Diagram

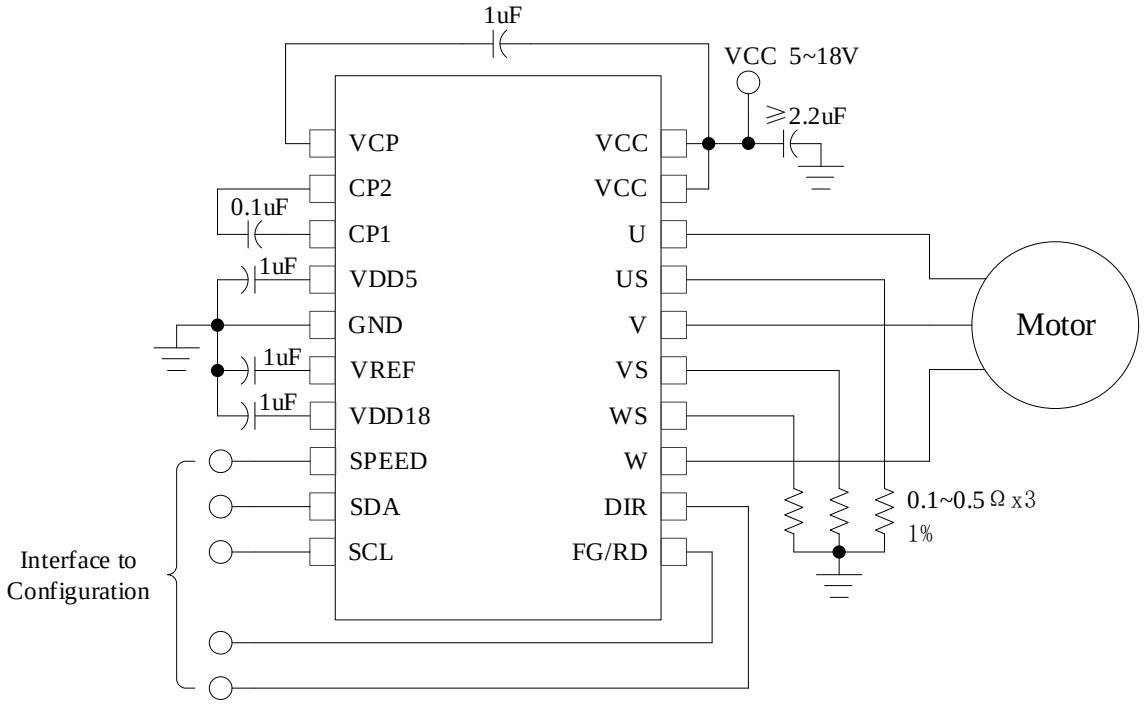


Figure 1-1 Typical Application Diagram of FT8213Q

1.5 Functional Block Diagram

1.5.1 FT8213Q

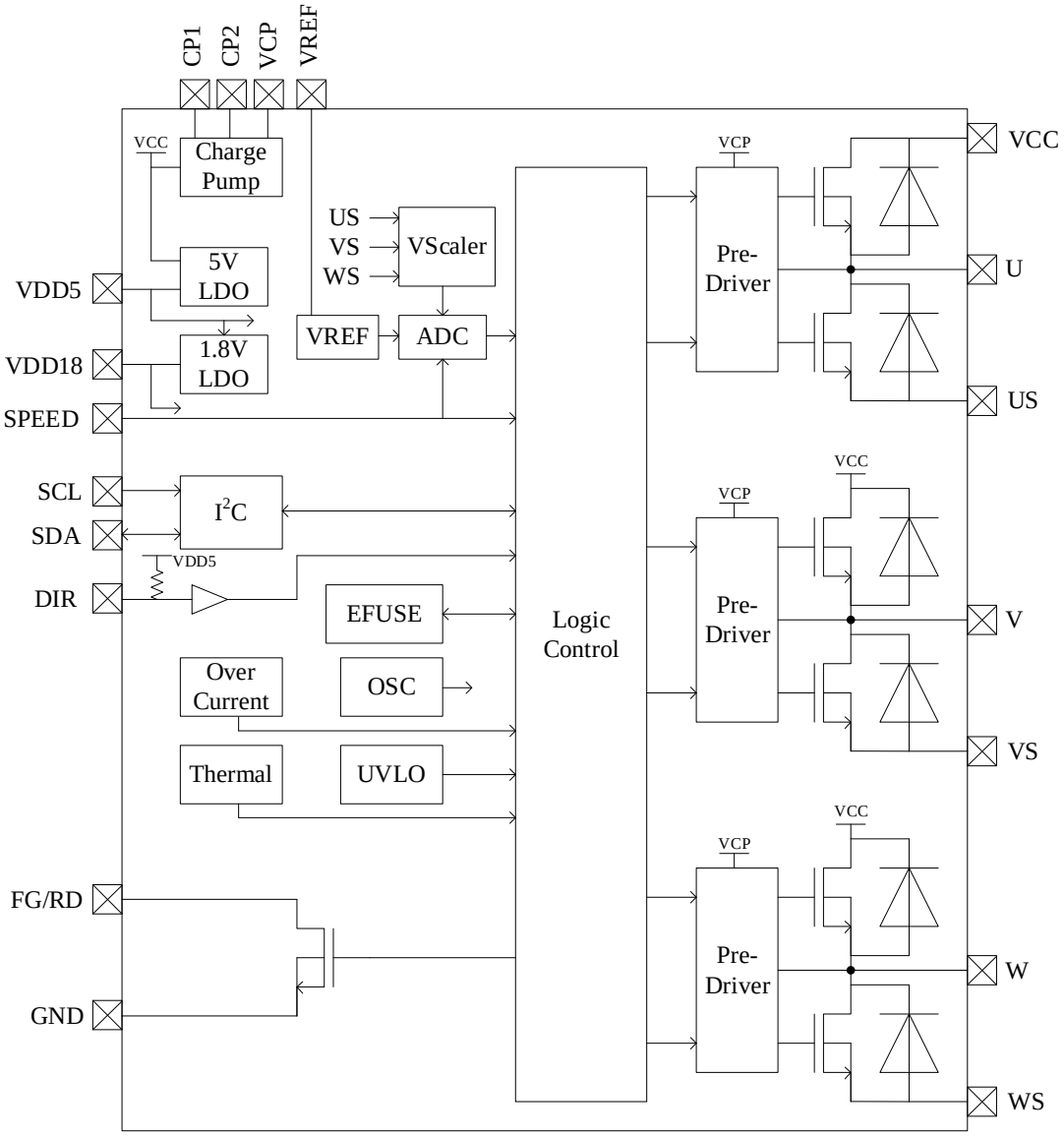


Figure 1-2 Functional Block Diagram of FT8213Q

1.6 Pinout Diagram

1.6.1 FT8213Q QFN28

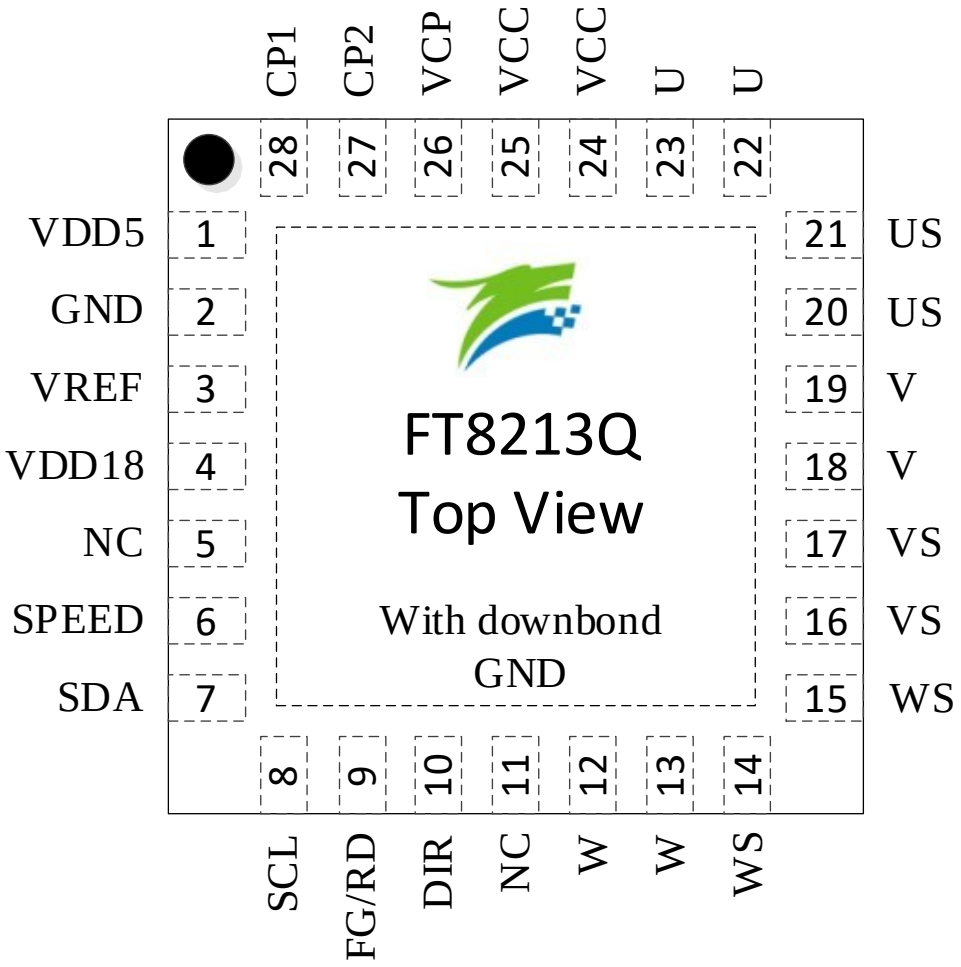


Figure 1-3 FT8213Q QFN28 Pinout Diagram

1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.1 FT8213Q QFN28 Pins

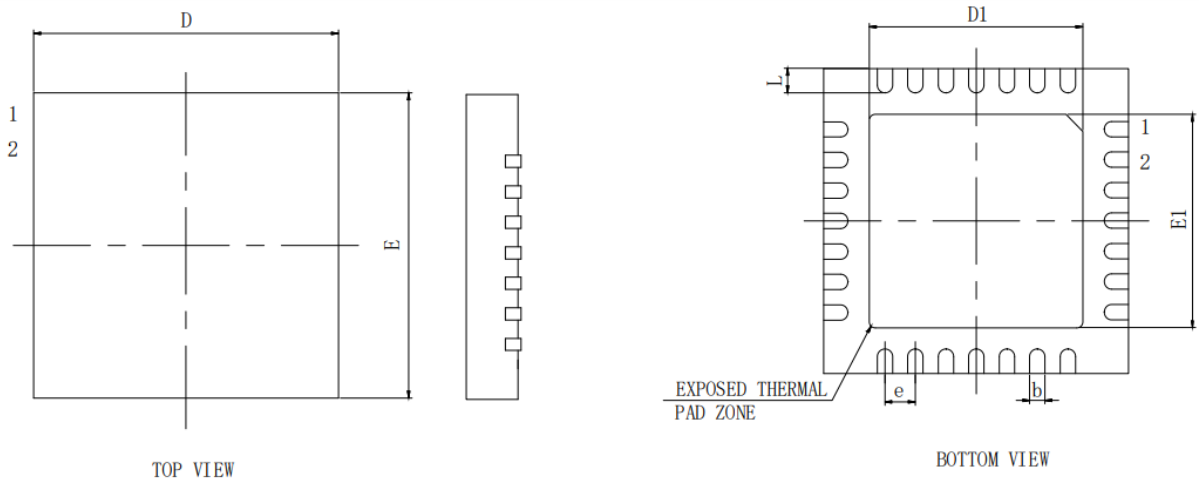
Table 1-1 FT8213Q QFN28 Pin Descriptions

Pin	FT8213Q QFN28	IO Type	Function Description
VDD5	1	P	5V LDO output with a 1μF ~ 4.7μF capacitor connected to ground
GND	2	P	Ground
VREF	3	AI	ADC reference voltage, with a 1μF external capacitor connected to ground
VDD18	4	P	1.8V LDO output with a 1μF external capacitor connected to ground
NC	5		Not connected
SPEED	6	DI/AI	Speed control input, PWM or analog voltage, determined by EFUSE; Internal pull-up resistor is available in PWM input mode; When I^2C is selected for motor speed regulation, this pin does not work, and is left floating or is connected with VDD5.
SDA	7	DB	I^2C SDA in slave mode, with collector open-drain output, maximum speed rate at 400KHz and an internal configurable pull-up resistor
SCL	8	DB	I^2C SCL in slave mode, with collector open-drain output, maximum speed rate at 400KHz and an internal configurable pull-up resistor
FG/RD	9	DO	Motor speed signal or motor block indication, with collector open-drain output and an internal configurable pull-up resistor
DIR	10	DI	Motor rotation control, with built-in pull-up resistor 1: Forward output phase sequence: U --> V --> W. 0: Reverse output phase sequence: U --> W --> V.
NC	11		Not connected
W	12	DO	W-phase output
W	13	DO	W-phase output
WS	14	AI	W-phase ground input
WS	15	AI	W-phase ground input
VS	16	AI	V-phase ground input
VS	17	AI	V-phase ground input
V	18	DO	V-phase output
V	19	DO	V-phase output
US	20	AI	U-phase ground input
US	21	AI	U-phase ground input
U	22	DO	U-phase output
U	23	DO	U-phase output
VCC	24	P	Power supply. The input voltage range is 5V ~ 18V, with a capacitor of 2.2μF or above connected to ground (depends on actual applications)

Pin	FT8213Q QFN28	IO Type	Function Description
VCC	25	P	Input power supply
VCP	26	P	Charge pump output, with a 1μF~4.7μF capacitor connected to VCC pin
CP2	27	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins
CP1	28	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins

2 Package Information

2.1 FT8213Q QFN28_5X5



QFN28			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1			0.05
E	4.9	5	5.1
D	4.9	5	5.1
E1	3.4	3.5	3.6
D1	3.4	3.5	3.6
L	0.35	0.4	0.45
e		0.5	
b	0.18	0.25	0.3

Figure 2-1 FT8213Q QFN28_5X5 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Supply Voltage (V)	Rdson (High Side + Low Side) (Ω)	Drive Current (A)	Control Features						Protection Features						Operating Temperature Tj (°C)	Lead-free	Package
				Driver Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	Phase Loss Protection	OVLO	OCP	UVLO	CLP	TSD	MLP			
					I²C	PWM	Analog Voltage												
FT8213Q	5 ~ 18	1	1	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	QFN28 (5x5 mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A[2]		-40	—	85	℃
Operating Ambient Temperature T_A[2]	FT8213Q, I(VCC) ≤ 0.5A	-40	—	105	℃
Operating Junction Temperature T_J		-40	—	150	℃
Storage Temperature		-55	—	150	℃
VCC Supply Voltage		-0.3	—	22	V
VCC to VSS Spike Voltage	Peak Duration < 500ms	-0.3	—	26	V
VCP to VCC Voltage		-0.7	—	6.5	V
US/VS/WS Voltage		-0.7	—	0.7	V
SPEED/SDA/SCL/DIR/FG Voltage		-0.3	—	VDD5 + 0.3	V

Notes:

[1] Stress values greater than "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

[2] It is not mandatory as long as Operating Junction Temperature T_J does not exceed the maximum specified.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

(T_A = 25°C and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		5	—	18	V
VDD5 Output Voltage	T_A = -40 ~ 85°C	4.8	5	5.2	V
V_{REF} Reference Voltage	T_A = -40 ~ 85°C	4.3	4.5	4.7	V
I_{VCC} Operating Current[1]		—	5	—	mA
I_{VCC} Sleep-mode Current		—	45	100	μA
Rdson (High-side MOS + Low-side MOS)		—	1	—	Ω

[1] Characteristics may vary with different configurations.

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OVP} VCC OVLO Threshold Voltage		22	24	26	V
V_{OVP_HYS} VCC OVLO Hysteresis Voltage		—	0.5	—	V
V_{UVLO_F} VCC UVLO Threshold Voltage		—	4.5	4.6	V
V_{UVLO_HYS} VCC UVLO Hysteresis Voltage		—	0.2	—	V
I_{OCP} OCP Threshold Current		1.6	1.7	—	A
T_{TSD} TSD Threshold Temperature		—	165	—	℃
T_{TSD_HYS} TSD Hysteresis Temperature		—	15	—	℃

4.4 Speed Control with Analog Voltage

Table 4-4 Speed Control with Analog Voltage

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SPDMAX}		—	VREF	—	V

4.5 IO Electrical Characteristics (SCL/SDA/SPEED/FG/DIR)

Table 4-5 IO Electrical Characteristics (SCL/SDA/SPEED/FG/DIR)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH} High-level Input Voltage		2.5	—	—	V
V_{IL} Low-level Input Voltage		—	—	0.6	V
I_{OL} Output Sink Current	V_{out} = 0.3V	5	—	—	mA
F_{IN} PWM Input Frequency		1	—	100	KHz

4.6 Package Thermal Resistance

Table 4-6 QFN28 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	43	℃/W
Junction-to-case Temperature Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	15	℃/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Description

5.1 Operating Modes

The chip works in normal mode (Normal) or sleep mode (Sleep).

5.2 Communication Interfaces

The chip integrates I^2C interface for slave devices with programmable address starting from "0x00" and maximum transmission speed less than 400KHz.

5.3 Speed Control

5.3.1 Speed Control Modes

The chip supports three types of speed control input interface: PWM, analog voltage and I^2C, and only one of them can be chosen at a time. PWM control mode and analog voltage control mode support inverting input. When voltage-loop control mode is selected, motor speed can be controlled by varying the supply voltage.

5.3.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input, and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

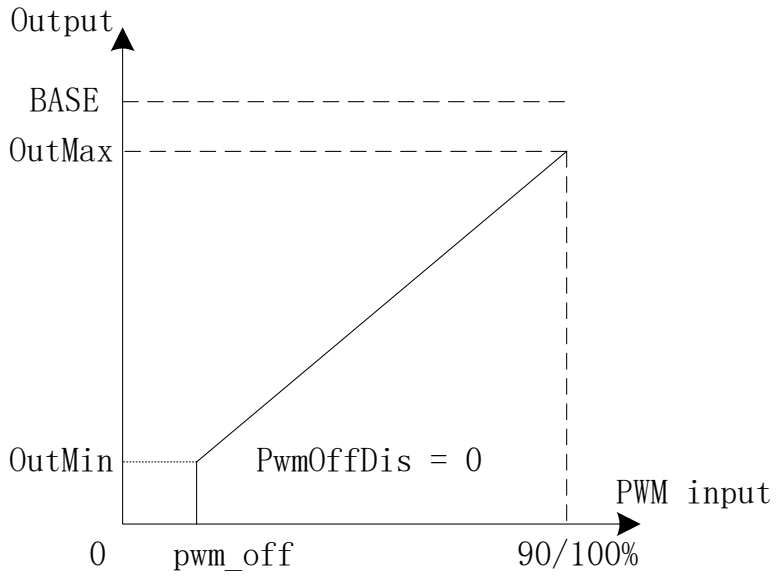


Figure 5-1 Output Curve at PwmOffDis = 0

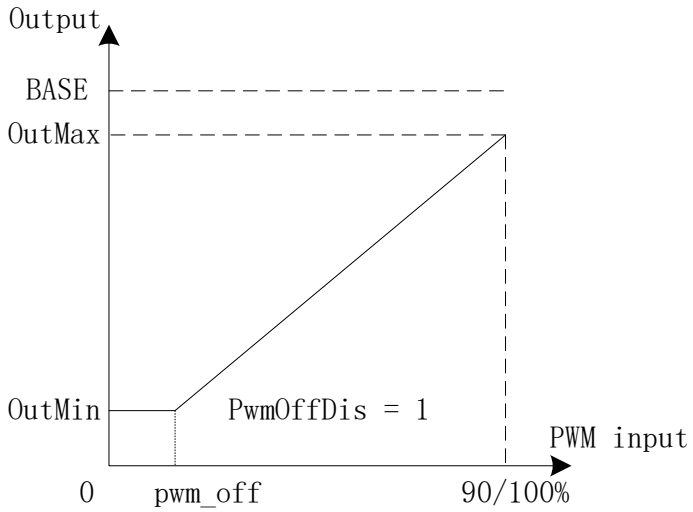


Figure 5-2 Output Curve at PwmOffDis = 1

5.4 Protection Features

The chip supports protection features, including phase loss protection, over-voltage lockout, over-current protection, under-voltage lockout, temperature sensor detect, motor lock protection, etc.

5.5 FG

The chip delivers motor speed signal or motor status via FG/RD pin.

5.5.1 Frequency Multiplication and Division of FG

Configuring FG/RD to FG outputs FG signal, that is, FG/RD pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2, 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	**2**	**3**	**4**
FGDIV	**1**	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

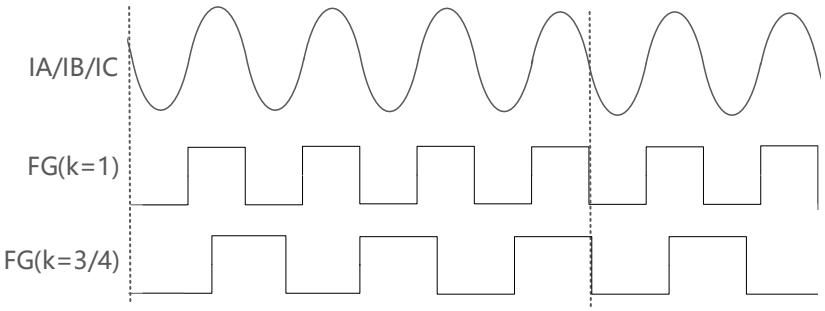


Figure 5-3 FG Output Waveforms at k = 1 and k= 3/4

5.5.2 FG Output in Open-loop Control Mode

FG pin outputs feedback signal to indicate rotation speed of the motor in close-loop control mode, but not in open-loop control mode. The chip outputs FG signal or high-level signal according to FGSet.

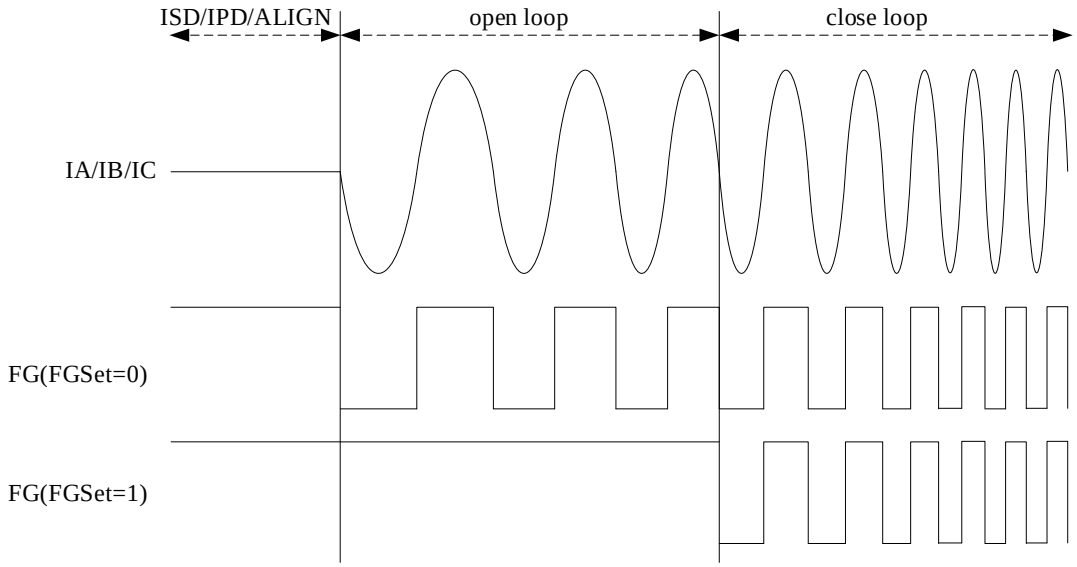


Figure 5-4 FG Output Waveform

5.6 RD

RD pin outputs high-level signal to indicate operating status of the motor. Configuring FG/RD to RD outputs RD signal, that is, FG/RD pin is selected to output RD signal. The chip outputs different RD signals according to FGSet.

- FGSet = 0: RD = 0 in open-loop or close-loop control mode and RD = 1 in other control modes.
- FGSet = 1: RD = 0 in close-loop control mode and RD = 1 in other control modes.

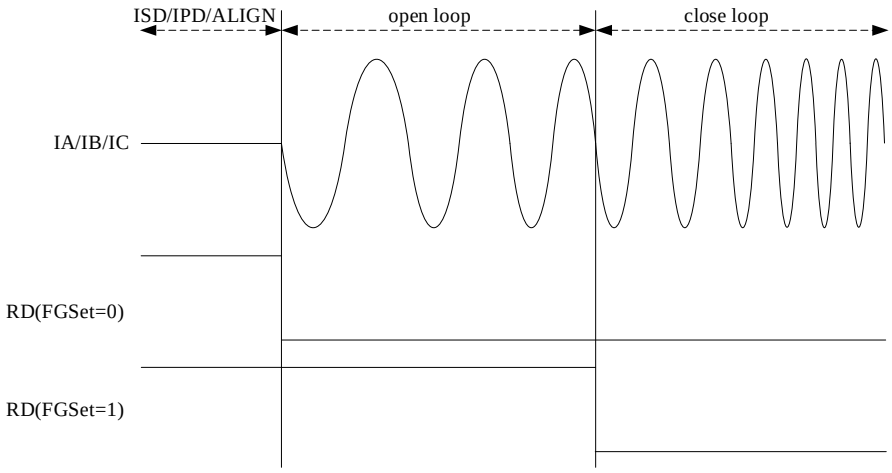


Figure 5-5 RD Output Waveform

6 Revision History

Rev.	Description	Date	Prepared By
V1.1	First release, translated from Chinese version 1.1	2021/05/28	Husy Hu
V1.2	Modified the name of section "1.6 Packaging" as "1.6 Pinout Diagram".	2022/05/21	Bruce Long
V1.3	1. Modified the pin name "FG" as "FG/RD"; 2. Added "phase loss protection" in section 1.1 Overview; 3. Added "current-limiting protection (CLP)" in sections 1.1 Overview, 1.3 Features and 3 Ordering Information; 4. Modified the description "a configurable pull-up resistor" as "an internal configurable pull-up resistor" in section 1.7.1 FT8213Q QFN28 Pins; 5. Corrected the maximum value "VCC + 6.5V" of VCP to VCC Voltage in Table 4-1 Absolute Maximum Ratings as "6.5V"; 6. Modified maximum transmission speed of I^2C interface "1Mbps" in section 5.2 Communication Interfaces as "400KHz"; 7. Updated descriptions in section 5.5.1 Frequency Multiplication and Division of FG; 8. Modified "FGRDSet" in section 5.5.2 FG Output in Open-loop Control Mode and 3.6 RD as "FGSet"; 9. Updated Figure 2-1 FT8213Q QFN28_5X5 Package Drawings and Dimensions; 10. Deleted "Please refer to speed regulating table" in section 5.3.2 Speed Control Curve; 11. Proofread the overall document, reorganized document structure and standardized document format.	2023/10/25	Eric Deng
V1.4	Modified the minimum value "-65℃" of Storage Temperature in Table 4-1 Absolute Maximum Ratings as "-55℃", and added the parameter "VCC to VSS Spike Voltage" in the table.	2023/12/13	Eric Deng

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