

DATASHEET

FU7512_64_65_74Q1

Three-phase Motor Control MCU

Future Is In Control

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Explanation of Symbols

- > The symbol “[]” following a register indicates a bit in the register. For example, ABCD[XY] indicates the XY bit in ABCD register.
- > The symbol “x” in a register name indicates similar registers. For example, TIMx_CR0 indicates TIM3_CR0 and TIM4_CR0.
- > [m:n] indicates a range of bits. For example, [3:0] means the bits from bit3 to bit0.
- > Register read and write symbols:
 - >> r: Read only
 - >> w: Write only
 - >> rw: Read/write
 - >> w0: Only 0 can be written
 - >> w1: Only 1 can be written
- > The symbol “-” indicates an uncertainty or invalid value.
- > The RMW instruction cannot be used for registers with different read and written representations.
- > Q (number) format is to store floating-point numbers using fixed-point numbers. MSB is the sign bit, followed by integer bits and fraction bits, where lower Q bits are assigned to the fractional part and the remaining bits are assigned to the integer part. For example, for Q12, bit15 is the sign bit, bit14 ~ bit12 represent the integer part and bit11 ~ bit0 represent the fraction part. The Q12 format has a decimal range -8 ~ 7.9998 (corresponding to 0x8000 ~ 0x7FFF).

Abbreviations

ADC	Analog to Digital Convertor
AO	Adaptive Observer
AFO	Adaptive Flux Observer
BEMF	Back Electromotive Force
BISS	Bidirectional Synchronous Serial Interface
BLDC	Brushless Direct Current
CFO	Common Flux Observer
CORDIC	Coordinate Rotation Digital Computer
CRC	Cyclic Redundancy Check
CSR	Control and Status Register
DAC	Digital to Analog Convertor
DMA	Direct Memory Access
FG	Frequency Generator
FICE	Fortior Interactive Connectivity Establishment
FOC	Field Oriented Control
FOSC	Fast Oscillator
GPIO	General Purpose Input Output
I ² C	Inter Integrated Circuit
IC	Integrated Circuit
IDE	Integrated Development Environment
LDO	Low Dropout Regulator
LPF	Low Pass Filter
LVD	Low Voltage Detection
LVDS	Low Voltage Differential Signal
IWDT	Independent Watchdog Timer
ME	Motor Engine
MSB	Most Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NC	Not Connected

NFO	Nonlinear Flux Observer
PGA	Programmable Gain Amplifier
PI/PID	Proportional Integral/Proportional Integral Derivative
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
QEP	Quadrature Encoder Pulse
RAM	Random Access Memory
RMW	Read Modified Write
ROM	Read Only Memory
RSD	Rotating State Detection
RTC	Real Time Clock
SAR	Successive Approximation Register
SCL	Serial Clock Line
SDA	Serial Data Line
SMO	Sliding Mode Observer
SOSC	Slow Oscillator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SVPWM	Space Vector PWM
TSD	Temperature Sensor Detect
UART	Universal Asynchronous Receiver/Transmitter
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

1 System Introduction

1.1 Features

- > Power Supply
 - » FU7512Q1: External power supply 3V ~ 5.5V is connected to VDD5 pin; internal LDO generates VDD2P5 voltage.
 - » FU7564Q1: External power supply 5.5V ~ 18V is connected to VCC pin; internal LDO generates VBB, VDD5, and VDD2P5 voltage.
 - » FU7565Q1: External power supply 9V ~ 60V is connected to VCC pin; Buck DC-DC converter generates VBB voltage; internal LDO generates VDD5 and VDD2P5 voltage.
 - » FU7574Q1: External power supply 5.5V ~ 18V is connected to VCC_x pin; internal LDO generates VBB_x, VDD5_x, and VDD2P5 voltage.
- > Dual core: RISC-V core and ME core
- > System clock up to 48MHz
- > 64kB Flash with ECC, CRC, self-program and code protection
- > Flash endurance: 1000 erase cycles
- > 12kB SRAM
- > 4kB PRAM for program execution
- > ME core integrates FOC module and CORDIC module
- > Interrupt sources with 8 configurable priority levels
 - » FU7512Q1: 32
 - » FU7564Q1: 31
 - » FU7565Q1: 28
 - » FU7574Q1: 29
- > Number of GPIOs
 - » FU7512Q1: 46

- » FU7564Q1: 29
- » FU7565Q1: 21
- » FU7574Q1: 36
- > Timers:
 - » Timer2 (FU7512Q1/FU7564Q1/FU7565Q1): Timer supporting PWM output, measurement of duty cycle and period of input PWM wave, measurement of the time of set PWM wave numbers, QEP decoding, rotating state detection, and rotation direction and speed detection of step motor
 - » Timer2 (FU7574Q1): Basic timing and counting
 - » Timer5 (FU7512Q1/FU7564Q1): Timer supporting PWM output, measurement of duty cycle and period of input PWM wave, measurement of the time of set PWM wave numbers, QEP decoding, rotating state detection, and rotation direction and speed detection of step motor
 - » Timer5 (FU7565Q1/FU7574Q1): Basic timing and counting
 - » Timer6: Timer supporting PWM output, measurement of duty cycle and period of input PWM wave, measurement of the time of set PWM wave numbers, and rotating state detection
 - » Timer3/Timer4/Timer7/Timer8: Timers supporting PWM output, and measurement of duty cycle and period of input PWM wave. Timer4 supports FG generation and Timer3/Timer8 supports up to 96MHz input.
 - » SysTick timer
 - » RTC
- > Communication interfaces:
 - » SPI
 - »» FU7512Q1: 2*SPIs
 - »» FU7564Q1: 1*SPI (SPI2), supporting only 3-wire mode
 - »» FU7565Q1: 1*SPI (SPI2), supporting only 3-wire mode
 - »» FU7574Q1: None
 - » I²C
 - »» FU7512Q1: 2*MCU I²Cs
 - »» FU7564Q1: 2*MCU I²Cs (where I²C2 is for internal use only, enabling the communication between MCU and pre-driver1)
 - »» FU7565Q1: 2*MCU I²Cs (where I²C2 is for internal use only, enabling the communication between MCU and

pre-driver1)

»» FU7574Q1: 1*6N pre-driver2 I²C, 2*MCU I²Cs (where I²C2 is for internal use only, enabling the communication between MCU and pre-driver1)

» 2*UARTs, supporting single-wire mode

» LIN

»» FU7512Q1: 1*LIN

»» FU7564Q1/FU7565Q1/FU7574Q1: 1*LIN, integrated with the LIN transceiver, supporting 12V LIN applications

» 1*CAN, supporting CANFD

» 1*BISS (available for FU7512Q1/FU7564Q1/FU7565Q1)

» 6-channel DMA: supporting data transmission via I²C/SPI/UART/LIN/DataMonitor (Communication interfaces vary according to different chip models. For details, see the above descriptions.)

> Analog peripherals

» 12-bit ADC, operating with 1μs conversion time and internal VREF or external VREF as reference voltage

» Number of channels in ADC1

»» FU7512Q1: 12 (Channels 3/11 in AD1 are for internal use only.)

»» FU7564Q1: 12 (Channels 0/1/3/4/11 in AD1 are for internal use only.)

»» FU7565Q1: 10 (Channels 0/1/3/4 in AD1 are for internal use only.)

»» FU7574Q1: 13 (Channels 0/1/4/11 in AD1 are for internal use only.)

» Number of channels in ADC2

»» FU7512Q1: 13 (Channels 0/1/4 in AD2 are for internal use only.)

»» FU7564Q1: 8 (Channels 1/3/4/13 in AD2 are for internal use only.)

»» FU7565Q1: 4 (Channel 13 in AD2 is for internal use only.)

»» FU7574Q1: 15 (Channels 0/1/4/13 in AD2 are for internal use only.)

» Number of channels in ADC3

»» FU7512Q1: 3 (Channel 2 in AD3 is for internal use only.)

»» FU7564Q1/FU7565Q1: None

»» FU7574Q1: 3 (Channel 2 in AD3 is for internal use only.)

» Internal VREF. 3V, 4V, 4.5V, or 5V can be selected as the internal reference

- » Internal VHALF, with VREF/2, 1/4 VREF, 1/8 VREF, or 25/64 VREF as the internal reference
- » Operational amplifiers, where PGA is configurable
 - » FU7512Q1: 7
 - » FU7564Q1: 4
 - » FU7564Q1: 3
 - » FU7574Q1: 7
- » Analog comparator
 - » FU7512Q1: 2 analog comparator groups and 6 independent analog comparators
 - » FU7564Q1: 2 analog comparator groups and 4 independent analog comparators
 - » FU7565Q1: 1 analog comparator group and 3 independent analog comparators
 - » FU7574Q1: 2 analog comparator groups and 6 independent analog comparators
- » DAC
 - » FU7512Q1: Dual-channel 9-bit, single-channel 8-bit, and dual-channel 6-bit (DAC0/4 are for internal use only.)
 - » FU7564Q1: Dual-channel 9-bit and dual-channel 6-bit (All are for internal use only.)
 - » FU7565Q1: Single-channel 9-bit and single-channel 6-bit (All are for internal use only.)
 - » FU7574Q1: Dual-channel 9-bit, dual-channel 6-bit, and single-channel 8-bit (DAC1/4 are for internal use only.)
- > Drive Type
 - » FU7512Q1: 2*PWM outputs
 - » FU7564Q1: 1*PWM output (PWM2) and 1*6N pre-driver output (6N pre-driver1)
 - » FU7565Q1: 1*6N pre-driver output (6N pre-driver1)
 - » FU7574Q1: 2*6N pre-driver outputs
- > Configurable OVP threshold VDS (available for FU7564Q1/FU7565Q1/FU7574Q1)
- > FOC module supports single-/dual-/triple-shunt current sampling (For FU7565Q1, FOC module supports single-/dual-shunt current sampling)
- > PFC (available for FU7512Q1/FU7574Q1)
 - » Full-automatic hardware
 - » ADC automatic sampling
 - » Over-current protection and cycle-by-cycle current limiting

- >> Interleaved two-phase boost PFC
- > System clock
 - >> Built-in 24MHz high-speed RC oscillator
 - >> Built-in 32.8kHz low-speed RC oscillator
 - >> 12MHz external crystal clock
 - >> IWDT
 - >> WWDT
- > Level change wake-up via MON_HVx pin (available for FU7564Q1/FU7565Q1/FU7574Q1)
- > LVD
- > Temperature sensor
- > Two-wire FICE protocol based in-circuit emulation

1.2 Applications

The chip can be used to drive sensorless or sensed BLDC motors/PMSM, single-phase/three-phase induction motors and servo motors.

- > FU7512Q1 is designed for a wide range of motor control applications in automotive systems, including thermal management compressors, fans, pumps, refrigerators, blowers, seats, wipers, seat ventilation systems, sunroofs, power windows, etc.
- > FU7564Q1 is designed for a wide range of motor control applications in automotive systems, including fans, pumps, valves, refrigerators, blowers, seats, active grille shutters (AGS), wipers, seat ventilation systems, sunroofs, power windows, A/C outlets, etc.
- > FU7565Q1 is designed for a wide range of motor control applications in automotive systems, including fans, oil pumps, water pumps, valves, seats, seat ventilation systems, flip/rotating screens, dimmable sunroof/window glass, wipers, sunroofs, panoramic sunroofs, sunshades, windows, refrigerators, on-board oxygen generators, suspension air compressors, etc.
- > FU7574Q1 is designed for a wide range of motor control applications in automotive systems, including fans, electric pumps, valves, seats, seat ventilation systems, A/C outlets, damper actuators, active grille

shutters (AGS), flip/rotating screens, dimmable sunroof/window glass, wipers, sunroofs, panoramic sunroofs, sunshades, windows, refrigerators, on-board oxygen generators, etc.

1.3 Overview

FU7512_64_65_74Q1 is a high-performance motor drive chip that incorporates ME core and RISC-V core. ME core integrates FOC module and CORDIC module that allow for automatic calculation of FOC or square-wave control by the hardware for sensored/sensorless BLDC/PMSM motors. RISC-V core is used for parameter configuration and routine processing. The dual cores work in parallel to achieve high-performance motor control. The chip integrates high-speed operational amplifiers, comparators, high-speed ADC, CRC, SPI, I²C, UART, LIN, CANFD, DataMonitor, Timers, and built-in LDO, which are suitable for FOC or square-wave based BLDC/PMSM motors.

The above are the general descriptions on the product family. The features vary by models. For details, see chapters 2 Pin Definitions and 4 Ordering Information.

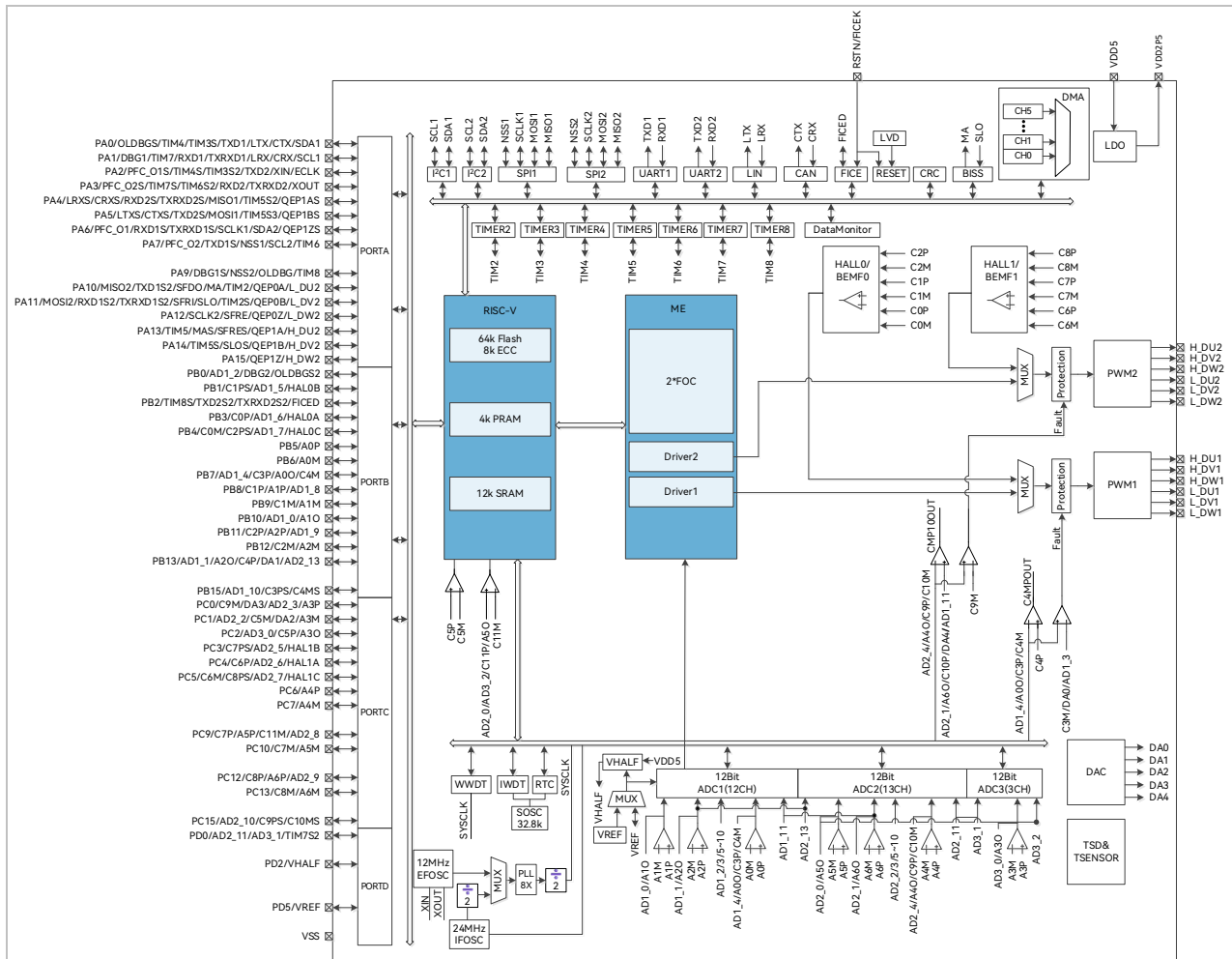
For concise description and easy differentiation, if it is specified that a feature is applied to a specific model, the feature is exclusive to this model. Otherwise, the feature is a common feature of the product family.

- FU7512Q1 and FU7564Q1 adopt the QFN56 package.
- FU7565Q1 adopts the QFN48 package.
- FU7574Q1 adopts the QFN88 package.

1.4 Functional Block Diagram

1.4.1 FU7512Q1

Figure 1-1 Functional Block Diagram of FU7512Q1



1.4.2 FU7564Q1

Figure 1-2 Functional Block Diagram of FU7564Q1

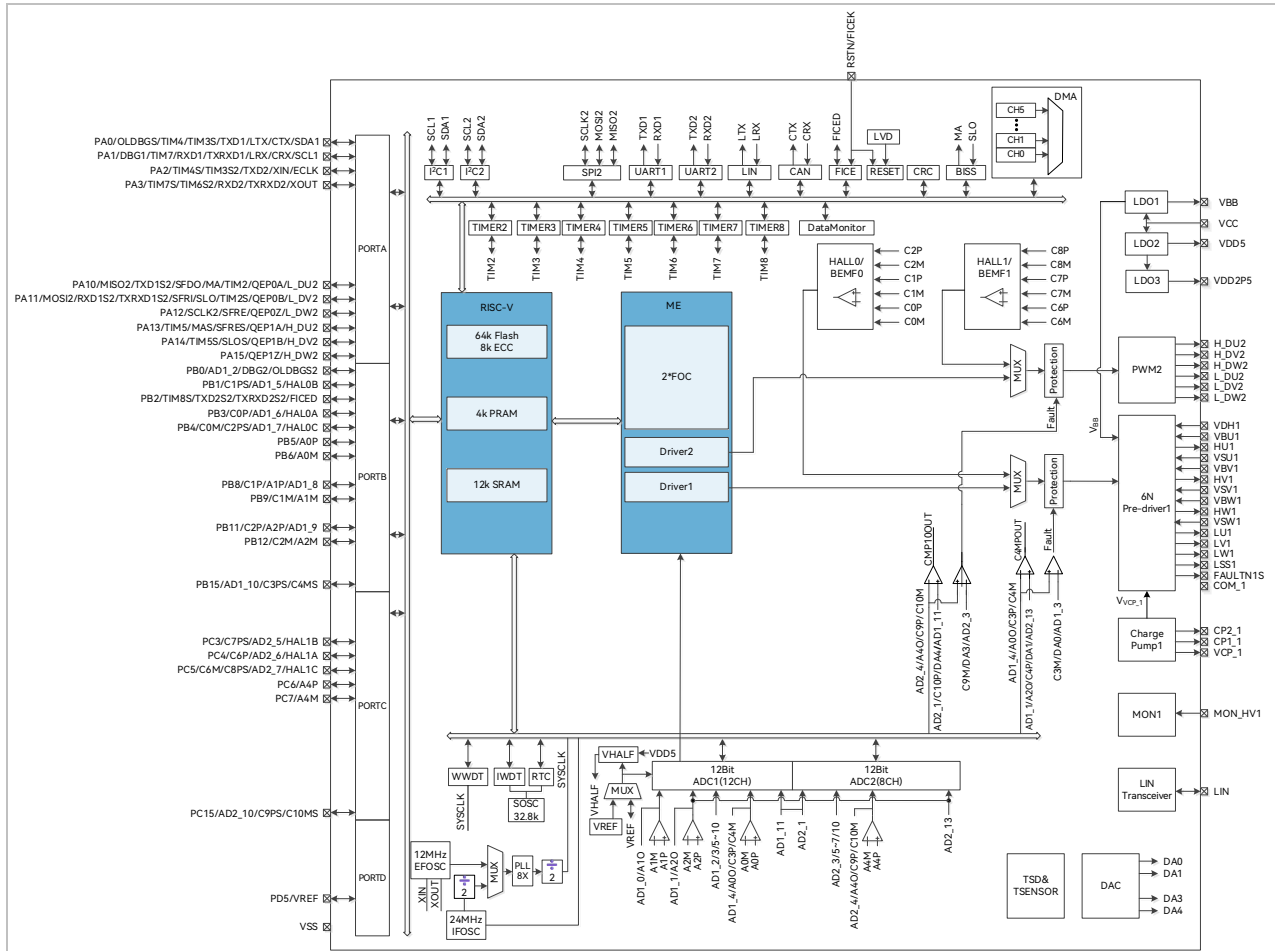
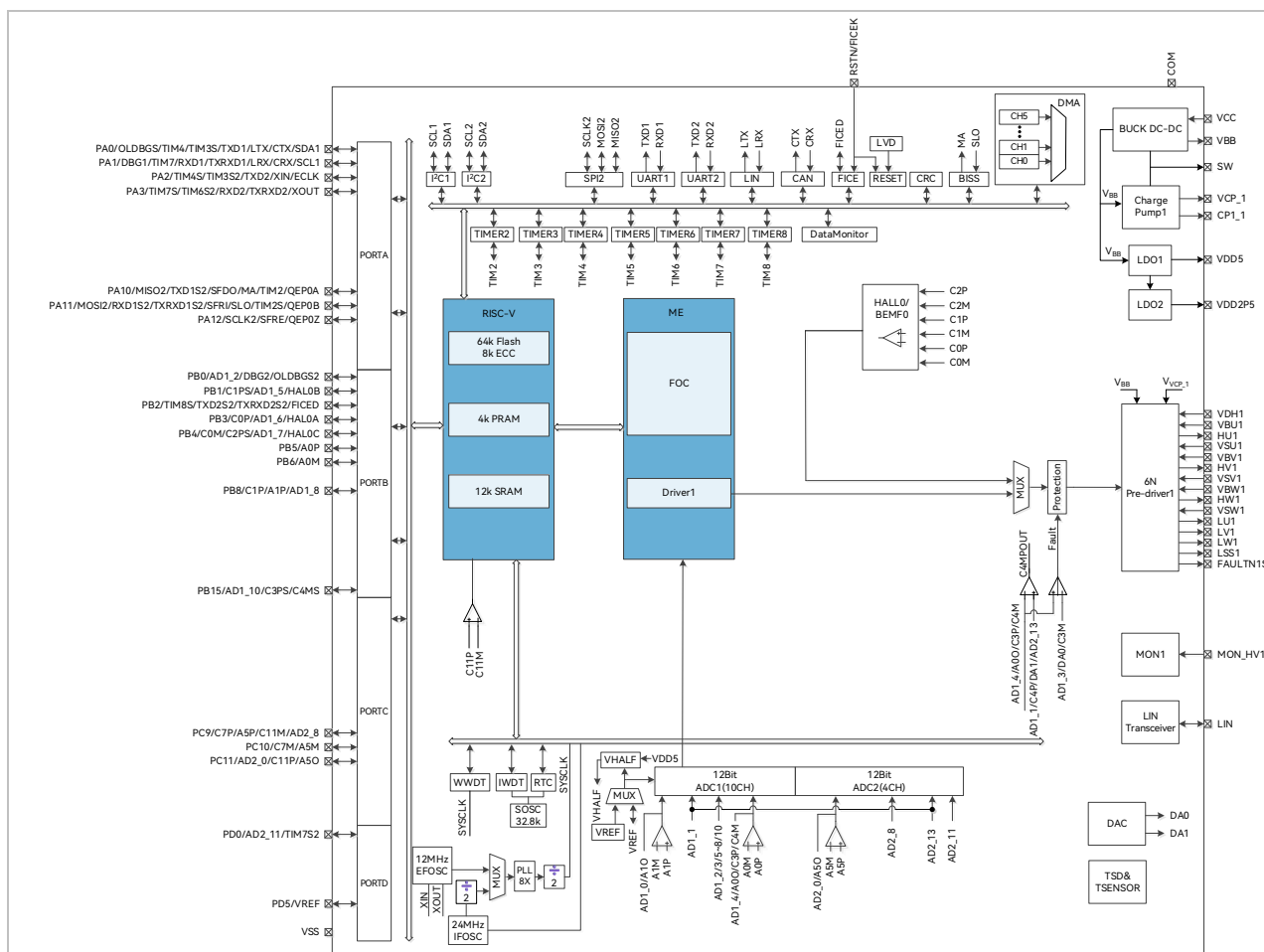
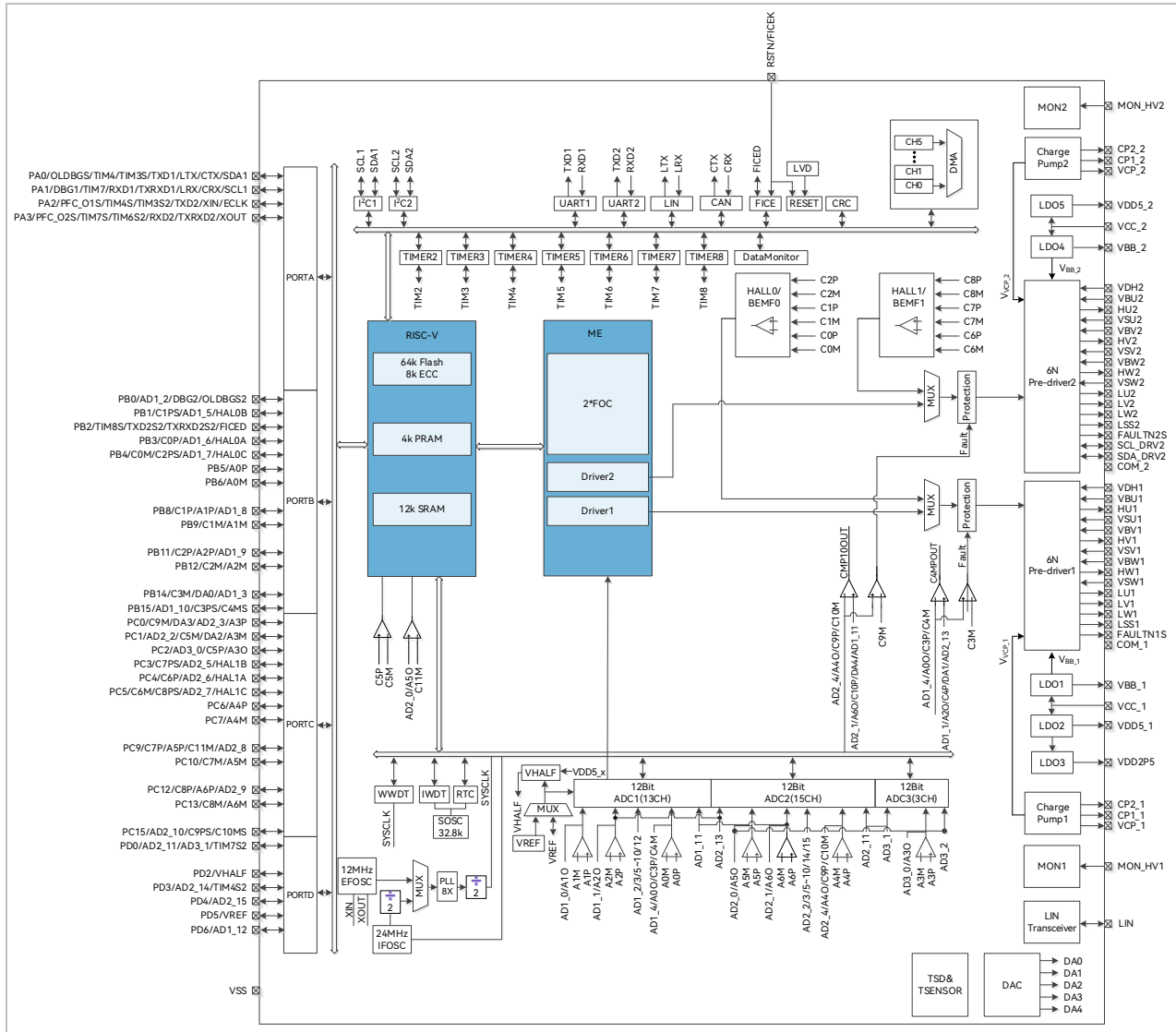


Figure 1-3 Functional Block Diagram of FU7565Q1



1.4.4 FU7574Q1

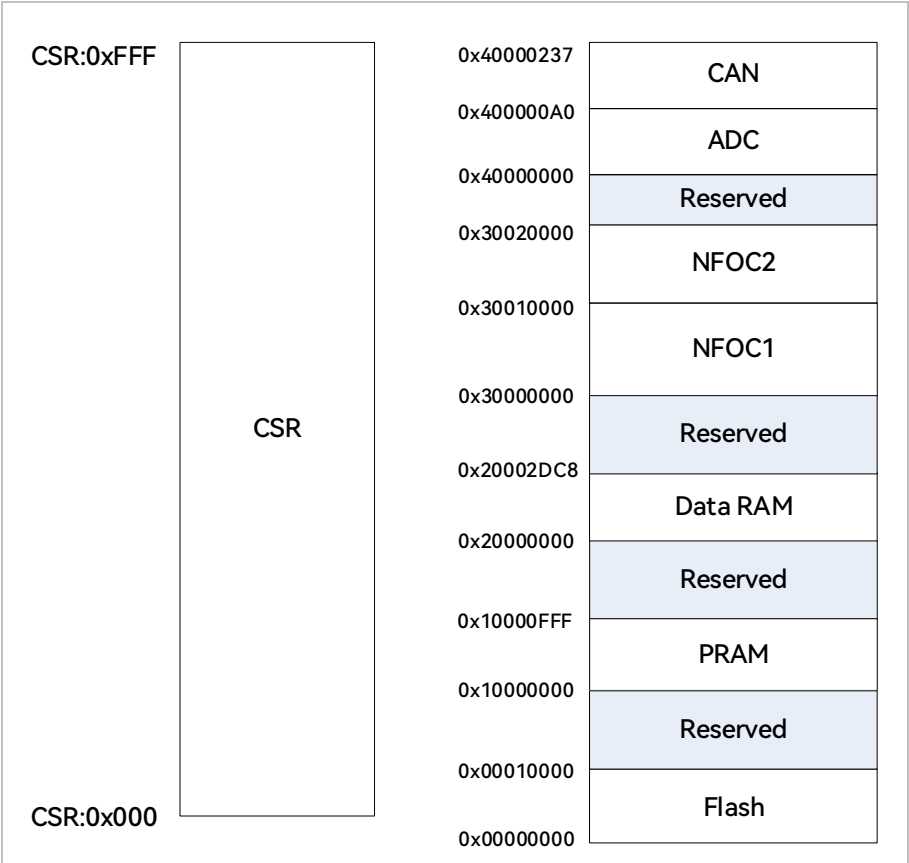
Figure 1-4 Functional Block Diagram of FU7574Q1



1.5 Memory Organization

The MCU internal storage space is divided into Program Memory and Data Memory, which are independently addressed.

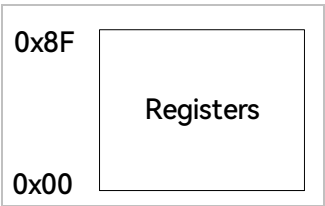
Figure 1-5 Memory Organization



For FU7564Q1 and FU7565Q1, their 6N pre-driver1 registers are mapped to the address range 0x00 ~ 0x8F, and are accessed via its I²C2 in the MCU.

For FU7574Q1, both its 6N pre-driver1 and 6N pre-driver2 registers are mapped to the address range 0x00 ~ 0x8F; its 6N pre-driver1 register is accessed via its I²C2 in the MCU, while its 6N pre-driver2 register is accessed via the I²C outside 6N pre-driver2.

Figure 1-6 FU7564Q1/FU7565Q1/FU7574Q1 6N Pre-driverx Register Address Mapping



1.5.1 CSR Memory

CSR (Control and Status Registers) is a group of special registers in RISC-V for controlling and managing processors. The CSR register provides programming access to both internal processor functions and external systems. In the RISC-V architecture, six instructions — CSRRW, CSRRS, CSRRC, CSRRWI, CSRRSI and CSRRCI — can be used to read, write and modify values in CSR registers.

1.5.2 Flash

The chip implements this program memory as Flash memory with a block from addresses 0x00000000 to 0x0000FFFF to store control programs. The sector 0x00000000 ~ 0x0000007F is the interrupt vector address area, which is used to store the start address of each interrupt subroutine. The last sector 0x0000FF00 ~ 0x0000FFFF contains internal control bits of the chip.

1.5.3 Peripheral Memory

The peripheral memory stores data related to peripheral modules. It comprises NFOC (0x30000000 ~ 0x3001FFFF), ADC1 result memory area (0x40000040 ~ 0x4000005F), ADC2 result memory area (0x40000060 ~ 0x4000007F), and CAN message data store area (0x400000A0 ~ 0x40000237).

1.5.4 Data Memory

The data memory stores user variables and related data. It is addressed from 0x20000000 ~ 0x20002DC7, as shown in Figure 1-5.

1.5.5 Address Mapping

1.5.5.1 CSR Address Mapping

Table 1-1 CSR Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x000	PA	PA_OE	PA_PU	PA_PL				
0x008	RSV							
0x010	PB	PB_OE	PB_PU	PB_AN				
0x018	RSV							
0x020	PC	PC_OE	PC_PU	PC_AN				
0x028	RSV							
0x030	PD	PD_OE	PD_PU	PD_AN				
0x038~ 0x058	RSV							
0x060	PH_SEL	PH_SEL1						

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x068~ 0x078	RSV							
0x080	CK_CR							
0x088~ 0x098	RSV							
0x0A0	DMA0_CR	DMA0_LEN	DMA0_BA					
0x0A8	RSV							
0x0B0	DMA1_CR	DMA1_LEN	DMA1_BA					
0x0B8	RSV							
0x0C0	DMA2_CR	DMA2_LEN	DMA2_BA					
0x0C8	RSV							
0x0D0	DMA3_CR	DMA3_LEN	DMA3_BA					
0x0D8	RSV							
0x0E0	DMA4_CR	DMA4_LEN	DMA4_BA					
0x0E8	RSV							
0x0F0	DMA5_CR	DMA5_LEN	DMA5_BA					
0x0F8~ 0x138	RSV							
0x140	UT1_CR0	UT1_CR1	UT1_DR	UT1_BAUD	SF_CR	SF_SR	SF_BAUD	
0x148	RSV							
0x150	UT2_CR0	UT2_CR1	UT2_DR	UT2_BAUD				
0x158	RSV							
0x160	I2C1_CR	I2C1_ID	I2C1_DR	I2C1_SR	I2C1_BAUD			
0x168	RSV							
0x170	I2C2_CR	I2C2_ID	I2C2_DR	I2C2_SR	I2C2_BAUD			
0x178	RSV							
0x180	SPI1_CR	SPI1_SR	SPI1_CLK	SPI1_DR				
0x188	RSV							
0x190	SPI2_CR	SPI2_SR	SPI2_CLK	SPI2_DR				
0x198	RSV							
0x1A0	LIN_CR	LIN_SR	LIN_CSR	LIN_ID	LIN_SIZE	LIN_BAUD	LIN_IDLECNT	LIN_BRKCNT
0x1A8~ 0x1B8	RSV							
0x1C0	CAN_CR0	CAN_CR1	CAN_STS	CAN_IER	CAN_IFR	CAN_TSPT	CAN_NBTR	CAN_DBTR
0x1C8	CAN_TDCR	CAN_ACR	CAN_AMR	CAN_ERR	CAN_ERLIM	CAN_TMSTA	CAN_TMID0	CAN_TMDT0
0x1D0	CAN_TMID1	CAN_TMDT1	CAN_TMID2	CAN_TMDT2				
0x1D8	CRC_DIN	CRC_CR	CRC_DR	CRC_BEG	CRC_CNT			
0x1E0~ 0x208	RSV							
0x210	TIM2_CR0	TIM2_CR1	TIM2_IER	TIM2_SR	TIM2_CNTR	TIM2_DR	TIM2_ARR	TIM2_QEP_M NUM
0x218	TIM2_QEP_ TNUM	TIM2_QEP_ TS_EMP	TIM2_QEP_ CNTR	TIM2_QEP_ ARR	TIM2_CR2			
0x220	TIM3_CR0	TIM3_CR1	TIM3_IER	TIM3_SR	TIM3_CNTR	TIM3_DR	TIM3_ARR	
0x228	RSV							
0x230	TIM4_CR0	TIM4_CR1	TIM4_IER	TIM4_SR	TIM4_CNTR	TIM4_DR	TIM4_ARR	
0x238	RSV							
0x240	TIM5_CR0	TIM5_CR1	TIM5_IER	TIM5_SR	TIM5_CNTR	TIM5_DR	TIM5_ARR	TIM5_QEP_M NUM
0x248	TIM5_QEP_ TNUM	TIM5_QEP_ TS_EMP	TIM5_QEP_ CNTR	TIM5_QEP_ ARR	TIM5_CR2			

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x250	TIM6_CR0	TIM6_CR1	TIM6_IER	TIM6_SR	TIM6_CNTR	TIM6_DR	TIM6_ARR	TIM6_QEP_M NUM
0x258	TIM6_QEP_ TNUM	TIM6_QEP_ TS_EMP	TIM6_QEP_ CNTR	TIM6_QEP_ ARR	TIM6_CR2			
0x260	TIM7_CR0	TIM7_CR1	TIM7_IER	TIM7_SR	TIM7_CNTR	TIM7_DR	TIM7_ARR	
0x268	RSV							
0x270	TIM8_CR0	TIM8_CR1	TIM8_IER	TIM8_SR	TIM8_CNTR	TIM8_DR	TIM8_ARR	
0x278 ~ 0x2F8	RSV							
0x300	MIE					MTVEC		
0x308~ 0x338	RSV							
0x340		MEPC	MCAUSE					
0x348 ~ 0x3F8	RSV							
0x400	PIE	EXTIOIE	EXTI1IE	EXTI2IE	EXTIOIF	EXTI1IF	EXTI2IF	EXTI_TCON
0x408	LVSR	IP0	IP1	IP2	IP3	IP4	IP5	IP6
0x410	IP7	IP8	IP9	IP10	IP11	IP12	IP13	IP14
0x418	IP15	IP16	IP17	IP18	IP19	IP20	IP21	IP22
0x420	IP23	IP24	IP25	IP26	IP27	IP28	IP29	IP30
0x428	IP31							
0x430~ 0x438	RSV							
0x440	SYST_ARR	SYST_SR						
0x448~ 0x458	RSV							
0x460	RTC_CR	RTC_DR	CAL_CR	OSC_CR	OSC_SR			
0x468~ 0x478	RSV							
0x480	IWDT_KR	IWDT_REL						
0x488~ 0x498	RSV							
0x4A0	WWDTCR	WWDTCFR	WWDTCR					
0x4A8~ 0x4C8	RSV							
0x4D0	RST_SR	RST_CR	PCON					
0x4D8	RSV							
0x4E0	FLA_KEY	FLA_CR	FLA_ECSR	FLA_EEADR				
0x4E8~ 0x4F8	RSV							
0x500	ME_CR							
0x508					ME_COR			
0x510~ 0x538	RSV							
0x540	DRV1_CR	DRV1_OUT	DRV1_IER	DRV1_IFR	DRV1_PER	DRV1_PTR	DRV1_PSR	DRV1_CMR
0x548	DRV1_FCR0	DRV1_FCR1	DRV1_FCR2	DRV1_FCR3	DRV1_FCR4	DRV1_FCR5	DRV1_FCR6	DRV1_FCR7
0x550	DRV1_ARR	DRV1_DR	DRV1_ COMR	DRV1_DTR	DRV1_ CMPU1	DRV1_ CMPD1	DRV1_ CMPU2	DRV1_ CMPD2
0x558	DRV1_ CMPU3	DRV1_ CMPD3	DRV1_CNTR	DRV1_TRG1	DRV1_TRG2	DRV1_COMU R	DRV1_COMD R	DRV1_ARRS H
0x560~	RSV							

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x578								
0x580	DRV2_CR	DRV2_OUT	DRV2_IER	DRV2_IFR	DRV2_PER	DRV2_PTR	DRV2_PSR	DRV2_CMR
0x588	DRV2_FCR0	DRV2_FCR1	DRV2_FCR2	DRV2_FCR3	DRV2_FCR4	DRV2_FCR5	DRV2_FCR6	DRV2_FCR7
0x590	DRV2_ARR	DRV2_DR	DRV2_COMR	DRV2_DTR	DRV2_CMPU1	DRV2_CMPD1	DRV2_CMPU2	DRV2_CMPD2
0x598	DRV2_CMPU3	DRV2_CMPD3	DRV2_CNTR	DRV2_TRG1	DRV2_TRG2	DRV2_COMU R	DRV2_COMD R	DRV2_ARRS H
0x5A0~ 0x5B8	RSV							
0x5C0	PFC_CR0	PFC_CR1	PFC_CR2	PFC_KM	UAC_CSO	IAC1_CSO	IAC2_CSO	PFC_ARR
0x5C8	PFC_DR1	PFC_DR2	UDC_ARR	PFC_TRGDLY	UDC_REF	UDC_UK	UDC_KP	UDC_KI
0x5D0	UDC_UKMAX	UDC_UKMIN	IAC1_REF	IAC1_UK	IAC1_KP	IAC1_KI	IAC1_UKMAX	IAC1_UKMIN
0x5D8	IAC2_REF	IAC2_UK	IAC2_KP	IAC2_KI	IAC2_UKMAX	IAC2_UKMIN	PFC_UAC	PFC_IAC1
0x5E0	PFC_IAC2	PFC_UDC	PFC_UAVG	PFC_COM	PFC_KCOM	PFC_DDCM		PFC_KDDCM
0x5E8	PFC_DCCMC SO	PFC_KIAC1	PFC_KIAC2					
0x5F0~ 0x5F8	RSV							
0x600	CMP_CR0	CMP_CR1	CMP_CR2	CMP_CR3	CMP_SR	CMP_IFR	CMP_SAMR	CMP_DBR
0x608	CMP_CR4	CMP_CR5	CMP_CR6					
0x610~ 0x618	RSV							
0x620	VREF_VHALF_CR	AMP_CR0	AMP_CR1					
0x628	RSV							
0x630	TSD_CR	TSEN_DR						
0x638	RSV							
0x640	DAC_CR	DAC_DR0	DAC_DR1	DAC_DR2	DAC_DR3	DAC_DR4		
0x648~ 0x658	RSV							
0x660	ADC1_CR	ADC1_MASK	ADC1_SCYC					
0x668	RSV							
0x670	ADC2_CR	ADC2_MASK	ADC2_SCYC					
0x678	RSV							
0x680	ADC3_CR	ADC3_MASK	ADC3_SCYC	ADC3_DR0	ADC3_DR1	ADC3_DR2		
0x688	RSV							
0x690~ 0x6F8	RSV							
0x700	BISS_CLK_CNT	BISS_OVER TIME_CNT	BISS_DATA_L EN	BISS_STATE	BISS_S DATAL	BISS_S DATAH		
0x708~ 0xFF0	RSV							
0xFF8					CCFG3	CCFG2		

1.5.5.2 Peripheral Address Mapping

1.5.5.2.1 ADC Address Mapping

Table 1-2 ADC Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x40000000~ 0x40000038	RSV							
0x40000040	ADC1_DR0	ADC1_DR1	ADC1_DR2	ADC1_DR3	ADC1_DR4	ADC1_DR5	ADC1_DR6	ADC1_DR7
0x40000048	ADC1_DR8	ADC1_DR9	ADC1_DR10	ADC1_DR11	ADC1_DR12			
0x40000050~ 0x40000058	RSV							
0x40000060	ADC2_DR0	ADC2_DR1	ADC2_DR2	ADC2_DR3	ADC2_DR4	ADC2_DR5	ADC2_DR6	ADC2_DR7
0x40000068	ADC2_DR8	ADC2_DR9	ADC2_DR10	ADC2_DR11		ADC2_DR13	ADC2_DR14	
0x40000070~ 0x40000098	RSV							

1.5.5.2.2 CAN Address Mapping

Table 1-3 CAN Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x400000A0	CAN_TX0DA0				CAN_TX0DA1			
0x400000A8	CAN_TX0DA2				CAN_TX0DA3			
0x400000B0	CAN_TX0DA4				CAN_TX0DA5			
0x400000B8	CAN_TX0DA6				CAN_TX0DA7			
0x400000C0	CAN_TX0DA8				CAN_TX0DA9			
0x400000C8	CAN_TX0DA10				CAN_TX0DA11			
0x400000D0	CAN_TX0DA12				CAN_TX0DA13			
0x400000D8	CAN_TX0DA14				CAN_TX0DA15			

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x40000E0		CAN_TX1DA0				CAN_TX1DA1		
0x40000E8		CAN_TX1DA2				CAN_TX1DA3		
0x40000F0		CAN_TX1DA4				CAN_TX1DA5		
0x40000F8		CAN_TX1DA6				CAN_TX1DA7		
0x4000100		CAN_TX1DA8				CAN_TX1DA9		
0x4000108		CAN_TX1DA10				CAN_TX1DA11		
0x4000110		CAN_TX1DA12				CAN_TX1DA13		
0x4000118		CAN_TX1DA14				CAN_TX1DA15		
0x4000120		CAN_TX2DA0				CAN_TX2DA1		
0x4000128		CAN_TX2DA2				CAN_TX2DA3		
0x4000130		CAN_TX2DA4				CAN_TX2DA5		
0x4000138		CAN_TX2DA6				CAN_TX2DA7		
0x4000140		CAN_TX2DA8				CAN_TX2DA9		
0x4000148		CAN_TX2DA10				CAN_TX2DA11		
0x4000150		CAN_TX2DA12				CAN_TX2DA13		
0x4000158		CAN_TX2DA14				CAN_TX2DA15		
0x4000160		CAN_RX0ID				CAN_RX0TD		
0x4000168		CAN_RX0DA0				CAN_RX0DA1		
0x4000170		CAN_RX0DA2				CAN_RX0DA3		
0x4000178		CAN_RX0DA4				CAN_RX0DA5		
0x4000180		CAN_RX0DA6				CAN_RX0DA7		
0x4000188		CAN_RX0DA8				CAN_RX0DA9		
0x4000190		CAN_RX0DA10				CAN_RX0DA11		
0x4000198		CAN_RX0DA12				CAN_RX0DA13		
0x40001A0		CAN_RX0DA14				CAN_RX0DA15		
0x40001A8		CAN_RX1ID				CAN_RX1TD		
0x40001B0		CAN_RX1DA0				CAN_RX1DA1		
0x40001B8		CAN_RX1DA2				CAN_RX1DA3		

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x400001C0	CAN_RX1DA4				CAN_RX1DA5			
0x400001C8	CAN_RX1DA6				CAN_RX1DA7			
0x400001D0	CAN_RX1DA8				CAN_RX1DA9			
0x400001D8	CAN_RX1DA10				CAN_RX1DA11			
0x400001E0	CAN_RX1DA12				CAN_RX1DA13			
0x400001E8	CAN_RX1DA14				CAN_RX1DA15			
0x400001F0	CAN_RX2ID				CAN_RX2TD			
0x400001F8	CAN_RX2DA0				CAN_RX2DA1			
0x40000200	CAN_RX2DA2				CAN_RX2DA3			
0x40000208	CAN_RX2DA4				CAN_RX2DA5			
0x40000210	CAN_RX2DA6				CAN_RX2DA7			
0x40000218	CAN_RX2DA8				CAN_RX2DA9			
0x40000220	CAN_RX2DA10				CAN_RX2DA11			
0x40000228	CAN_RX2DA12				CAN_RX2DA13			
0x40000230	CAN_RX2DA14				CAN_RX2DA15			

1.5.5.2.3 NFOC1 Address Mapping

Table 1-4 NFOC1 Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30000000	NFOC1_UDC		NFOC1_UDCK		NFOC1_UDCFLT			
0x30000008	NFOC1_IAREF		NFOC1_IBREF		NFOC1_ICREF		NFOC1_ITREF	
0x30000010	NFOC1_IRLOW		NFOC1_IRUPP		NFOC1_OVP		NFOC1_OVPARR	NFOC1_OVPCNT
0x30000018	NFOC1_UVP		NFOC1_UVPARR	NFOC1_UVPCNT	NFOC1_SOCP		NFOC1_SOCPARR	NFOC1_SOCPCNT
0x30000020	NFOC1_LKSMIN		NFOC1_LKSMAX		NFOC1_LOCKK		RSV	
0x30000028	NFOC1_LKARR		NFOC1_LKCNT		NFOC1_NCURRE		NFOC1_PLK	
0x30000030	NFOC1_XI0		NFOC1_YI0		RSV		NFOC1_THETA0	
0x30000038	NFOC1_XO0		NFOC1_YO0		NFOC1_XI1		NFOC1_YI1	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30000040	RSV		NFOC1_THETA1		NFOC1_XO1		NFOC1_YO1	
0x30000048	NFOC1_XI2		NFOC1_YI2		NFOC1_US2		NFOC1_THETA2	
0x30000050	NFOC1_XI3		NFOC1_YI3		NFOC1_US3		NFOC1_THETA3	
0x30000058 ~ 0x30000098	RSV							
0x300000A0	RSV				NFOC1_UDCALP		NFOC1_UDCBET	
0x300000A8 ~ 0x300000B0	RSV							
0x300000B8	RSV				NFOC1_FEK7		NFOC1_FEK8	
0x300000C0	NFOC1_AFKP		NFOC1_AFKI		NFOC1_AFMAX		NFOC1_AFMIN	
0x300000C8	NFOC1_AFEK		NFOC1_AFEK1		NFOC1_AFUK			
0x300000D0	RSV				NFOC1_ITFLT			
0x300000D8	NFOC1_ITRIP		NFOC1_POWER		NFOC1_US		NFOC1_UTHETA	
0x300000E0	NFOC1_HKP		NFOC1_HKI		NFOC1_HMAX		NFOC1_HMIN	
0x300000E8	NFOC1_HEK		NFOC1_HEK1		NFOC1_HUK			
0x300000F0	RSV				NFOC1_ID0		NFOC1_IQ0	
0x300000F8	RSV				NFOC1_HALPHA		NFOC1_HBETA	
0x30000100	NFOC1_DKP		NFOC1_DKI		NFOC1_DMAX		NFOC1_DMIN	
0x30000108	NFOC1_DEK		NFOC1_DEK1		NFOC1_DUK			
0x30000110	NFOC1_CVDUK		NFOC1_CVKI2D		NFOC1_HS		NFOC1_HTHETA	
0x30000118	NFOC1_UALORG		NFOC1_UBEORG		RSV		NFOC1_HTCOM	
0x30000120	NFOC1_QKP		NFOC1_QKI		NFOC1_QMAX		NFOC1_QMIN	
0x30000128	NFOC1_QEK		NFOC1_QEK1		NFOC1_QUK			
0x30000130	NFOC1_CVQUK		NFOC1_CVKI2Q		NFOC1_IALPHA		NFOC1_IBETA	
0x30000138	NFOC1_ID		NFOC1_IQ		NFOC1_IDFLT			
0x30000140	NFOC1_EKP		NFOC1_EKI		NFOC1_EMAX		NFOC1_EMIN	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30000148	NFOC1_EEK		NFOC1_EEK1		NFOC1_EUK			
0x30000150	RSV				NFOC1_IQFLT			
0x30000158	NFOC1_THETA				NFOC1_EALPHA			
					NFOC1_AFRPAH			
0x30000160	NFOC1_WKP		NFOC1_WKI		NFOC1_WMAX		NFOC1_WMIN	
0x30000168	NFOC1_WEK		NFOC1_WEK1		NFOC1_WUK			
0x30000170	RSV				NFOC1_AFRPBH			
					NFOC1_EBETA			
0x30000178	NFOC1_ETHERA				NFOC1_ZALORG		NFOC1_ZBEORG	
					NFOC1_AFKDF		NFOC1_AFKAF	
0x30000180	NFOC1_FWKP		NFOC1_FWKI		NFOC1_FWMAX		NFOC1_FWMIN	
0x30000188	NFOC1_FWEK		NFOC1_FWEK1		NFOC1_FWUK			
0x30000190	RSV		NFOC1_KUSF		NFOC1_OMEACC			
0x30000198	NFOC1_OMEEND				NFOC1_OMEMIN		NFOC1_FTCK	
0x300001A0	NFOC1_FBASE		NFOC1_OMEMI2		NFOC1_THECOM		NFOC1_FTCOM	
0x300001A8	NFOC1_EK1		NFOC1_EK2		NFOC1_EK3		NFOC1_EK4	
0x300001B0	NFOC1_FEK5				NFOC1_MERRRE		NFOC1_TDTC	
					NFOC1_FEK6			
0x300001B8	NFOC1_IDREF		NFOC1_IQREF		NFOC1_I1		NFOC1_I2	
0x300001C0	NFOC1_IA		NFOC1_IB		NFOC1_IC		NFOC1_ICMAX	
0x300001C8	NFOC1_IAMAX		NFOC1_IBMAX		NFOC1_UDCPS		NFOC1_UQCPS	
0x300001D0	NFOC1_WREF		NFOC1_WFDB		NFOC1_ITK		NFOC1_POWK1	NFOC1_POWK2
0x300001D8	NFOC1_FGBASE		RSV		NFOC1_UALCPS		NFOC1_UBECPS	
0x300001E0	NFOC1_EMF		NFOC1_ATHETA		NFOC1_RATAR		NFOC1_RAOUT	
0x300001E8	NFOC1_RAINC		NFOC1_RADEC		NFOC1_LK1		NFOC1_LK2	
0x300001F0	NFOC1_LK3		NFOC1_LK4		NFOC1_LK5		NFOC1_LK6	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x300001F8	NFOC1_LED		NFOC1_LEQ		NFOC1_LOME			
0x30000200	RSV				NFOC1_OMEGA		RSV	
0x30000208	NFOC1_IESTA		NFOC1_IESTB		NFOC1_OMEFLT			
0x30000210	NFOC1_OMEFL2				NFOC1_ZALPHA		NFOC1_ZBETA	
0x30000218	NFOC1_KLPF		NFOC1_FUWEI		NFOC1_UDFIN		NFOC1_UQFIN	
0x30000220	NFOC1_UALPHA		NFOC1_UBETA		RSV			
0x30000228 ~ 0x30000230	RSV							
0x30000238	NFOC1_UIK0		NFOC1_UIK1		NFOC1_UIK2		NFOC1_UIK3	
0x30000240	NFOC1_UITC0		NFOC1_UIUS0		NFOC1_UITC1		NFOC1_UIUS1	
0x30000248	NFOC1_UITC2		NFOC1_UIUS2		NFOC1_UITC3		NFOC1_UIUS3	
0x30000250	NFOC1_TRG1		NFOC1_TRG2		NFOC1_AFTHE			
0x30000258	NFOC1_OTHETA				NFOC1_USOMEK		NFOC1_UA	
0x30000260	NFOC1_UB		NFOC1_UC		NFOC1_USK		NFOC1_USOUS	
0x30000268	NFOC1_FTCPS		NFOC1_FTHETA		RSV			
0x30000270	RSV				NFOC1_FWREF		NFOC1_CMRSH	
0x30000278	NFOC1_TS		NFOC1_NTS		NFOC1_TDLY		NFOC1_TDLYD	
0x30000280	NFOC1_ARR		RSV		NFOC1_IDK		NFOC1_IQK	
0x30000288	NFOC1_OMEGAK		NFOC1_OMEK2		NFOC1_DELOTHE			
0x30000290	NFOC1_DELETHE				NFOC1_UDCD		NFOC1_UDCQ	
0x30000298 ~ 0x300002F8	RSV							
0x30000300	RSV		NFOC1_CVDULO		RSV			
0x30000308 ~ 0x30000320	RSV							
0x30000328	RSV		NFOC1_CVQULO		RSV			
0x30000330	RSV							

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30000338	RSV				NFOC1_WUCPS		NFOC1_WUFIN	
0x30000340 ~ 0x30000368	RSV							
0x30000370	NFOC1_UDK		NFOC1_UQK		NFOC1_UDFLT			
0x30000378	NFOC1_UQFLT				NFOC1_FWIDR		NFOC1_OSCNT	
0x30000380	NFOC1_OSSUM				RSV			
0x30000388	RSV				NFOC1_OMUNIT		NFOC1_CSAM	
0x30000390 ~ 0x300003A8	RSV						NFOC1_DLYCNT	
0x300003B0	RSV						NFOC1_IDRLIM	
0x300003B8 ~ 0x300003C0	RSV							
0x300003C8	RSV				NFOC1_CVK1		NFOC1_CVK3	
0x300003D0	NFOC1_CVDK4		NFOC1_CVQK4		NFOC1_CVDK5		NFOC1_CVQK5	
0x300003D8	NFOC1_DCOM		NFOC1_DAS		NFOC1_QCOM		NFOC1_QAS	
0x300003E0	NFOC1_CVK2		NFOC1_UDCLIM		NFOC1_UDCMAX		NFOC1_UDCMIN	
0x300003E8	NFOC1_FUMAX		NFOC1_FUMIN		NFOC1_IS		NFOC1_ITHETA	
0x300003F0	NFOC1_USFLT				NFOC1_DUKF		NFOC1_QUKF	
0x300003F8	RSV				NFOC1_UDCPS1		NFOC1_UQCPS1	

1.5.5.2.4 NFOC2 Address Mapping

Table 1-5 NFOC2 Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30010000	NFOC2_UDC		NFOC2_UDCK		NFOC2_UDCFLT			
0x30010008	NFOC2_IAREF		NFOC2_IBREF		NFOC2_ICREF		NFOC2_ITREF	
0x30010010	NFOC2_IRLOW		NFOC2_IRUPP		NFOC2_OVP		NFOC2_OVPARR	NFOC2_OVPCNT

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30010018	NFOC2_UVP		NFOC2_UVPARR	NFOC2_UVPCNT	NFOC2_SOCP		NFOC2_SOCPARR	NFOC2_SOCPCNT
0x30010020	NFOC2_LKSMIN		NFOC2_LKSMAX		NFOC2_LOCKK		RSV	
0x30010028	NFOC2_LKARR		NFOC2_LKCNT		NFOC2_NCURRE		NFOC2_PLK	
0x30010030	NFOC2_XI0		NFOC2_YI0		RSV		NFOC2_THETA0	
0x30010038	NFOC2_XO0		NFOC2_YO0		NFOC2_XI1		NFOC2_YI1	
0x30010040	RSV		NFOC2_THETA1		NFOC2_XO1		NFOC2_YO1	
0x30010048	NFOC2_XI2		NFOC2_YI2		NFOC2_US2		NFOC2_THETA2	
0x30010050	NFOC2_XI3		NFOC2_YI3		NFOC2_US3		NFOC2_THETA3	
0x30010058 ~ 0x30010098	RSV							
0x300100A0	RSV				NFOC2_UDCALP		NFOC2_UDCBET	
0x300100A8 ~ 0x300100B0	RSV							
0x300100B8	RSV				NFOC2_FEK7		NFOC2_FEK8	
0x300100C0	NFOC2_AFKP		NFOC2_AFKI		NFOC2_AFMAX		NFOC2_AFMIN	
0x300100C8	NFOC2_AFEK		NFOC2_AFEK1		NFOC2_AFUK			
0x300100D0	RSV				NFOC2_ITFLT			
0x300100D8	NFOC2_ITRIP		NFOC2_POWER		NFOC2_US		NFOC2_UTHETA	
0x300100E0	NFOC2_HKP		NFOC2_HKI		NFOC2_HMAX		NFOC2_HMIN	
0x300100E8	NFOC2_HEK		NFOC2_HEK1		NFOC2_HUK			
0x300100F0	RSV				NFOC2_ID0		NFOC2_IQ0	
0x300100F8	RSV				NFOC2_HALPHA		NFOC2_HBETA	
0x30010100	NFOC2_DKP		NFOC2_DKI		NFOC2_DMAX		NFOC2_DMIN	
0x30010108	NFOC2_DEK		NFOC2_DEK1		NFOC2_DUK			
0x30010110	NFOC2_CVDUK		NFOC2_CVKI2D		NFOC2_HS		NFOC2_HTHETA	
0x30010118	NFOC2_UALORG		NFOC2_UBEORG		RSV		NFOC2_HTCOM	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30010120	NFOC2_QKP		NFOC2_QKI		NFOC2_QMAX		NFOC2_QMIN	
0x30010128	NFOC2_QEK		NFOC2_QEK1		NFOC2_QUK			
0x30010130	NFOC2_CVQUK		NFOC2_CVKI2Q		NFOC2_IALPHA		NFOC2_IBETA	
0x30010138	NFOC2_ID		NFOC2_IQ		NFOC2_IDFLT			
0x30010140	NFOC2_EKP		NFOC2_EKI		NFOC2_EMAX		NFOC2_EMIN	
0x30010148	NFOC2_EEK		NFOC2_EEK1		NFOC2_EUK			
0x30010150	RSV				NFOC2_IQFLT			
0x30010158	NFOC2_THETA				NFOC2_EALPHA			
					NFOC2_AFRPAH			
0x30010160	NFOC2_WKP		NFOC2_WKI		NFOC2_WMAX		NFOC2_WMIN	
0x30010168	NFOC2_WEK		NFOC2_WEK1		NFOC2_WUK			
0x30010170	RSV				NFOC2_AFRPBH			
					NFOC2_EBETA			
0x30010178	NFOC2_ETHETA				NFOC2_ZALORG		NFOC2_ZBEORG	
					NFOC2_AFKDF		NFOC2_AFKAF	
0x30010180	NFOC2_FWKP		NFOC2_FWKI		NFOC2_FWMAX		NFOC2_FWMIN	
0x30010188	NFOC2_FWEK		NFOC2_FWEK1		NFOC2_FWUK			
0x30010190	RSV		NFOC2_KUSF		NFOC2_OMEACC			
0x30010198	NFOC2_OMEEND				NFOC2_OMEMIN		NFOC2_FTCK	
0x300101A0	NFOC2_FBASE		NFOC2_OMEMI2		NFOC2_THECOM		NFOC2_FTCOM	
0x300101A8	NFOC2_EK1		NFOC2_EK2		NFOC2_EK3		NFOC2_EK4	
0x300101B0	NFOC2_FEK5				NFOC2_MERRRE		NFOC2_TDTC	
	NFOC2_KSLIDE		NFOC2_MAXERR		NFOC2_FEK6			
0x300101B8	NFOC2_IDREF		NFOC2_IQREF		NFOC2_I1		NFOC2_I2	
0x300101C0	NFOC2_IA		NFOC2_IB		NFOC2_IC		NFOC2_ICMAX	
0x300101C8	NFOC2_IAMAX		NFOC2_IBMAX		NFOC2_UDCPS		NFOC2_UQCPS	

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x300101D0	NFOC2_WREF		NFOC2_WFDB		NFOC2_ITK		NFOC2_POWK1	NFOC2_POWK2
0x300101D8	NFOC2_FGBASE		RSV		NFOC2_UALCPS		NFOC2_UBECPS	
0x300101E0	NFOC2_EMF		NFOC2_ATHETA		NFOC2_RATAR		NFOC2_RAOUT	
0x300101E8	NFOC2_RAINC		NFOC2_RADEC		NFOC2_LK1		NFOC2_LK2	
0x300101F0	NFOC2_LK3		NFOC2_LK4		NFOC2_LK5		NFOC2_LK6	
0x300101F8	NFOC2_LED		NFOC2_LEQ		NFOC2_LOME			
0x30010200	RSV				NFOC2_OMEGA		RSV	
0x30010208	NFOC2_IESTA		NFOC2_IESTB		NFOC2_OMEFLT			
0x30010210	NFOC2_OMEFL2				NFOC2_ZALPHA		NFOC2_ZBETA	
0x30010218	NFOC2_KLPF		NFOC2_FUWEI		NFOC2_UDFIN		NFOC2_UQFIN	
0x30010220	NFOC2_UALPHA		NFOC2_UBETA		RSV			
0x30010228 ~ 0x30010230	RSV							
0x30010238	NFOC2_UIK0		NFOC2_UIK1		NFOC2_UIK2		NFOC2_UIK3	
0x30010240	NFOC2_UITC0		NFOC2_UIUS0		NFOC2_UITC1		NFOC2_UIUS1	
0x30010248	NFOC2_UITC2		NFOC2_UIUS2		NFOC2_UITC3		NFOC2_UIUS3	
0x30010250	NFOC2_TRG1		NFOC2_TRG2		NFOC2_AFTHE			
0x30010258	NFOC2_OTHETA				NFOC2_USOMEK		NFOC2_UA	
0x30010260	NFOC2_UB		NFOC2_UC		NFOC2_USK		NFOC2_USOUS	
0x30010268	NFOC2_FTCPS		NFOC2_FTHETA		RSV			
0x30010270	RSV				NFOC2_FWREF		NFOC2_CMRSH	
0x30010278	NFOC2_TS		NFOC2_NTS		NFOC2_TDLY		NFOC2_TDLYD	
0x30010280	NFOC2_ARR		RSV		NFOC2_IDK		NFOC2_IQK	
0x30010288	NFOC2_OMEGAK		NFOC2_OMEK2		NFOC2_DELOTHE			
0x30010290	NFOC2_DELETEHE				NFOC2_UDCD		NFOC2_UDCQ	
0x30010298 ~ 0x300102F8	RSV							

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x30010300	RSV		NFOC2_CVDULO		RSV			
0x30010308 ~ 0x30010320	RSV							
0x30010328	RSV		NFOC2_CVQULO		RSV			
0x30010330	RSV							
0x30010338	RSV				NFOC2_WUCPS		NFOC2_WUFIN	
0x30010340 ~ 0x30010368	RSV							
0x30010370	NFOC2_UDK		NFOC2_UQK		NFOC2_UDFLT			
0x30010378	NFOC2_UQFLT				NFOC2_FWIDR		NFOC2_OSCNT	
0x30010380	NFOC2_OSSUM				RSV			
0x30010388	RSV				NFOC2_OMUNIT		NFOC2_CSAM	
0x30010390 ~ 0x300103A8	RSV						NFOC2_DLYCNT	
0x300103B0	RSV						NFOC2_IDRLIM	
0x300103B8 ~ 0x300103C0	RSV							
0x300103C8	RSV				NFOC2_CVK1		NFOC2_CVK3	
0x300103D0	NFOC2_CVDK4		NFOC2_CVQK4		NFOC2_CVDK5		NFOC2_CVQK5	
0x300103D8	NFOC2_DCOM		NFOC2_DAS		NFOC2_QCOM		NFOC2_QAS	
0x300103E0	NFOC2_CVK2		NFOC2_UDCLIM		NFOC2_UDCMAX		NFOC2_UDCMIN	
0x300103E8	NFOC2_FUMAX		NFOC2_FUMIN		NFOC2_IS		NFOC2_ITHETA	
0x300103F0	NFOC2_USFLT				NFOC2_DUKF		NFOC2_QUKF	
0x300103F8	RSV				NFOC2_UDCPS1		NFOC2_UQCPS1	

1.5.5.3 6N Pre-driver Register Address Mapping (FU7564Q1/FU7565Q1/FU7574Q1)

1.5.5.3.1 FU7564Q1/FU7574Q1 6N Pre-driverx Register Address Mapping

Table 1-6 FU7564Q1/FU7574Q1 6N Pre-driverx Register Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x00	RSV		SLPF_R	RSV				STAU_R
0x08	STAV_R	STAW_R	RSV					
0x80	RSV			I2C_R	DIS_R	RSV	VTHU_R	VTLU_R
0x88	TVDU_R	VTHV_R	VTLV_R	TVDV_R	VTHW_R	VTLW_R	TVDW_R	RSV

1.5.5.3.2 FU7565Q1 6N Pre-driver1 Register Address Mapping

Table 1-7 FU7565Q1 6N Pre-driver1 Register Address Mapping

Addr	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0x00	RSV		SLPF_R	RSV			TSD_R	STAU_R
0x08	STAV_R	STAW_R	RSV					
0x80	RSV				I2C_R	DIS_R	LIN_PU_R	VTHU_R
0x88	VTLU_R	TVDU_R	VTHV_R	VTLV_R	TVDV_R	VTHW_R	VTLW_R	TVDW_R

2 Pin Definitions

The IO types are defined as follows:

- > DI = Digital Input
- > DO = Digital Output
- > DB = Digital Bidirectional
- > AI = Analog Input
- > AO = Analog Output
- > AB = Analog Bidirectional
- > P = Power Input/Output or Ground

2.1 FU7512Q1 QFN56 Pins

Table 2-1 FU7512Q1 QFN56 Pin Descriptions

Pin	FU7512Q1 QFN56	IO Type	Description
PB2/ TIM8S/ TXD2S2/ TXRXD2S2/ FICED	1	DB/ DB/ DO/ DB/ DB	GPIO, configurable as EXTI1/EXTI2 input Timer8 input/output after function switching UART2 TXD output after the second function switching UART2 TXD output/RXD input in single-wire mode after the second function switching FICE data line
PB0/ AD1_2/ DBG2/ OLDBGS2	2	DB/ AI/ DO/ DO	GPIO, configurable as EXTI2 input ADC1 channel 2 input; Bus voltage divider sampling input Debug2 output DataMonitor output after the second function switching
PB1/ C1PS/ AD1_5/ HAL0B	3	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP1 positive input after function switching ADC1 channel 5 input Hall0 B input
PB3/ C0P/ AD1_6/ HAL0A	4	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 positive input ADC1 channel 6 input Hall0 A input

Pin	FU7512Q1 QFN56	IO Type	Description
PB4/ C0M/ C2PS/ AD1_7/ HAL0C	5	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 negative input CMP2 positive input after function switching ADC1 channel 7 input Hall0 C input
VDD2P5	6	P	2.5V LDO output, with an external capacitor of 1μF or above
PB5/ A0P	7	DB/ AI	GPIO, configurable as EXTI2 input AMP0 positive input
PB6/ A0M	8	DB/ AI	GPIO, configurable as EXTI2 input AMP0 negative input
PB7/ AD1_4/ C3P/ A0O/ C4M	9	DB/ AI/ AI/ AO/ AI	GPIO, configurable as EXTI2 input ADC1 channel 4 input CMP3 positive input AMP0 output CMP4 negative input
PB8/ C1P/ A1P/ AD1_8	10	DB/ AI/ AI/ AI	GPIO CMP1 positive input AMP1 positive input ADC1 channel 8 input
PB9/ C1M/ A1M	11	DB/ AI/ AI	GPIO CMP1 negative input AMP1 negative input
PB10/ AD1_0/ A1O	12	DB/ AI/ AO	GPIO ADC1 channel 0 input AMP1 output
PB11/ C2P/ A2P/ AD1_9	13	DB/ AI/ AI/ AI	GPIO CMP2 positive input AMP2 positive input ADC1 channel 9 input
PB12/ C2M/ A2M	14	DB/ AI/ AI	GPIO CMP2 negative input AMP2 negative input
PB13/ AD1_1/ A2O/ C4P/ DA1/ AD2_13	15	DB/ AI/ AO/ AI/ AO/ AI	GPIO ADC1 channel 1 input AMP2 output CMP4 positive input DAC1 output ADC2 channel 13 input

Pin	FU7512Q1 QFN56	IO Type	Description
PB15/ AD1_10/ C3PS/ C4MS	16	DB/ AI/ AI/ AI	GPIO ADC1 channel 10 input CMP3 positive input after function switching CMP4 negative input after function switching
PD5/ VREF	17	DB/ AB	GPIO ADC external VREF input or internal VREF output, with a $1\ \mu\text{F} \sim 4.7\ \mu\text{F}$ external capacitor
PD2/ VHALF	18	DB/ AO	GPIO 1/2 VREF voltage output, with a $1\ \mu\text{F}$ external capacitor
PC15/ AD2_10/ C9PS/ C10MS	19	DB/ AI/ AI/ AI	GPIO ADC2 channel 10 input CMP9 positive input after function switching CMP10 negative input after function switching
PC13/ C8M/ A6M	20	DB/ AI/ AI	GPIO CMP8 negative input AMP6 negative input
PC12/ C8P/ A6P/ AD2_9	21	DB/ AI/ AI/ AI	GPIO CMP8 positive input AMP6 positive input ADC2 channel 9 input
PC10/ C7M/ A5M	22	DB/ AI/ AI	GPIO CMP7 negative input AMP5 negative input
PC9/ C7P/ A5P/ C11M/ AD2_8	23	DB/ AI/ AI/ AI/ AI	GPIO CMP7 positive input AMP5 positive input CMP11 negative input ADC2 channel 8 input
PC7/ A4M	24	DB/ AI	GPIO, configurable as EXTI2 input AMP4 negative input
PC6/ A4P	25	DB/ AI	GPIO, configurable as EXTI2 input AMP4 positive input
PC5/ C6M/ C8PS/ AD2_7/ HAL1C	26	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 negative input CMP8 input after function switching ADC2 channel 7 input Hall1 C-phase input
PC4/ C6P/ AD2_6/ HAL1A	27	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 positive input ADC2 channel 6 input Hall1 A-phase input

Pin	FU7512Q1 QFN56	IO Type	Description
PC3/ C7PS/ AD2_5/ HAL1B	28	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP7 positive input after function switching ADC2 channel 5 input Hall1 B-phase input
PC2/ AD3_0/ C5P/ A3O	29	DB/ AI/ AI/ AO	GPIO, configurable as EXTI2 input ADC3 channel 0 input CMP5 positive input AMP3 output
PC1/ AD2_2/ C5M/ DA2/ A3M	30	DB/ AI/ AI/ AO/ AI	GPIO, configurable as EXTI2 input ADC2 channel 2 input CMP5 negative input DAC2 output AMP3 negative input
PC0/ C9M/ DA3/ AD2_3/ A3P	31	DB/ AI/ AO/ AI/ AI	GPIO, configurable as EXTI2 input CMP9 negative input DAC3 output ADC2 channel 3 input AMP3 positive input
PD0/ AD2_11/ AD3_1/ TIM7S2	32	DB/ AI/ AI/ DB	GPIO, configurable as EXTI0 input ADC2 channel 11 input ADC3 channel 1 input (sampling PFC input voltage PFC_UAC) Timer7 input/output after the second function switching
PA0/ OLDBGS/ TIM4/ TIM3S/ TXD1/ LTX/ CTX/ SDA1	33	DB/ DO/ DB/ DB/ DO/ DO/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input DataMonitor output after function switching Timer4 input/output Timer3 input/output after function switching UART1 TXD output LIN TXD output CAN TXD output I ² C1 SDA, with open-drain output
PA1/ DBG1/ TIM7/ RXD1/ TXRXD1/ LRX/ CRX/ SCL1	34	DB/ DO/ DB/ DI/ DB/ DI/ DI/ DB	GPIO, configurable as EXTI0/EXTI1 input Debug1 output Timer7 input/output UART1 RXD input UART1 TXD output/RXD input in single-wire mode LIN RXD input CAN RXD input I ² C1 SCL, with open-drain output

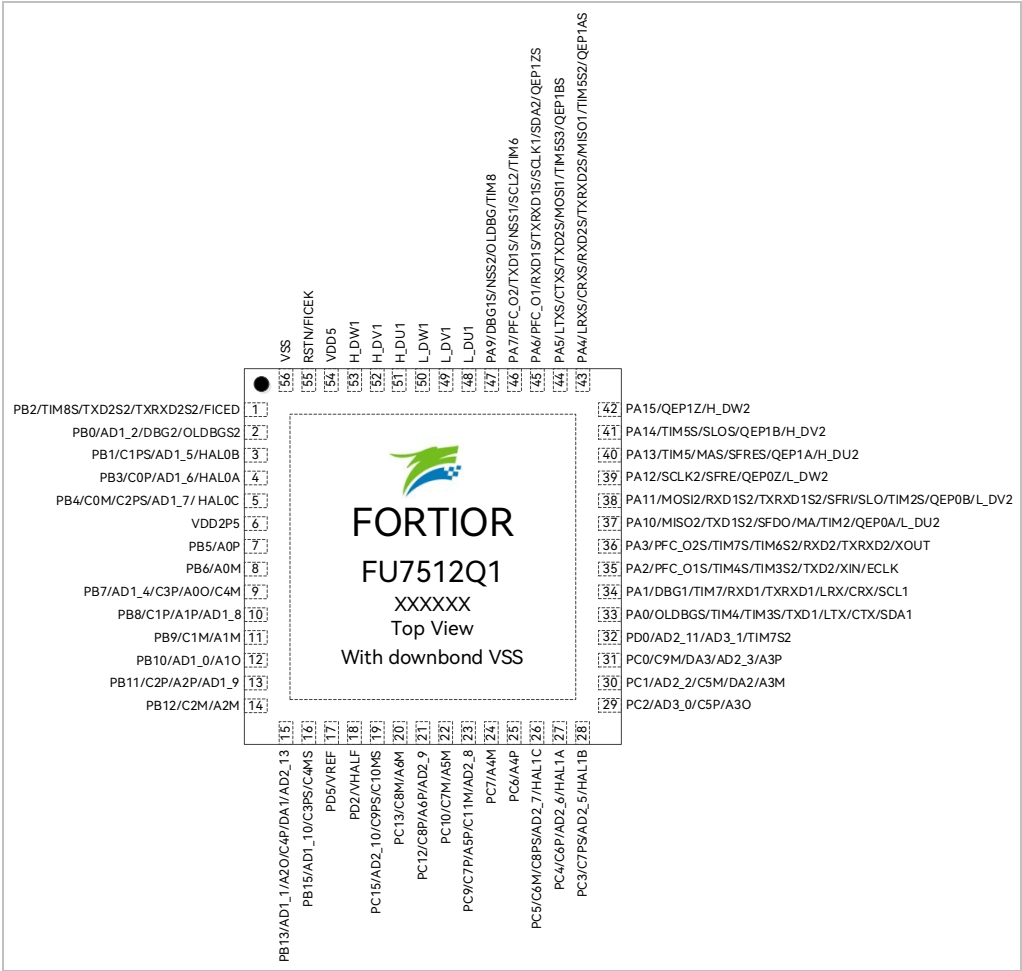
Pin	FU7512Q1 QFN56	IO Type	Description
PA2/ PFC_O1S/ TIM4S/ TIM3S2/ TXD2/ XIN/ ECLK	35	DB/ DO/ DB/ DB/ DO/ AI/ DI	GPIO, configurable as EXTI0/EXTI1 input PFC PWM1 output after function switching Timer4 input/output after function switching Timer3 input/output after the second function switching UART2 TXD output External fast clock input External crystal input
PA3/ PFC_O2S/ TIM7S/ TIM6S2/ RXD2/ TXRXD2/ XOUT	36	DB/ DO/ DB/ DB/ DI/ DB/ AO	GPIO, configurable as EXTI0/EXTI1 input PFC PWM2 output after function switching Timer7 input/output after function switching Timer6 input/output after the second function switching UART2 RXD input UART2 TXD output/RXD input in single-wire mode External fast clock output
PA10/ MISO2/ TXD1S2/ SFDO/ MA/ TIM2/ QEP0A/ L_DU2	37	DB/ DB/ DO/ DO/ DO/ DB/ DI/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 MISO, master input or slave output UART1 TXD output after the second function switching TFDO output in S-format communication BISS MA output Timer2 input/output QEP0 A input Low-side U-phase PWM output (slave motor)
PA11/ MOSI2/ RXD1S2/ TXRXD1S2/ SFRI/ SLO/ TIM2S/ QEP0B/ L_DV2	38	DB/ DB/ DI/ DB/ DI/ DI/ DB/ DI/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 MOSI, master output or slave input UART1 RXD input after the second function switching UART1 TXD output/RXD input in single-wire mode after the second function switching TFRI input for S-format communication BISS SLO input Timer2 input/output after function switching QEP0 B input Low-side V-phase PWM output (slave motor)
PA12/ SCLK2/ SFRE/ QEP0Z/ L_DW2	39	DB/ DB/ DO/ DB/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 clock S-format communication output QEP0 Z-signal input/output Low-side W-phase PWM output (slave motor)

Pin	FU7512Q1 QFN56	IO Type	Description
PA13/ TIM5/ MAS/ SFRES/ QEP1A/ H_DU2	40	DB/ DB/ DO/ DO/ DI/ DO	GPIO, configurable as EXTI1 input Timer5 input/output BISS MA output after function switching S-format communication output after function switching QEP1 A input High-side U-phase PWM output (slave motor)
PA14/ TIM5S/ SLOS/ QEP1B/ H_DV2	41	DB/ DB/ DI/ DI/ DO	GPIO, configurable as EXTI1 input Timer5 input/output after function switching BISS SLO input after function switching QEP1 B input High-side V-phase PWM output (slave motor)
PA15/ QEP1Z/ H_DW2	42	DB/ DB/ DO	GPIO QEP1 Z-signal input/output High-side W-phase PWM output (slave motor)
PA4/ LRXS/ CRXS/ RXD2S/ TXRXD2S/ MISO1/ TIM5S2/ QEP1AS	43	DB/ DI/ DI/ DI/ DB/ DI/ DB/ DI	GPIO, configurable as EXTI0/EXTI1 input LIN RXD input after function switching CAN RXD input after function switching UART2 RXD input after function switching UART2 TXD output/RXD input in single-wire mode after function switching SPI1 MISO, master input or slave output Timer5 input/output after the second function switching QEP1 A input after function switching
PA5/ LTXS/ CTXS/ TXD2S/ MOSI1/ TIM5S3/ QEP1BS	44	DB/ DO/ DO/ DO/ DB/ DB/ DI	GPIO, configurable as EXTI0/EXTI1 input LIN TXD output after function switching CAN TXD output after function switching UART2 TXD output after function switching SPI1 MOSI, master output or slave input Timer5 input/output after the third function switching QEP1 B input after function switching
PA6/ PFC_O1/ RXD1S/ TXRXD1S/ SCLK1/ SDA2/ QEP1ZS	45	DB/ DO/ DI/ DB/ DI/ DB/ DB	GPIO, configurable as EXTI0/EXTI1 input PFC1 PWM output UART1 RXD input after function switching UART1 TXD output/RXD input in single-wire mode after function switching SPI1 clock I ² C2 SDA QEP1 Z-signal input/output after function switching

Pin	FU7512Q1 QFN56	IO Type	Description
PA7/ PFC_O2/ TXD1S/ NSS1/ SCL2/ TIM6	46	DB/ DO/ DO/ DB/ DB/ DB	GPIO, configurable as EXTI0/EXTI1 input PFC2 PWM output UART1 TXD output after function switching SPI1 NSS I ² C2 SCL Timer6 input/output
PA9/ DBG1S/ NSS2/ OLDBG/ TIM8	47	DB/ DO/ DB/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input Debug1 output after function switching SPI2 NSS DataMonitor output Timer8 input/output
L_DU1	48	DO	Low-side U-phase PWM output (master motor)
L_DV1	49	DO	Low-side V-phase PWM output (master motor)
L_DW1	50	DO	Low-side W-phase PWM output (master motor)
H_DU1	51	DO	High-side U-phase PWM output (master motor)
H_DV1	52	DO	High-side V-phase PWM output (master motor)
H_DW1	53	DO	High-side W-phase PWM output (master motor)
VDD5	54	P	5V power supply, with a 1μF ~ 4.7μF external capacitor
RSTN/ FICEK	55	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VSS	56	P	Ground

2.2 FU7512Q1 QFN56 Pinout Diagram

Figure 2–1 Pinout Diagram of FU7512Q1 QFN56



2.3 FU7564Q1 QFN56 Pins

Table 2-2 FU7564Q1 QFN56 Pin Descriptions

Pin	FU7564Q1 QFN56	IO Type	Description
VSW1	1	P	6N pre-driver1 W-phase input, as GND reference for W-phase high-side bootstrap
HV1	2	DO	6N pre-driver1 high-side V-phase output
VBV1	3	P	6N pre-driver1 high-side V-phase bootstrap power supply
VSV1	4	P	6N pre-driver1 V-phase input, as GND reference for high-side V-phase bootstrap
HU1	5	DO	6N pre-driver1 high-side U-phase output
VBU1	6	P	6N pre-driver1 high-side U-phase bootstrap power supply
VSU1	7	P	6N pre-driver1 U-phase input, as GND reference for high-side U-phase bootstrap
VBB	8	P	Driver power supply, 11V LDO1, with a 1μF external capacitor connected to VSS. When VCC ≥ 12V, it delivers an additional load capability of no less than 30mA.
VDH1	9	P	6N pre-driver1 high-side MOSFET drain voltage connection
VCP_1	10	P	Charge pump 1 output, with a 1μF external capacitor connected to VDH1 pin
CP2_1	11	DO	Charge pump 1 pin, with a 0.1μF capacitor connected to CP1_1 pin
CP1_1	12	DO	Charge pump 1 pin, with a 0.1μF capacitor connected to CP2_1 pin
VCC	13	P	Power input
LIN	14	DB	LIN bus
MON_HV1	15	DI	MON1 high-voltage input
COM_1	16	P	6N pre-driver1 ground
VDD5	17	P	5V LDO2 output to supply voltage for the digital and analog sections, with a 1μF external capacitor connected to VSS. When VCC ≥ 12V, it delivers an additional load capability of no less than 30mA.
RSTN/ FICEK	18	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VSS	19	P	MCU ground
PB2/ TIM8S/ TXD2S2/ TXRXD2S2/ FICED	20	DB/ DB/ DO/ DB/ DB	GPIO, configurable as EXTI1/EXTI2 input Timer8 input/output after function switching UART2 TXD output after the second function switching UART2 TXD output/RXD input in single-wire mode after the second function switching FICE data line

Pin	FU7564Q1 QFN56	IO Type	Description
PB0/ AD1_2/ DBG2/ OLDBGS2	21	DB/ AI/ DO/ DO	GPIO, configurable as EXTI2 input ADC1 channel 2 input; Bus voltage divider sampling input Debug2 output DataMonitor output after the second function switching
PB1/ C1PS/ AD1_5/ HAL0B	22	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP1 positive input after function switching ADC1 channel 5 input Hall0 B input
PB3/ C0P/ AD1_6/ HAL0A	23	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 positive input ADC1 channel 6 input Hall0 A input
PB4/ C0M/ C2PS/ AD1_7/ HAL0C	24	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 negative input CMP2 positive input after function switching ADC1 channel 7 input Hall0 C input
VDD2P5	25	P	2.5V LDO3 output, with an external capacitor of 1μF or above
PB5/ A0P	26	DB/ AI	GPIO, configurable as EXTI2 input AMP0 positive input
PB6/ A0M	27	DB/ AI	GPIO, configurable as EXTI2 input AMP0 negative input
PB8/ C1P/ A1P/ AD1_8	28	DB/ AI/ AI/ AI	GPIO CMP1 positive input AMP1 positive input ADC1 channel 8 input
PB9/ C1M/ A1M	29	DB/ AI/ AI	GPIO CMP1 negative input AMP1 negative input
PB11/ C2P/ A2P/ AD1_9	30	DB/ AI/ AI/ AI	GPIO CMP2 positive input AMP2 positive input ADC1 channel 9 input
PB12/ C2M/ A2M	31	DB/ AI/ AI	GPIO CMP2 negative input AMP2 negative input
PB15/ AD1_10/ C3PS/ C4MS	32	DB/ AI/ AI/ AI	GPIO ADC1 channel 10 input CMP3 positive input after function switching CMP4 negative input after function switching

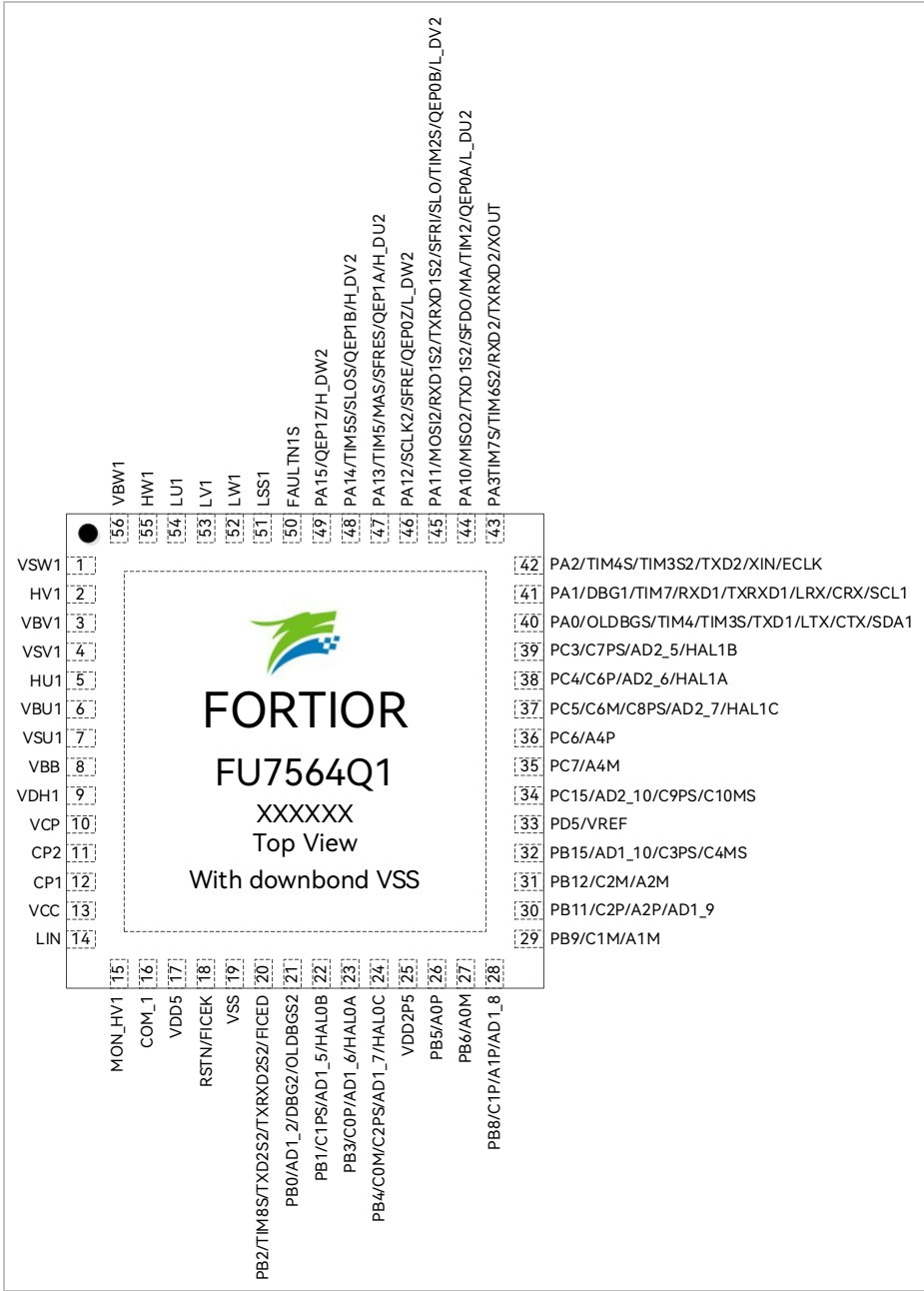
Pin	FU7564Q1 QFN56	IO Type	Description
PD5/ VREF	33	DB/ AB	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
PC15/ AD2_10/ C9PS/ C10MS	34	DB/ AI/ AI/ AI	GPIO ADC2 channel 10 input CMP9 positive input after function switching CMP10 negative input after function switching
PC7/ A4M	35	DB/ AI	GPIO, configurable as EXTI2 input AMP4 negative input
PC6/ A4P	36	DB/ AI	GPIO, configurable as EXTI2 input AMP4 positive input
PC5/ C6M/ C8PS/ AD2_7/ HAL1C	37	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 negative input CMP8 positive input after function switching ADC2 channel 7 input Hall1 C-phase input
PC4/ C6P/ AD2_6/ HAL1A	38	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 positive input ADC2 channel 6 input Hall1 A-phase input
PC3/ C7PS/ AD2_5/ HAL1B	39	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP7 positive input after function switching ADC2 channel 5 input Hall1 B-phase input
PA0/ OLDBGS/ TIM4/ TIM3S/ TXD1/ LTX/ CTX/ SDA1	40	DB/ DO/ DB/ DB/ DO/ DO/ DO/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input DataMonitor output after function switching Timer4 input/output Timer3 input/output after function switching UART1 TXD output LIN TXD output CAN TXD output I ² C1 SDA, with open-drain output
PA1/ DBG1/ TIM7/ RXD1/ TXRXD1/ LRX/ CRX/ SCL1	41	DB/ DO/ DB/ DI/ DB/ DI/ DI/ DI/ DB	GPIO, configurable as EXTI0/EXTI1 input Debug1 output Timer7 input/output UART1 RXD input UART1 TXD output/RXD input in single-wire mode LIN RXD input CAN RXD input I ² C1 SCL, with open-drain output

Pin	FU7564Q1 QFN56	IO Type	Description
PA2/ TIM4S/ TIM3S2/ TXD2/ XIN/ ECLK	42	DB/ DB/ DB/ DO/ AI/ DI	GPIO, configurable as EXTI0/EXTI1 input Timer4 input/output after function switching Timer3 input/output after the second function switching UART2 TXD output External fast clock input External crystal input
PA3/ TIM7S/ TIM6S2/ RXD2/ TXRXD2/ XOUT	43	DB/ DB/ DB/ DI/ DB/ AO	GPIO, configurable as EXTI0/EXTI1 input Timer7 input/output after function switching Timer6 input/output after the second function switching UART2 RXD input UART2 TXD output/RXD input in single-wire mode External fast clock output
PA10/ MISO2/ TXD1S2/ SFDO/ MA/ TIM2/ QEP0A/ L_DU2	44	DB/ DB/ DO/ DO/ DO/ DB/ DI/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 MISO, master input or slave output UART1 TXD output after the second function switching TFDO output in S-format communication BISS MA output Timer2 input/output QEP0 A input Low-side U-phase PWM output (slave motor)
PA11/ MOSI2/ RXD1S2/ TXRXD1S2/ SFRI/ SLO/ TIM2S/ QEP0B/ L_DV2	45	DB/ DB/ DI/ DB/ DI/ DI/ DB/ DI/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 MOSI, master output or slave input UART1 RXD input after the second function switching UART1 TXD output/RXD input in single-wire mode after the second function switching TFRI input for S-format communication BISS SLO input Timer2 input/output after function switching QEP0 B input Low-side V-phase PWM output (slave motor)
PA12/ SCLK2/ SFRE/ QEP0Z/ L_DW2	46	DB/ DB/ DO/ DB/ DO	GPIO, configurable as EXTI0/EXTI1 input SPI2 clock S-format communication output QEP0 Z-signal input/output Low-side W-phase PWM output (slave motor)
PA13/ TIM5/ MAS/ SFRES/ QEP1A/ H_DU2	47	DB/ DB/ DO/ DO/ DI/ DO	GPIO, configurable as EXTI1 input Timer5 input/output BISS MA output after function switching S-format communication output after function switching QEP1 A input High-side U-phase PWM output (slave motor)

Pin	FU7564Q1 QFN56	IO Type	Description
PA14/ TIM5S/ SLOS/ QEP1B/ H_DV2	48	DB/ DB/ DI/ DI/ DO	GPIO, configurable as EXTI1 input Timer5 input/output after function switching BISS SLO input after function switching QEP1 B input High-side V-phase PWM output (slave motor)
PA15/ QEP1Z/ H_DW2	49	DB/ DB/ DO	GPIO QEP1 Z-signal input/output High-side W-phase PWM output (slave motor)
FAULTN1S	50	DO	FAULTN1 output after function switching, used for fault status indication. High level (H) indicates normal operation and low level (L) indicates fault status. It can be configured with a 4.7k Ω pull-up resistor via the associated register, and defaults to a high-impedance input.
LSS1	51	AO	This pin provides the discharge path for the gate capacitors of the low-side MOSFET in the phases U, V and W. Each path features low impedance and connects to the common source of the external low-side MOSFET.
LW1	52	DO	6N pre-driver1 low-side W-phase output
LV1	53	DO	6N pre-driver1 low-side V-phase output
LU1	54	DO	6N pre-driver1 low-side U-phase output
HW1	55	DO	6N pre-driver1 high-side W-phase output
VBW1	56	P	6N pre-driver1 high-side W-phase bootstrap power supply

2.4 FU7564Q1 QFN56 Pinout Diagram

Figure 2-2 FU7564Q1 QFN56 Pinout Diagram



2.5 FU7565Q1 QFN48 Pins

Table 2-3 FU7565Q1 QFN48 Pin Descriptions

Pin	FU7565Q1 QFN48	IO Type	Description
PB5/ A0P	1	DB/ AI	GPIO, configurable as EXTI2 input AMP0 positive input
PB6/ A0M	2	DB/ AI	GPIO, configurable as EXTI2 input AMP0 negative input
PB8/ C1P/ A1P/ AD1_8	3	DB/ AI/ AI/ AI	GPIO CMP1 positive input AMP1 positive input ADC1 channel 8 input
PB15/ AD1_10/ C3PS/ C4MS	4	DB/ AI/ AI/ AI	GPIO ADC1 channel 10 input CMP3 positive input after function switching CMP4 negative input after function switching
PD5/ VREF	5	DB/ AB	GPIO ADC external VREF input or internal VREF output, with a 1μF~4.7μF external capacitor
PC11/ AD2_0/ C11P/ A5O	6	DB/ AI/ AI/ AO	GPIO ADC2 channel 0 input CMP11 positive input AMP5 output
PC10/ C7M/ A5M	7	DB/ AI/ AI	GPIO CMP7 negative input AMP5 negative input
PC9/ C7P/ A5P/ C11M/ AD2_8	8	DB/ AI/ AI/ AI/ AI	GPIO CMP7 positive input AMP5 positive input CMP11 negative input ADC2 channel 8 input
PD0/ AD2_11/ TIM7S2	9	DB/ AI/ DB	GPIO, configurable as EXTI0 input ADC2 channel 11 input Timer7 input/output after the second function switching

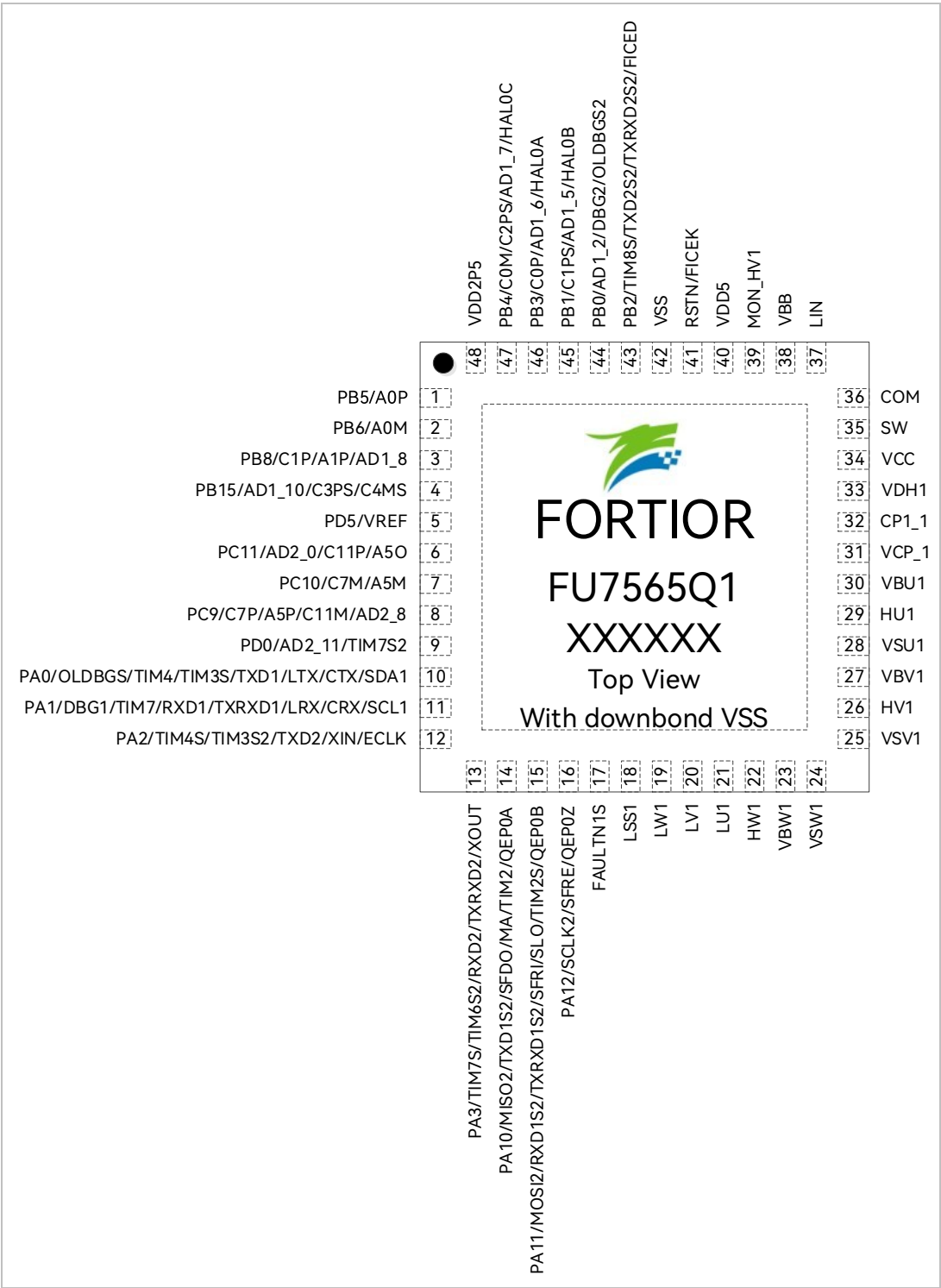
Pin	FU7565Q1 QFN48	IO Type	Description
PA0/ OLDBGS/ TIM4/ TIM3S/ TXD1/ LTX/ CTX/ SDA1	10	DB/ DO/ DB/ DB/ DO/ DO/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input DataMonitor output after function switching Timer4 input/output Timer3 input/output after function switching UART1 TXD output LIN TXD output CAN TXD output I ² C1 SDA, with open-drain output
PA1/ DBG1/ TIM7/ RXD1/ TXRXD1/ LRX/ CRX/ SCL1	11	DB/ DO/ DB/ DI/ DB/ DI/ DI/ DB	GPIO, configurable as EXTI0/EXTI1 input Debug1 output Timer7 input/output UART1 RXD input UART1 TXD output/RXD input in single-wire mode LIN RXD input CAN RXD input I ² C1 SCL, with open-drain output
PA2/ TIM4S/ TIM3S2/ TXD2/ XIN/ ECLK	12	DB/ DB/ DB/ DO/ AI/ DI	GPIO, configurable as EXTI0/EXTI1 input Timer4 input/output after function switching Timer3 input/output after the second function switching UART2 TXD output External fast clock input External crystal input
PA3/ TIM7S/ TIM6S2/ RXD2/ TXRXD2/ XOUT	13	DB/ DB/ DB/ DI/ DB/ AO	GPIO, configurable as EXTI0/EXTI1 input Timer7 input/output after function switching Timer6 input/output after the second function switching UART2 RXD input UART2 TXD output/RXD input in single-wire mode External fast clock output
PA10/ MISO2/ TXD1S2/ SFDO/ MA/ TIM2/ QEP0A	14	DB/ DB/ DO/ DO/ DO/ DB/ DI	GPIO, configurable as EXTI0/EXTI1 input SPI2 MISO, master input or slave output UART1 TXD output after the second function switching TFDO output in S-format communication BISS MA output Timer2 input/output QEP0 A input

Pin	FU7565Q1 QFN48	IO Type	Description
PA11/ MOSI2/ RXD1S2/ TXRXD1S2/ SFRI/ SLO/ TIM2S/ QEP0B	15	DB/ DB/ DI/ DB/ DI/ DI/ DB/ DI	GPIO, configurable as EXTI0/EXTI1 input SPI2 MOSI, master output or slave input UART1 RXD input after the second function switching UART1 TXD output/RXD input in single-wire mode after the second function switching TFRI input for S-format communication BISS SLO input Timer2 input/output after function switching QEP0 B input
PA12/ SCLK2/ SFRE/ QEP0Z	16	DB/ DB/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input SPI2 clock S-format communication output QEP0 Z-signal input/output
FAULTN1S	17	DO	FAULTN1 output after function switching, used for fault status indication. High level (H) indicates normal operation and low level (L) indicates fault status. It can be configured with a 4.7k Ω pull-up resistor via the associated register, and defaults to a high-impedance input.
LSS1	18	AO	This pin provides the discharge path for the gate capacitors of the low-side MOSFET in the phases U, V and W. Each path features low impedance and connects to the common source of the external low-side MOSFET.
LW1	19	DO	6N pre-driver1 low-side W-phase output
LV1	20	DO	6N pre-driver1 low-side V-phase output
LU1	21	DO	6N pre-driver1 low-side U-phase output
HW1	22	DO	6N pre-driver1 high-side W-phase output
VBW1	23	P	6N pre-driver1 high-side W-phase bootstrap power supply
VSW1	24	P	6N pre-driver1 W-phase input, as GND reference for W-phase high-side bootstrap
VSV1	25	P	6N pre-driver1 V-phase input, as GND reference for high-side V-phase bootstrap
HV1	26	DO	6N pre-driver1 high-side V-phase output
VBV1	27	P	6N pre-driver1 high-side V-phase bootstrap power supply
VSU1	28	P	6N pre-driver1 U-phase input, as GND reference for high-side U-phase bootstrap
HU1	29	DO	6N pre-driver1 high-side U-phase output
VBU1	30	P	6N pre-driver1 high-side U-phase bootstrap power supply
VCP_1	31	P	Charge pump 1 output, with a 1 μ F external capacitor connected to VDH1 pin
CP1_1	32	DO	Charge pump 1 pin, with a 0.1 μ F capacitor connected to SW pin
VDH1	33	P	6N pre-driver1 high-side MOSFET drain voltage connection

Pin	FU7565Q1 QFN48	IO Type	Description
VCC	34	P	Power input
SW	35	DO	Buck DC-DC converter switch output, with an external 100 μ H inductor connected to VBB
COM_1	36	P	Buck DC-DC converter ground
LIN	37	DB	LIN bus
VBB	38	P	Buck DC-DC converter output, with an external inductor connected to SW and a 1 μ F capacitor connected to ground
MON_HV1	39	DI	MON1 high-voltage input
VDD5	40	P	5V LDO1 output with a 1 μ F ~ 4.7 μ F external capacitor
RSTN/ FICEK	41	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VSS	42	P	MCU ground
PB2/ TIM8S/ TXD2S2/ TXRXD2S2/ FICED	43	DB/ DB/ DO/ DB/ DB	GPIO, configurable as EXTI1/EXTI2 input Timer8 input/output after function switching UART2 TXD output after the second function switching UART2 TXD output/RXD input in single-wire mode after the second function switching FICE data line
PB0/ AD1_2/ DBG2/ OLDBGS2	44	DB/ AI/ DO/ DO	GPIO, configurable as EXTI2 input ADC1 channel 2 input; Bus voltage divider sampling input Debug2 output DataMonitor output after the second function switching
PB1/ C1PS/ AD1_5/ HAL0B	45	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP1 positive input after function switching ADC1 channel 5 input Hall0 B input
PB3/ C0P/ AD1_6/ HAL0A	46	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 positive input ADC1 channel 6 input Hall0 A input
PB4/ C0M/ C2PS/ AD1_7/ HAL0C	47	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 negative input CMP2 positive input after function switching ADC1 channel 7 input Hall0 C input
VDD2P5	48	P	2.5V LDO2 output, with an external capacitor of 1 μ F or above

2.6 FU7565Q1 QFN48 Pinout Diagram

Figure 2–3 FU7565Q1 QFN48 Pinout Diagram



2.7 FU7574Q1 QFN88 Pins

Table 2-4 FU7574Q1 QFN88 Pin Descriptions

Pin	FU7574Q1 QFN88	IO Type	Description
PC3/ C7PS/ AD2_5/ HAL1B	1	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP7 positive input after function switching ADC2 channel 5 input Hall1 B-phase input
PC2/ AD3_0/ C5P/ A3O	2	DB/ AI/ AI/ AO	GPIO, configurable as EXTI2 input ADC3 channel 0 input CMP5 positive input AMP3 output
PC1/ AD2_2/ C5M/ DA2/ A3M	3	DB/ AI/ AI/ AO/ AI	GPIO, configurable as EXTI2 input ADC2 channel 2 input CMP5 negative input DAC2 output AMP3 negative input
PC0/ C9M/ DA3/ AD2_3/ A3P	4	DB/ AI/ AO/ AI/ AI	GPIO, configurable as EXTI2 input CMP9 negative input DAC3 output ADC2 channel 3 input AMP3 positive input
PD0/ AD2_11/ AD3_1/ TIM7S2	5	DB/ AI/ AI/ DB	GPIO, configurable as EXTI0 input ADC2 channel 11 input ADC3 channel 1 input (sampling PFC input voltage PFC_UAC) Timer7 input/output after the second function switching
PD3/ AD2_14/ TIM4S2	6	DB/ AI/ DB	GPIO, configurable as EXTI0 input ADC2 channel 14 input Timer4 input/output after the second function switching
PD4/ AD2_15	7	DB/ AI	GPIO ADC2 channel 15 input
PA0/ OLDBGS/ TIM4/ TIM3S/ TXD1/ LTX/ CTX/ SDA1	8	DB/ DO/ DB/ DB/ DO/ DO/ DO/ DB	GPIO, configurable as EXTI0/EXTI1 input DataMonitor output after function switching Timer4 input/output Timer3 input/output after function switching UART1 TXD output LIN TXD output CAN TXD output MCU I ² C1 SDA, with open-drain output

Pin	FU7574Q1 QFN88	IO Type	Description
PA1/ DBG1/ TIM7/ RXD1/ TXRXD1/ LRX/ CRX/ SCL1	9	DB/ DO/ DB/ DI/ DB/ DI/ DI/ DB	GPIO, configurable as EXTI0/EXTI1 input Debug1 output Timer7 input/output UART1 RXD input UART1 TXD output/RXD input in single-wire mode LIN RXD input CAN RXD input MCU I ² C1 SCL, with open-drain output
PA2/ PFC_O1S/ TIM4S/ TIM3S2/ TXD2/ XIN/ ECLK	10	DB/ DO/ DB/ DB/ DO/ AI/ DI	GPIO, configurable as EXTI0/EXTI1 input PFC PWM1 output after function switching Timer4 input/output after function switching Timer3 input/output after the second function switching UART2 TXD output External fast clock input External crystal input
PA3/ PFC_O2S/ TIM7S/ TIM6S2/ RXD2/ TXRXD2/ XOUT	11	DB/ DO/ DB/ DB/ DI/ DB/ AO	GPIO, configurable as EXTI0/EXTI1 input PFC PWM2 output after function switching Timer7 input/output after function switching Timer6 input/output after the second function switching UART2 RXD input UART2 TXD output/RXD input in single-wire mode External fast clock output
SCL_DRV2	12	DB	6N pre-driver2 I ² C SCL, with open-drain output
SDA_DRV2	13	DB	6N pre-driver2 I ² C SCL, with open-drain output
FAULTN2S	14	DO	FAULTN2 output after function switching, used for fault status indication. High level (H) indicates normal operation and low level (L) indicates fault status. It can be configured with a 4.7kΩ pull-up resistor via the associated register, and defaults to a high-impedance input.
LSS2	15	AO	This pin provides the discharge path for the gate capacitors of the low-side MOSFET in the phases U, V and W. Each path features low impedance and connects to the common source of the external low-side MOSFET.
LW2	16	DO	6N pre-driver2 low-side W-phase output
LV2	17	DO	6N pre-driver2 low-side V-phase output
LU2	18	DO	6N pre-driver2 low-side U-phase output
HW1	19	DO	6N pre-driver2 high-side W-phase output
VBW2	20	P	6N pre-driver2 high-side W-phase bootstrap power supply
VSW2	21	P	6N pre-driver2 W-phase input, as GND reference for high-side W-phase bootstrap
HV2	22	DO	6N pre-driver2 high-side V-phase output

Pin	FU7574Q1 QFN88	IO Type	Description
VBV2	23	P	6N pre-driver2 high-side V-phase bootstrap power supply
VSV2	24	P	6N pre-driver2 V-phase input, as GND reference for high-side V-phase bootstrap
HU2	25	DO	6N pre-driver2 high-side U-phase output
VBU2	26	P	6N pre-driver2 high-side U-phase bootstrap power supply
VSU2	27	P	6N pre-driver2 U-phase input, as GND reference for high-side U-phase bootstrap
VBB_2	28	P	Driver power supply, 11V LDO4, with a 1μF external capacitor connected to VSS. When VCC_2 ≥ 12V, it delivers an additional load capability of no less than 30mA.
VDH2	29	P	6N pre-driver2 high-side MOSFET drain voltage connection
VCP_2	30	P	Charge pump 2 output, with a 1μF external capacitor connected to VDH2 pin
CP2_2	31	DO	Charge pump 2 pin, with a 0.1μF capacitor connected to CP1_2 pin
CP1_2	32	DO	Charge pump 2 pin, with a 0.1μF capacitor connected to CP2_2 pin
VCC_2	33	P	Power input
MON_HV2	34	DI	MON2 high-voltage input
COM_2	35	P	6N pre-driver2 ground
VDD5_2	36	P	5V LDO5 output with a 1μF ~ 4.7μF external capacitor
FAULTN1S	37	DO	FAULTN1 output after function switching, used for fault status indication. High level (H) indicates normal operation and low level (L) indicates fault status. It can be configured with a 4.7kΩ pull-up resistor via the associated register, and defaults to a high-impedance input.
LSS1	38	AO	This pin provides the discharge path for the gate capacitors of the low-side MOSFET in the phases U, V and W. Each path features low impedance and connects to the common source of the external low-side MOSFET.
LW1	39	DO	6N pre-driver1 low-side W-phase output
LV1	40	DO	6N pre-driver1 low-side V-phase output
LU1	41	DO	6N pre-driver1 low-side U-phase output
HW1	42	DO	6N pre-driver1 high-side W-phase output
VBW1	43	P	6N pre-driver1 high-side W-phase bootstrap power supply
VSW1	44	P	6N pre-driver1 W-phase input, as GND reference for W-phase high-side bootstrap
HV1	45	DO	6N pre-driver1 high-side V-phase output
VBV1	46	P	6N pre-driver1 high-side V-phase bootstrap power supply
VSV1	47	P	6N pre-driver1 V-phase input, as GND reference for high-side V-phase bootstrap

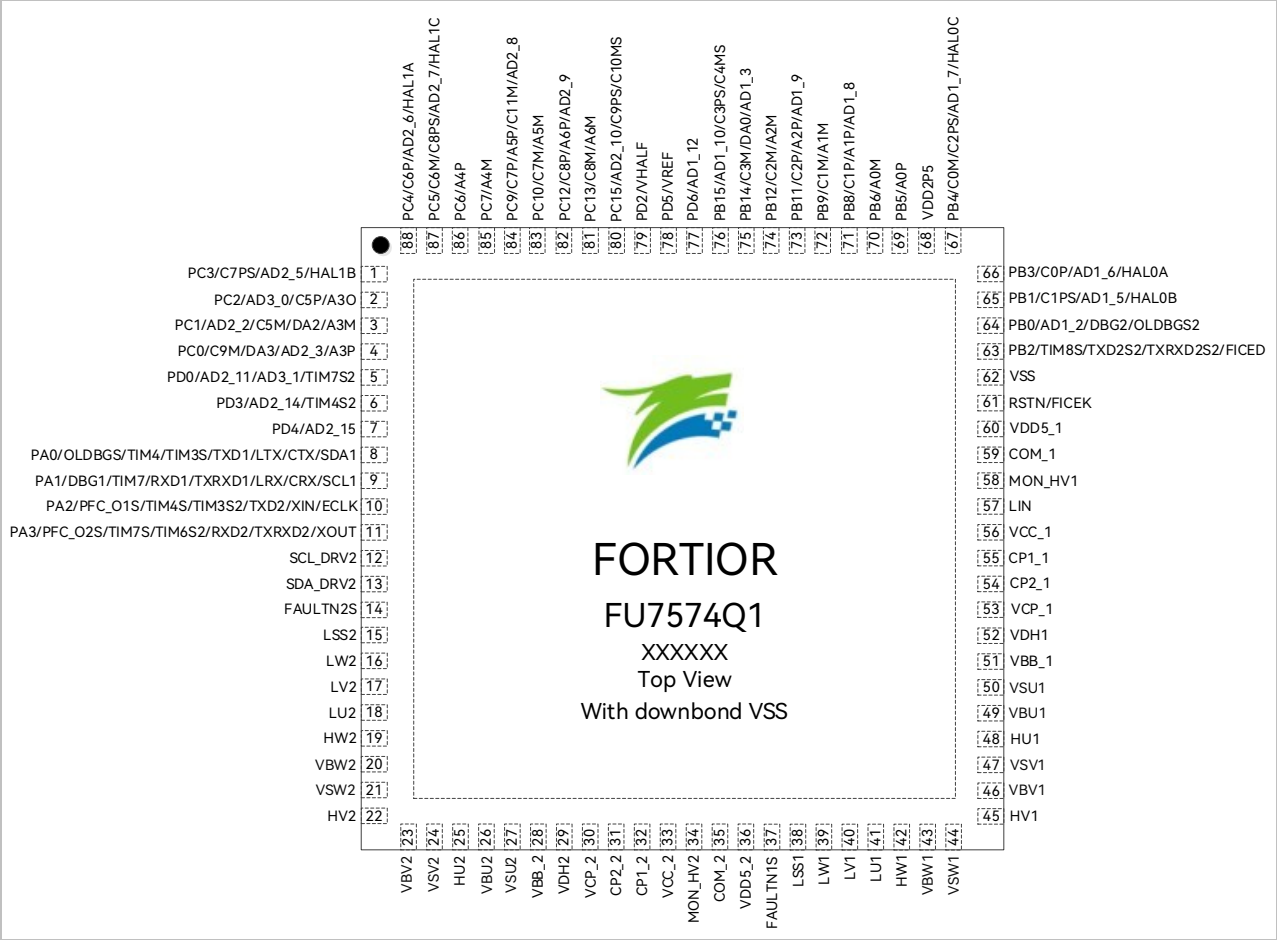
Pin	FU7574Q1 QFN88	IO Type	Description
HU1	48	DO	6N pre-driver1 high-side U-phase output
VBU1	49	P	6N pre-driver1 high-side U-phase bootstrap power supply
VSU1	50	P	6N pre-driver1 U-phase input, as GND reference for high-side U-phase bootstrap
VBB_1	51	P	Driver power supply, 11V LDO1, with a 1μF external capacitor connected to VSS. When VCC_1 ≥ 12V, it delivers an additional load capability of no less than 30mA.
VDH1	52	P	6N pre-driver1 high-side MOSFET drain voltage connection
VCP_1	53	P	Charge pump 1 output, with a 1μF external capacitor connected to VDH1 pin
CP2_1	54	DO	Charge pump 1 pin, with a 0.1μF capacitor connected to CP1_1 pin
CP1_1	55	DO	Charge pump 1 pin, with a 0.1μF capacitor connected to CP2_1 pin
VCC_1	56	P	Power input
LIN	57	DB	LIN bus
MON_HV1	58	DI	MON1 high-voltage input
COM_1	59	P	6N pre-driver1 ground
VDD5_1	60	P	5V LDO2 output with a 1μF ~ 4.7μF external capacitor
RSTN/ FICEK	61	DI/ DI	Input of external reset, with built-in pull-up resistor FICE clock line
VSS	62	P	MCU ground
PB2/ TIM8S/ TXD2S2/ TXRXD2S2/ FICED	63	DB/ DB/ DO/ DB/ DB	GPIO, configurable as EXT11/EXT12 input Timer8 input/output after function switching UART2 TXD output after the second function switching UART2 TXD output/RXD input in single-wire mode after the second function switching FICE data line
PB0/ AD1_2/ DBG2/ OLDBGS2	64	DB/ AI/ DO/ DO	GPIO, configurable as EXT12 input ADC1 channel 2 input; Bus voltage divider sampling input Debug2 output DataMonitor output after the second function switching
PB1/ C1PS/ AD1_5/ HAL0B	65	DB/ AI/ AI/ DI	GPIO, configurable as EXT12 input CMP1 positive input after function switching ADC1 channel 5 input Hall0 B input
PB3/ C0P/ AD1_6/ HAL0A	66	DB/ AI/ AI/ DI	GPIO, configurable as EXT12 input CMP0 positive input ADC1 channel 6 input Hall0 A input

Pin	FU7574Q1 QFN88	IO Type	Description
PB4/ C0M/ C2PS/ AD1_7/ HAL0C	67	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP0 negative input CMP2 positive input after function switching ADC1 channel 7 input Hall0 C input
VDD2P5	68	P	2.5V LDO3 output, with an external capacitor of 1μF or above
PB5/ A0P	69	DB/ AI	GPIO, configurable as EXTI2 input AMP0 positive input
PB6/ A0M	70	DB/ AI	GPIO, configurable as EXTI2 input AMP0 negative input
PB8/ C1P/ A1P/ AD1_8	71	DB/ AI/ AI/ AI	GPIO CMP1 positive input AMP1 positive input ADC1 channel 8 input
PB9/ C1M/ A1M	72	DB/ AI/ AI	GPIO CMP1 negative input AMP1 negative input
PB11/ C2P/ A2P/ AD1_9	73	DB/ AI/ AI/ AI	GPIO CMP2 positive input AMP2 positive input ADC1 channel 9 input
PB12/ C2M/ A2M	74	DB/ AI/ AI	GPIO CMP2 negative input AMP2 negative input
PB14/ C3M/ DA0/ AD1_3	75	DB/ AI/ AO/ AI	GPIO CMP3 negative input DAC0 output ADC1 channel 3 input
PB15/ AD1_10/ C3PS/ C4MS	76	DB/ AI/ AI/ AI	GPIO ADC1 channel 10 input CMP3 positive input after function switching CMP4 negative input after function switching
PD6/ AD1_12	77	DB/ AI	GPIO ADC1 channel 12 input
PD5/ VREF	78	DB/ AB	GPIO ADC external VREF input or internal VREF output, with a 1μF ~ 4.7μF external capacitor
PD2/ VHALF	79	DB/ AO	GPIO 1/2 VREF voltage output, with a 1μF external capacitor

Pin	FU7574Q1 QFN88	IO Type	Description
PC15/ AD2_10/ C9PS/ C10MS	80	DB/ AI/ AI/ AI	GPIO ADC2 channel 10 input CMP9 positive input after function switching CMP10 negative input after function switching
PC13/ C8M/ A6M	81	DB/ AI/ AI	GPIO CMP8 negative input AMP6 negative input
PC12/ C8P/ A6P/ AD2_9	82	DB/ AI/ AI/ AI	GPIO CMP8 positive input AMP6 positive input ADC2 channel 9 input
PC10/ C7M/ A5M	83	DB/ AI/ AI	GPIO CMP7 negative input AMP5 negative input
PC9/ C7P/ A5P/ C11M/ AD2_8	84	DB/ AI/ AI/ AI/ AI	GPIO CMP7 positive input AMP5 positive input CMP11 negative input ADC2 channel 8 input
PC7/ A4M	85	DB/ AI	GPIO, configurable as EXTI2 input AMP4 negative input
PC6/ A4P	86	DB/ AI	GPIO, configurable as EXTI2 input AMP4 positive input
PC5/ C6M/ C8PS/ AD2_7/ HAL1C	87	DB/ AI/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 negative input CMP8 input after function switching ADC2 channel 7 input Hall1 C-phase input
PC4/ C6P/ AD2_6/ HAL1A	88	DB/ AI/ AI/ DI	GPIO, configurable as EXTI2 input CMP6 positive input ADC2 channel 6 input Hall1 A-phase input

2.8 FU7574Q1 QFN88 Pinout Diagram

Figure 2–4 FU7574Q1 QFN88 Pinout Diagram



2.9 FU7512_64_65_74Q1 Functions and Pins Comparison

Table 2-5 FU7512_64_65_74Q1 Functions and Pins Comparison

Functions	Pin	FU7512Q1 GPIO	FU7564Q1 GPIO	FU7565Q1 GPIO	FU7574Q1 GPIO
CMPG1	C0P	PB3	PB3	PB3	PB3
	C0M	PB4	PB4	PB4	PB4
	C1P	PB8	PB8	PB8	PB8
	C1PS	PB1	PB1	PB1	PB1
	C1M	PB9	PB9	-	PB9
	C2P	PB11	PB11	-	PB11
	C2PS	PB4	PB4	PB4	PB4
	C2M	PB12	PB12	-	PB12
CMPG2	C6P	PC4	PC4	-	PC4
	C6M	PC5	PC5	-	PC5
	C7P	PC9	-	PC9	PC9
	C7PS	PC3	PC3	-	PC3
	C7M	PC10	-	PC10	PC10
	C8P	PC12	-	-	PC12
	C8PS	PC5	PC5	-	PC5
	C8M	PC13	-	-	PC13
CMP3	C3P	PB7	-	-	-
	C3PS	PB15	PB15	PB15	PB15
	C3M	-	-	-	PB14
CMP9	C9P	-	-	-	-
	C9PS	PC15	PC15	-	PC15
	C9M	PC0	-	-	PC0
CMP4	C4P	PB13	-	-	-
	C4M	PB7	-	-	-
	C4MS	PB15	PB15	PB15	PB15
CMP10	C10P	-	-	-	-
	C10M	-	-	-	-
	C10MS	PC15	PC15	-	PC15
CMP5	C5P	PC2	-	-	PC2
	C5M	PC1	-	-	PC1
CMP11	C11P	-	-	PC11	-
	C11M	PC9	PC9	PC9	PC9

Functions	Pin	FU7512Q1 GPIO	FU7564Q1 GPIO	FU7565Q1 GPIO	FU7574Q1 GPIO
AMP0	A0P	PB5	PB5	PB5	PB5
	A0M	PB6	PB6	PB6	PB6
	A0O	PB7	-	-	-
AMP4	A4P	PC6	PC6	-	PC6
	A4M	PC7	PC7	-	PC7
	A4O	-	-	-	-
AMP1	A1P	PB8	PB8	PB8	PB8
	A1M	PB9	PB9	-	PB9
	A1O	PB10	-	-	-
AMP2	A2P	PB11	PB11	-	PB11
	A2M	PB12	PB12	-	PB12
	A2O	PB13	-	-	-
AMP5	A5P	PC9	-	PC9	PC9
	A5M	PC10	-	PC10	PC10
	A5O	-	-	PC11	-
AMP6	A6P	PC12	-	-	PC12
	A6M	PC13	-	-	PC13
	A6O	-	-	-	-
AMP3	A3P	PC0	-	-	PC0
	A3M	PC1	-	-	PC1
	A3O	PC2	-	-	PC2
DAC	DAC0	PB14	-	-	PB14
	DAC1	PB13	-	-	-
	DAC2	PC1	-	-	PC1
	DAC3	PC0	-	-	PC0
	DAC4	-	-	-	-
Bus Voltage Sampling	AD1_2	PB0	PB0	PB0	PB0
Bus Current Sampling	AD1_4	PB7	-	-	-
	AD2_4	-	-	-	-
U-phase Current Sampling	AD1_0	PB10	-	-	-
	AD2_0	-	-	PC11	-
V-phase Current Sampling	AD1_1	PB13	-	-	-
	AD2_1	-	-	-	-

Functions	Pin	FU7512Q1 GPIO	FU7564Q1 GPIO	FU7565Q1 GPIO	FU7574Q1 GPIO
PFC	AD3_1	PD0	-	-	PD0
	AD1_2	PB0	PB0	PB0	PB0
	PFC_O1	PA6	-	-	-
	PFC_O1S	PA2	-	-	PA2
	A3P	PC0	-	-	PC0
	A3M	PC1	-	-	PC1
	A3O	PC2	-	-	PC2
	PFC_O2	PA7	-	-	-
	PFC_O2S	PA3	-	-	PA3
	A5P	PC9	-	PC9	PC9
	A5M	PC10	-	PC10	PC10
	A5O	-	-	PC11	-
Hall-IC Input	HAL0A	PB3	PB3	PB3	PB3
	HAL0B	PB1	PB1	PB1	PB1
	HAL0C	PB4	PB4	PB4	PB4
	HAL1A	PC4	PC4	-	PC4
	HAL1B	PC3	PC3	-	PC3
	HAL1C	PC5	PC5	-	PC5
Timer2	TIM2	PA10	PA10	PA10	-
	TIM2S	PA11	PA11	PA11	-
Timer5	TIM5	PA13	PA13	-	-
	TIM5S	PA14	PA14	-	-
	TIM5S2	PA4	-	-	-
	TIM5S3	PA5	-	-	-
Timer6	TIM6	PA7	-	-	-
	TIM6S	-	-	-	-
	TIM6S2	PA3	PA3	PA3	PA3
Timer3	TIM3	-	-	-	-
	TIM3S	PA0	PA0	PA0	PA0
	TIM3S2	PA2	PA2	PA2	PA2
Timer4	TIM4	PA0	PA0	PA0	PA0
	TIM4S	PA2	PA2	PA2	PA2
	TIM4S2	-	-	-	PD3

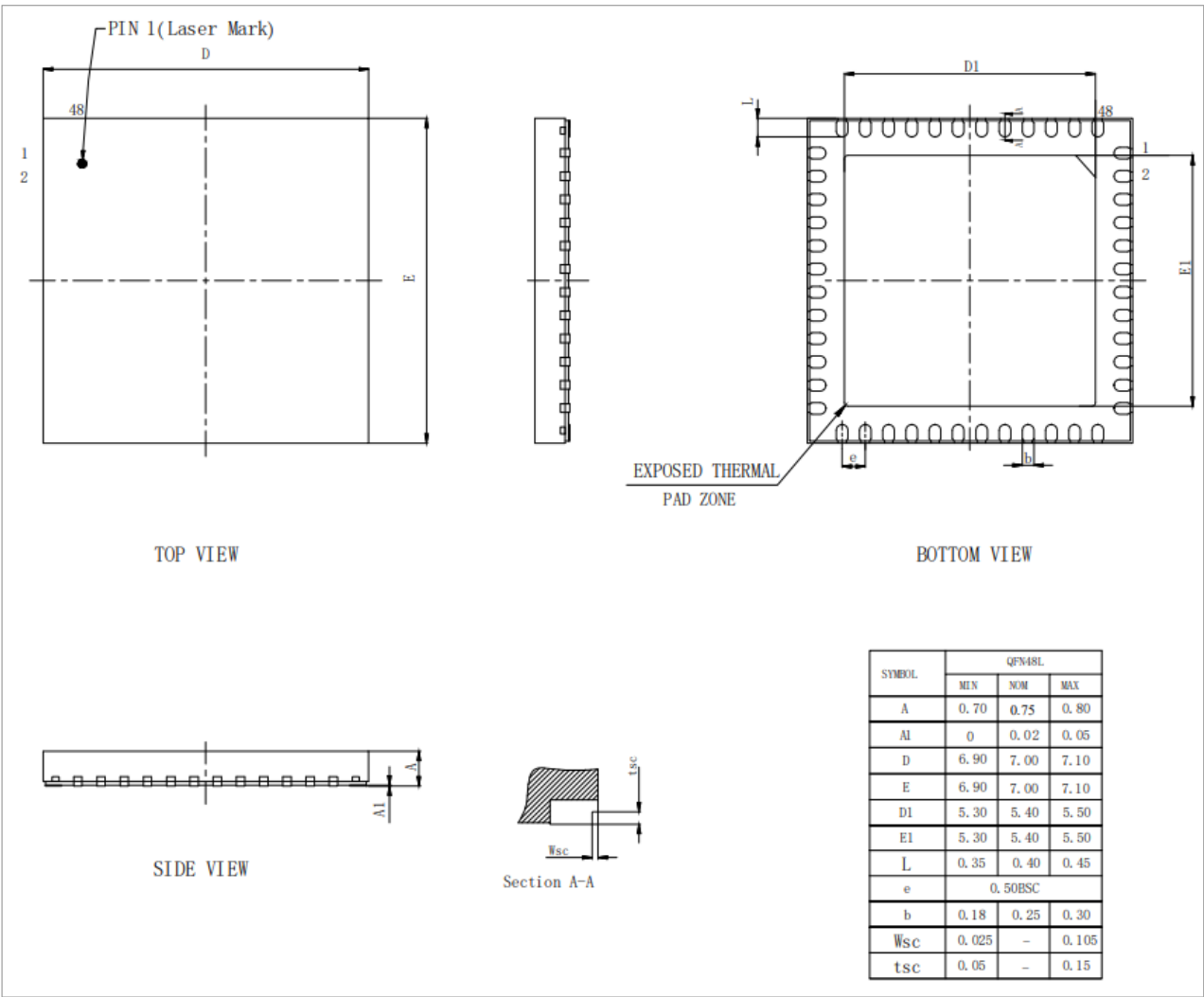
Functions	Pin	FU7512Q1 GPIO	FU7564Q1 GPIO	FU7565Q1 GPIO	FU7574Q1 GPIO
Timer7	TIM7	PA1	PA1	PA1	PA1
	TIM7S	PA3	PA3	PA3	PA3
	TIM7S2	PD0	-	PD0	PD0
Timer8	TIM8	PA9	-	-	-
	TIM8S	PB2	PB2	PB2	PB2
I ² C1	SCL1	PA1	PA1	PA1	PA1
	SDA1	PA0	PA0	PA0	PA0
I ² C2	SCL2	PA7	-	-	-
	SDA2	PA6	-	-	-
SPI1	SCLK1	PA6	-	-	-
	MOSI1	PA5	-	-	-
	MISO1	PA4	-	-	-
	NSS1	PA7	-	-	-
SPI2	SCLK2	PA12	PA12	PA12	-
	MOSI2	PA11	PA11	PA11	-
	MISO2	PA10	PA10	PA10	-
	NSS2	PA9	-	-	-
UART1	TXD1	PA0	PA0	PA0	PA0
	RXD1	PA1	PA1	PA1	PA1
	TXD1S	PA7	-	-	-
	RXD1S	PA6	-	-	-
	TXD1S2	PA10	PA10	PA10	-
	RXD1S2	PA11	PA11	PA11	-
	TXRXD1	PA1	PA1	PA1	PA1
	TXRXD1S	PA6	-	-	-
	TXRXD1S2	PA11	PA11	PA11	-
UART2	TXD2	PA2	PA2	PA2	PA2
	RXD2	PA3	PA3	PA3	PA3
	RXD2S	PA4	-	-	-
	TXD2S	PA5	-	-	-
	TXD2S2	PB2	PB2	PB2	PB2
	TXRXD2	PA3	PA3	PA3	PA3
	TXRXD2S	PA4	-	-	-
	TXRXD2S2	PB2	PB2	PB2	PB2

Functions	Pin	FU7512Q1 GPIO	FU7564Q1 GPIO	FU7565Q1 GPIO	FU7574Q1 GPIO
LIN	LTX	PA0	PA0	PA0	PA0
	LRX	PA1	PA1	PA1	PA1
	LTXS	PA5	-	-	-
	LRXS	PA4	-	-	-
LIN Transceiver	LIN	-	LIN	LIN	LIN
CAN	CTX	PA0	PA0	PA0	PA0
	CRX	PA1	PA1	PA1	PA1
	CTXS	PA5	-	-	-
	CRXS	PA4	-	-	-
BISS	MA	PA10	PA10	PA10	-
	MAS	PA13	PA13	-	-
	SLO	PA11	PA11	PA11	-
	SLOS	PA14	PA14	-	-
DataMonitor	OLDBG	PA9	-	-	-
	OLDBGS	PA0	PA0	PA0	PA0
	OLDBGS2	PB0	PB0	PB0	PB0
VREF Output	VREF	PD5	PD5	PD5	PD5
VHALF Output	VHALF	PD2	-	-	PD2
Debug Signal Detection	DBG1	PA1	PA1	PA1	PA1
	DBG1S	PA9	-	-	-
	DBG2	PB0	PB0	PB0	PB0
FICE Interface	FICEK	RSTN	RSTN	RSTN	RSTN
	FICED	PB2	PB2	PB2	PB2
Low-power Sleep Wake-up	LIN or MON_HVx	-	LIN or MON_HV1	LIN or MON_HV1	LIN and MON_HV2 MON_HV1 and MON_HV2
Charge Pump 1	CP1_1	-	CP1_1	CP1_1	CP1_1
	CP2_1 or SW	-	CP2_1	SW	CP2_1
	VCP_1	-	VCP_1	VCP_1	VCP_1
Charge Pump 2	CP1_2	-	-	-	CP1_2
	CP2_2	-	-	-	CP2_2
	VCP_2	-	-	-	VCP_2
6N Pre-driver1 VDS OVP	VDH1	-	VDH1	VDH1	VDH1
	VSU1/V1/W1	-	VSU1/V1/W1	VSU1/V1/W1	VSU1/V1/W1
	LSS1	-	LSS1	LSS1	LSS1
6N Pre-driver2 VDS OVP	VDH2	-	-	-	VDH2
	VSU2/V2/W2	-	-	-	VSU2/V2/W2
	LSS2	-	-	-	LSS2

3 Package Information

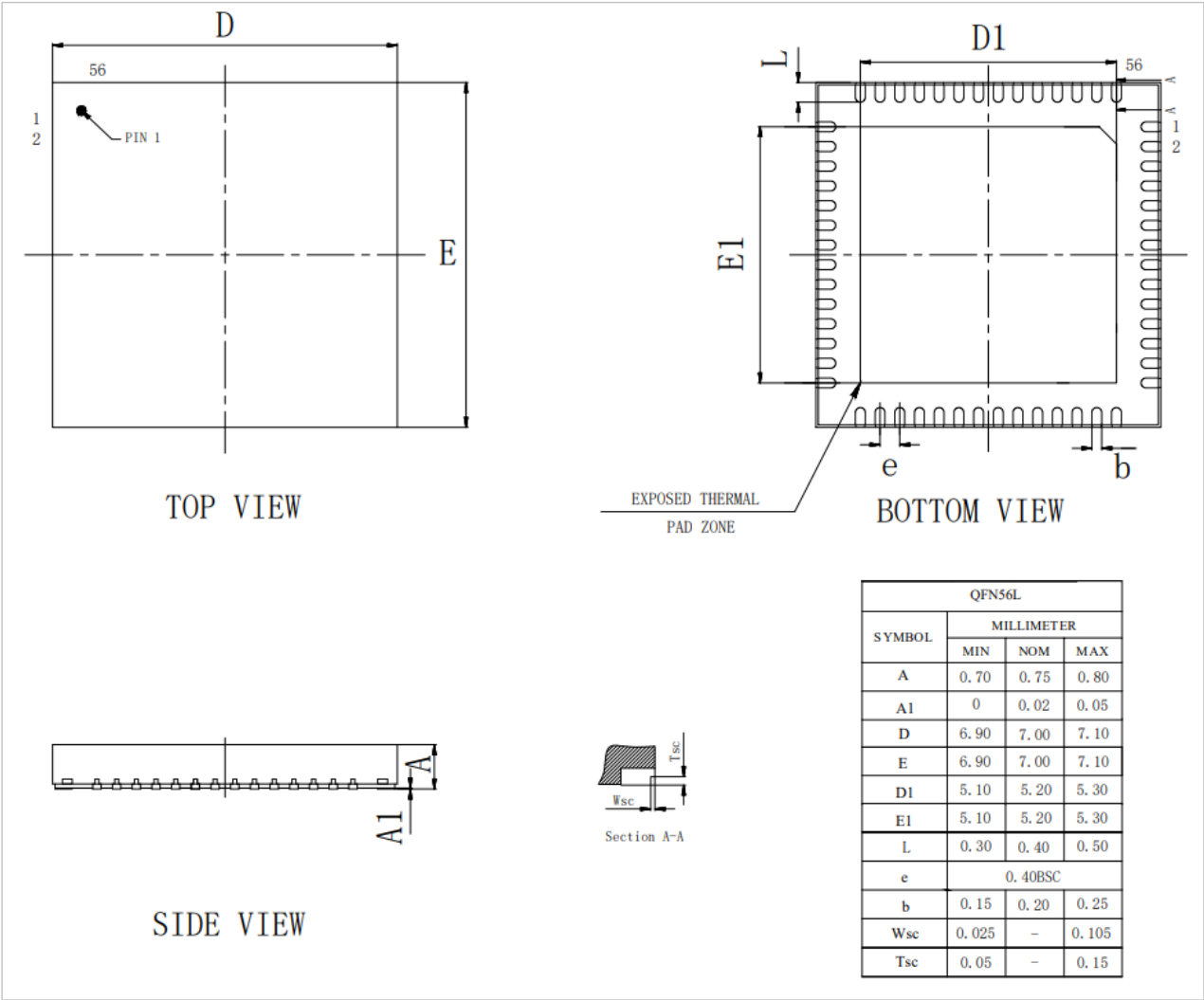
3.1 QFN48_7X7 (FU7565Q1)

Figure 3-1 QFN48_7X7 Package Drawings and Dimensions



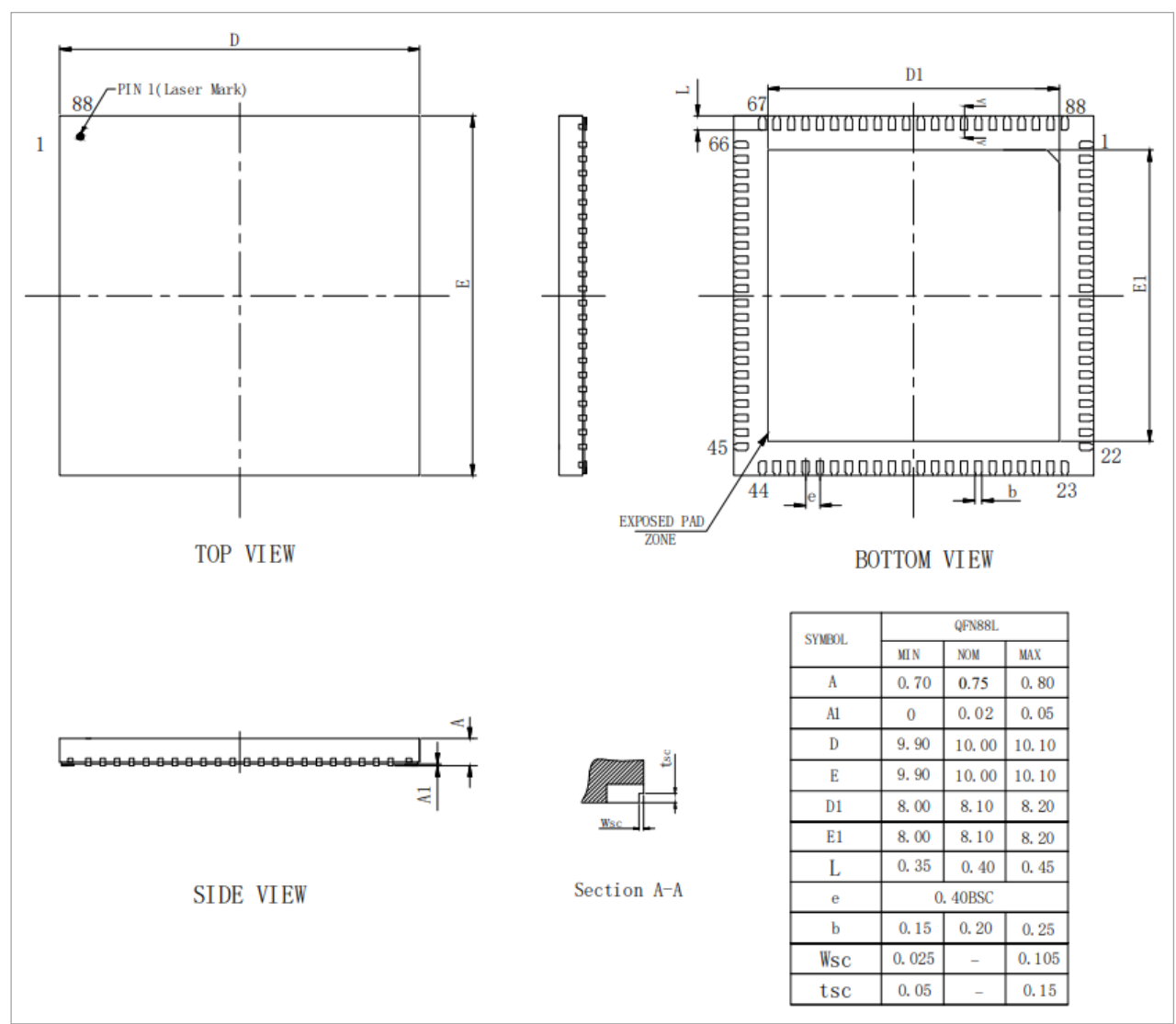
3.2 QFN56_7X7 (FU7512Q1/FU7564Q1)

Figure 3-2 QFN56_7X7 Package Drawings and Dimensions



3.3 QFN88_10X10 (FU7574Q1)

Figure 3-3 QFN88_10X10 Package Drawings and Dimensions



4 Ordering Information

Table 4-1 Model Selections

Model	System Clock (MHz)	Flash (KB)	SRAM (KB)	PRAM (KB)	Clock Circuit			Driver Interface				Driver Type	Communication Interface			Buck DC-DC Converter	DMA	GPIO	LIN Transceiver	Charge Pump	Timer	PFC	Analog Peripherals								Lead-free	Package		
					Internal Fast Clock	Internal Slow Clock	External Fast Clock	PWM		3P3N Pre-driver	6N Pre-driver		FOC	I ² C/UART/LIN/CANFD	BISS								SPI		ADC			DAC		VREF			Operational Amplifier	Comparator
								PWM1	PWM2		6N Pre-driver1	6N Pre-driver2											SPI1	SPI2	Unit	Channel	Bit	Unit	Bit					
FU7512Q1	48/24	64	12	4	√	√	√	√	√	-	-	-	√	√	√	√	-	√	46	-	-	9	√	3	28	12	5	9/8/6	√	7	8	√	QFN56 (7x7mm)	
FU7564Q1	48/24	64	12	4	√	√	√	-	√	-	√	-	√	√	-	√	-	√	29	√	1	9	-	2	20	12	4	9/6	√	4	6	√	QFN56 (7x7mm)	
FU7565Q1	48/24	64	12	4	√	√	√	-	-	-	√	-	√	√	-	√	√	√	21	√	1	9	-	2	14	12	2	9/6	√	3	4	√	QFN48 (7x7mm)	
FU7574Q1	48/24	64	12	4	√	√	√	-	-	-	√	√	√	√	-	-	-	√	36	√	2	9	√	3	31	12	5	9/8/6	√	7	8	√	QFN88 (10x10mm)	

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stress values greater than "Absolute Maximum Ratings" listed below may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

5.1.1 FU7512Q1

Table 5-1 Absolute Maximum Ratings of FU7512Q1

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	°C
Storage Temperature T_{STG}		-55	-	150	°C
VDD5 to VSS Voltage		-0.3	-	6.5	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V

5.1.2 FU7564Q1

Table 5-2 Absolute Maximum Ratings of FU7564Q1^[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	°C
Storage Temperature T_{STG}		-55	-	150	°C
VCC to VSS Voltage	Chip Standby with Pre-driver1 Output Off	-0.3	-	40	V
VCC to VSS Voltage	Peak Duration < 60s	-0.3	-	42	V
VCC to VSS Voltage	Peak Duration < 500ms	-0.3	-	45	V
VBB to VSS Voltage		-0.3	-	16	V
VDD5 to VSS Voltage ^[2]		-0.3	-	6.5	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V
CP1 Charge Pump Voltage V_{CP1}		-0.3	-	40	V
CP2 Charge Pump Voltage V_{CP2}		-0.3	-	60	V
Charge Pump Output Voltage V_{VCP_1}		-0.3	-	60	V
VVCP_1 to VCC Voltage $V_{VCP\_1} - V_{CC}$		-0.3	-	16	V
High-side MOSFET Drain Voltage V_{DH1}		-0.3	-	40	V
High-side Bootstrap Voltage for Phase U/V/W V_{BU1} , V_{BV1} , V_{BW1}		-0.3	-	60	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-side Floating Offset Voltage for Phase U/V/W $V_{SU1}, V_{SV1}, V_{SW1}$		-10	-	40	V
High-side Output Voltage for Phase U/V/W $V_{HU1}, V_{HV1}, V_{HW1}$		-0.3	-	60	V
Low-side Output Voltage for Phase U/V/W $V_{LU1}, V_{LV1}, V_{LW1}$		-0.3	-	16	V
Low-side MOSFET Source Voltage V_{LSS1}		-0.3	-	6	V
LIN Voltage V_{LIN}	LIN to VCC/VSS	-40	-	40	V
MON_HV1 Input Voltage V_{MON_HV1}		-0.3	-	40	V
Power Dissipation P_D ^[3]	$T_A \leq 25^\circ\text{C}$	-	-	0.625	W



Note:

[1] All pins are referenced to VSS unless otherwise specified

[2] VDD5 must be in the range of 5V~5.5V during Flash write or erase.

[3] In any case, power dissipation shall not exceed PD.

5.1.3 FU7565Q1

Table 5-3 Absolute Maximum Ratings of FU7565Q1^[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	$^\circ\text{C}$
Storage Temperature T_{STG}		-55	-	150	$^\circ\text{C}$
VCC to VSS Voltage	Chip Standby with Pre-driver Output Off	-0.3	-	80	V
VCC to VSS Voltage	Peak Duration < 60s	-0.3	-	85	V
VCC to VSS Voltage	Peak Duration < 500ms	-0.3	-	90	V
VBB to VSS Voltage		-0.3	-	16	V
VDD5 to VSS Voltage ^[2]		-0.3	-	6.5	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5 + 0.3	V
Charge Pump Voltage V_{CP1_1}		-0.3	-	90	V
Buck DC-DC Converter Inductor Voltage V_{BSW}		-0.3	-	90	V
Charge Pump Output Voltage V_{VCP_1}		-0.3	-	110	V
VVCP_1 to VCC Voltage $V_{VCP\_1} - V_{CC}$		-0.3	-	20	V
High-side MOSFET Drain Voltage V_{VDH1}		-0.3	-	90	V
High-side Bootstrap Voltage for Phase U/V/W $V_{BU1}, V_{BV1}, V_{BW1}$		-0.3	-	110	V
High-side Floating Offset Voltage for Phase U/V/W $V_{SU1}, V_{SV1}, V_{SW1}$		-10	-	90	V
High-side Output Voltage for Phase U/V/W $V_{HU1}, V_{HV1}, V_{HW1}$		-0.3	-	110	V
Low-side Output Voltage for Phase U/V/W $V_{LU1}, V_{LV1}, V_{LW1}$		-0.3	-	16	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LW1}					
Low-side MOSFET Source Voltage V_{LSS1}		-0.3	-	6	V
LIN Voltage V_{LIN}	LIN to VBB/VSS	-40	-	40	V
MON_HV1 Input Voltage V_{MON_HV1}		-0.3	-	40	V
Power Dissipation $P_D^{[3]}$	$T_A \leq 25^\circ\text{C}$	-	-	0.625	W



Note:

[1] All pins are referenced to VSS unless otherwise specified

[2] VDD5 must be in the range of 5V~5.5V during Flash write or erase.

[3] In any case, power dissipation shall not exceed PD.

5.1.4 FU7574Q1

Table 5-4 Absolute Maximum Ratings of FU7574Q1^[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_J		-40	-	150	$^\circ\text{C}$
Storage Temperature T_{STG}		-55	-	150	$^\circ\text{C}$
VCC_x to VSS Voltage	Chip Standby with Pre-driverx Output Off	-0.3	-	40	V
VCC_x to VSS Voltage	Peak Duration < 60s	-0.3	-	42	V
VCC_x to VSS Voltage	Peak Duration < 500ms	-0.3	-	45	V
VBB_x to VSS Voltage		-0.3	-	16	V
VDD5_x to VSS Voltage ^[2]		-0.3	-	6.5	V
RSTN/GPIO to VSS Voltage		-0.3	-	VDD5_x + 0.3	V
CP1 Charge Pump Voltage V_{CP1_x}		-0.3	-	40	V
CP2 Charge Pump Voltage V_{CP2_x}		-0.3	-	60	V
Charge Pump Output Voltage V_{VCP_x}		-0.3	-	60	V
VVCP_x to VCC Voltage $V_{VCP\_x} - V_{CC\_x}$		-0.3	-	16	V
High-side MOSFET Drain Voltage V_{DHx}		-0.3	-	40	V
High-side Bootstrap Voltage for Phase U/V/W V_{BUx} , V_{BVx} , V_{BWx}		-0.3	-	60	V
High-side Floating Offset Voltage for Phase U/V/W V_{SUx} , V_{SVx} , V_{SWx}		-10	-	40	V
High-side Output Voltage for Phase U/V/W V_{HUx} , V_{HVx} , V_{HWx}		-0.3	-	60	V
Low-side Output Voltage for Phase U/V/W V_{LUx} , V_{LVx} , V_{LWx}		-0.3	-	16	V
Low-side MOSFET Source Voltage V_{LSSx}		-0.3	-	6	V
LIN Voltage V_{LIN}	LIN to VCC_x/VSS	-40	-	40	V
MON_HVx Input Voltage V_{MON_HVx}		-0.3	-	40	V
Power Dissipation $P_D^{[3]}$	$T_A \leq 25^\circ\text{C}^\circ$	-	-	0.625	W



Note:

- [1] All pins are referenced to VSS unless otherwise specified
- [2] VDD5_x must be in the range of 5V~5.5V during Flash write or erase.
- [3] In any case, power dissipation shall not exceed PD.

5.2 Global Electrical Characteristics

5.2.1 FU7512Q1

Table 5-5 Global Electrical Characteristics of FU7512Q1

(T_A = -40°C ~ 125°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Operating Voltage ^[1]		3	5	5.5	V
I _{VDD5} Operating Current ^[2]	System clock 24M	-	15	-	mA
I _{VDD5} Operating Current ^[2]	System clock 48M	-	20	-	mA
I _{VDD5} Standby Current	All Peripherals Powered Off	-	1.5	-	mA
I _{VDD5} Sleep-mode Current		-	20	-	μA
Operating Ambient Temperature T _A		-40	-	125	°C



Note:

- [1] VDD5 must be in the range of 5V ~ 5.5V during Flash write or erase.
- [2] Characteristics may vary with different configurations.

5.2.2 FU7564Q1

Table 5-6 Global Electrical Characteristics of FU7564Q1

(T_A = -40°C ~ 125°C and VCC = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage ^[1]		5.5	-	18	V
I _{VCC} Operating Current ^[2]	System Clock 24M and VCC = 15V	-	20	-	mA
I _{VCC} Operating Current ^[2]	System Clock 48M and VCC = 15V	-	25	-	mA
I _{VCC} Standby Current	All Peripherals Powered Off, and VCC = 15V	-	8	-	mA
I _{VCC} Sleep-mode Current	VCC = 15V, SLPF_R[SLP_FORCE] = 1	-	40	-	μA
Operating Ambient Temperature T _A		-40	-	125	°C



Note:

- [1] VCC voltage rise rate ranges from 0.5V/μs ~ 0.1V/s depending on samples batches.
- [2] Characteristics may vary with different configurations.

5.2.3 FU7565Q1

Table 5-7 Global Electrical Characteristics of FU7565Q1

(T_A = -40°C ~ 125°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage ^[1]	VTLW_R[VCCOVS] = 00	22	-	60	V
	VTLW_R[VCCOVS] = 01	9	-	40	V
IVCC Operating Current ^[2]	System Clock 24M and VCC = 24V	-	20	-	mA
IVCC Operating Current ^[2]	System Clock 48M and VCC = 24V	-	25	-	mA
IVCC Standby Current	All Peripherals Powered Off, and VCC = 24V	-	5	-	mA
IVCC Sleep-mode Current	VCC = 24V, SLPF_R[SLP_FORCE] = 1	-	75	-	μA
Operating Ambient Temperature T _A		-40	-	125	°C



Note:

[1] VCC voltage rise rate ranges from 0.5V/μs ~ 0.1V/s depending on samples batches.

[2] Characteristics may vary with different configurations.

5.2.4 FU7574Q1

Table 5-8 Global Electrical Characteristics of FU7574Q1

(T_A = -40°C ~ 125°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC_x Operating Voltage ^[1]		5.5	-	18	V
I _{VCC_1} Operating Current ^[2]	System Clock 24M and VCC_1 = 15V	-	20	-	mA
I _{VCC_1} Operating Current ^[2]	System Clock 48M and VCC_1 = 15V	-	25	-	mA
I _{VCC_1} Standby Current	All Peripherals Powered Off, and VCC_1 = 15V	-	8	-	mA
I _{VCC_1} Sleep-mode Current	VCC_1 = 15V, SLPF_R[SLP_FORCE] = 1	-	40	-	μA
I _{VCC_2} Operating Current	VCC_2 = 15V	-	3	-	mA
I _{VCC_2} Quiescent Current	VCC_2 = 15V	-	20	-	μA
Operating Ambient Temperature T _A		-40	-	125	°C



Note:

[1] VCC_x voltage rise rate ranges from 0.5V/μs ~ 0.1V/s depending on samples batches.

[2] Characteristics may vary with different configurations.

5.3 GPIO Electrical Characteristics

5.3.1 FU7512Q1

Table 5-9 GPIO Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%,	-	15	-	ns

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	$T_A = 25^\circ\text{C}$				
Turn-off Fall Time	50pF load, from 90% to 10%, $T_A = 25^\circ\text{C}$	–	13	–	ns
V_{OH} High-level Output Voltage ^[1]	$I_{OH} = 4\text{mA}$ and $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$	$V_{DD5} - 0.7$	–	–	V
V_{OL} Low-level Output Voltage	$I_{OL} = 4\text{mA}$ and $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$	–	–	$V_{SS} + 0.7$	V
V_{IH} High-level Input Voltage		$0.7 \cdot V_{DD5}$	–	–	V
V_{IL} Low-level Input Voltage		–	–	$0.2 \cdot V_{DD5}$	V
Pull-up Resistor ^[2]		–	30	–	k Ω
Pull-up Resistor ^[3]		–	5.6	–	k Ω
Pull-down Resistor ^[4]		–	30	–	k Ω



Note:

[1] The high-level output voltage is referenced to and follows V_{DD5} .[2] Except for GPIOs in [3], all other GPIOs are configured with a 30k Ω pull-up resistor.

[3] PA[0:7], PB[1], PB[3:4], PC[3:5]

[4] PA[0:1], PA[4:7], PA[9:15]

5.3.2 FU7564Q1

Table 5-10 GPIO Electrical Characteristics of FU7564Q1

 $(T_A = 25^\circ\text{C}$ and $V_{CC} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, $T_A = 25^\circ\text{C}$	–	15	–	ns
Turn-off Fall Time	50pF load, from 90% to 10%, $T_A = 25^\circ\text{C}$	–	13	–	ns
V_{OH} High-level Output Voltage ^[1]	$I_{OH} = 4\text{mA}$ and $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$	$V_{DD5} - 0.7$	–	–	V
V_{OL} Low-level Output Voltage	$I_{OL} = 4\text{mA}$ and $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$	–	–	$V_{SS} + 0.7$	V
V_{IH} High-level Input Voltage		$0.7 \cdot V_{DD5}$	–	–	V
V_{IL} Low-level Input Voltage		–	–	$0.2 \cdot V_{DD5}$	V
Pull-up Resistor ^[2]		–	30	–	k Ω
Pull-up Resistor ^[3]		–	5.6	–	k Ω
Pull-down Resistor ^[4]		–	30	–	k Ω



Note:

[1] The high-level output voltage is referenced to and follows V_{DD5} .[2] Except for GPIOs in [3], all other GPIOs are configured with a 30k Ω pull-up resistor.

[3] PA[0:3], PB[1], PB[3:4], PC[3:5]

[4] PA[0:1], PA[10:15]

5.3.3 FU7565Q1

Table 5-11 GPIO Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, T _A = 25°C	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T _A = 25°C	-	13	-	ns
V _{OH} High-level Output Voltage ^[1]	I _{OH} = 4mA and T _A = -40°C ~ 125°C	VDD5 - 0.7	-	-	V
V _{OL} Low-level Output Voltage	I _{OL} = 4mA and T _A = -40°C ~ 125°C	-	-	VSS + 0.7	V
V _{IH} High-level Input Voltage		0.7*VDD5	-	-	V
V _{IL} Low-level Input Voltage		-	-	0.2*VDD5	V
Pull-up Resistor ^[2]		-	30	-	kΩ
Pull-up Resistor ^[3]		-	5.6	-	kΩ
Pull-down Resistor ^[4]		-	30	-	kΩ



Note:

[1] The high-level output voltage is referenced to and follows VDD5.

[2] Except for GPIOs in [3], all other GPIOs are configured with a 30kΩ pull-up resistor.

[3] PA[0: 3], PB[1], PB[3: 4]

[4] PA[0: 1], PA[10: 12]

5.3.4 FU7574Q1

Table 5-12 GPIO Electrical Characteristics of FU7574Q1

(T_A = 25°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Rise Time	50pF load, from 10% to 90%, T _A = 25° C	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T _A = 25° C	-	13	-	ns
V _{OH} High-level Output Voltage ^[1]	I _{OH} = 4mA and T _A = -40°C ~ 125°C	VDD5 _x - 0.7	-	-	V
V _{OL} Low-level Output Voltage	I _{OL} = 4mA and T _A = -40°C ~ 125°C	-	-	VSS + 0.7	V
V _{IH} High-level Input Voltage		0.7*VDD5 _x	-	-	V
V _{IL} Low-level Input Voltage		-	-	0.2*VDD5 _x	V
Pull-up Resistor ^[2]		-	30	-	kΩ
Pull-up Resistor ^[3]		-	5.6	-	kΩ
Pull-down Resistor ^[4]		-	30	-	kΩ



Note:

[1] The high-level output voltage is referenced to and follows VDD5_x.

[2] Except for GPIOs in [3], all other GPIOs are configured with a 30kΩ pull-up resistor.

[3] PA[0:3], PB[1], PB[3:4], PC[3:5]

[4] PA[0:1]

5.4 PWM IO Electrical Characteristics (FU7512Q1/FU7564Q1)

5.4.1 FU7512Q1

5.4.1.1 PWM1 IO Electrical Characteristics of FU7512Q1

Table 5-13 PWM1 IO Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	T _A = -40°C ~ 125°C	-	4	-	mA
Output Sink Current	T _A = -40°C ~ 125°C	-	4	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T _A = 25°C	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T _A = 25°C	-	13	-	ns

5.4.1.2 PWM2 IO Electrical Characteristics of FU7512Q1

Table 5-14 PWM2 IO Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	T _A = -40°C ~ 125°C	-	4	-	mA
Output Sink Current	T _A = -40°C ~ 125°C	-	4	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T _A = 25°C	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T _A = 25°C	-	13	-	ns

5.4.2 FU7564Q1

5.4.2.1 PWM2 IO Electrical Characteristics of FU7564Q1

Table 5-15 PWM2 IO Electrical Characteristics of FU7564Q1

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output Source Current	T _A = -40°C ~ 125°C	-	4	-	mA
Output Sink Current	T _A = -40°C ~ 125°C	-	4	-	mA
Turn-on Rise Time	50pF load, from 10% to 90%, T _A = 25°C	-	15	-	ns
Turn-off Fall Time	50pF load, from 90% to 10%, T _A = 25°C	-	13	-	ns

5.5 6N Pre-driver Electrical Characteristics

(FU7564Q1/FU7565Q1/FU7574Q1)

5.5.1 6N Pre-driver1 Electrical Characteristics of FU7564Q1

5.5.1.1 6N Pre-driver1 Electrical Parameters of FU7564Q1

Table 5-16 6N Pre-driver1 Electrical Parameters of FU7564Q1

($T_A = 25^\circ\text{C}$ and $V_{CC} = 15\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Forward Voltage V_{F_BOOT}	$I_F = 10\text{mA}$	0.5	0.8	1.1	V
	$I_F = 100\text{mA}$	1.5	2.2	2.8	V
High-side Pull-down Resistor R_{GHPD}	$V_{CC} = 0\text{V}, V_{HU/VW1} - V_{SU/VW1} < 0.1\text{V}$	–	950	–	k Ω
Low-side Pull-down Resistor R_{GLPD}	$V_{CC} = 0\text{V}, V_{LU/VW1} - V_{LSS1} < 0.1\text{V}$	–	950	–	k Ω
High-side Drive Sink Current I_{HF}	Turn-off Sink Current	–	800	–	mA
High-side Drive Source Current I_{HR}	Turn-on Source Current	–	400	–	mA
Low-side Drive Sink Current I_{LF}	Turn-off Sink Current	–	800	–	mA
Low-side Drive Source Current I_{LR}	Turn-on Source Current	–	400	–	mA
High-side Output Voltage (On-state) V_{GHH}	Bootstrap Capacitor Fully Charged	$V_{BU/VW1} - 0.2$	–	–	V
High-side Output Voltage (Off-state) V_{GHL}	$-10\mu\text{A} < I_{GH} < 10\mu\text{A}$	–	–	$V_{SU/VW1} + 0.3$	V
Low-side Output Voltage (On-state) V_{GLH}	Bootstrap Capacitor Fully Charged	$V_{BB} - 0.2$	–	–	V
Low-side Output Voltage (Off-state) V_{GLL}	$-10\mu\text{A} < I_{GL} < 10\mu\text{A}$	–	–	$V_{LSS1} + 0.3$	V
Turn-off Propagation Delay $t_{P(off)}$	From Input to Unloaded Pre-driver1 Output	–	30	–	ns
Turn-on Propagation Delay $t_{P(on)}$		–	40	–	ns
High-side MOSFET Drain Voltage V_{VDH1}	With the V_{DS} Monitor Active	5.5	V_{CC}	40	V
VDH1 Input Current I_{VDH1}	$V_{DSTH} = \text{Default}, V_{CC} = 12\text{V}, 0\text{V} < V_{VDH1} < V_{CC}$	–	–	500	μA
VDH1 Sleep-mode Current I_{VDHQ}	$V_{CC} = 12\text{V}, \text{Sleep Mode}$	–	–	5	μA
Deadtime		–	95	–	ns

5.5.1.2 6N Pre-driver1 Protection Characteristics of FU7564Q1

Table 5-17 6N Pre-driver1 Protection Characteristics of FU7564Q1

($T_A = 25^\circ\text{C}$ and $V_{CC} = 15\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB UVLO Threshold Voltage V_{BBUVF}		4.6	4.7	5.2	V
VBB UVLO Release Voltage V_{BBUVR}		5.0	5.3	5.6	V
VBB UVLO Hysteresis Voltage $V_{BBUVhys}$		–	0.6	–	V
VCC UVLO Threshold Voltage V_{CCUVF}		–	4.8	–	V
VCC UVLO Release Voltage V_{CCUVR}		–	5.3	–	V
VCC UVLO Hysteresis Voltage $V_{CCUVhys}$		–	0.5	–	V
VCC OVP Warning Threshold Voltage V_{CCOVWR}		–	36.1	–	V
VCC OVP Warning Release Voltage V_{CCOVWF}		–	33.8	–	V
VCC OVP Warning Hysteresis Voltage $V_{CCOVWhys}$		–	2.3	–	V
VCC OVP Threshold Voltage V_{CCOVPR}		–	41.5	–	V
VCC OVP Release Voltage V_{CCOVPR}		–	40.0	–	V
VCC OVP Hysteresis Voltage $V_{CCOVPhys}$		–	1.5	–	V
VCC Power-on Reset Threshold Voltage V_{CCPORF}		–	2.3	–	V
VCC Power-On Reset Release Voltage V_{CCPORR}		–	2.4	–	V
VCC Power-On Reset Hysteresis Voltage $V_{CCPORhys}$		–	0.1	–	V
VDD5 UVLO Threshold Voltage V_{DD5UVF}		–	3.8	–	V
VDD5 UVLO Release Voltage V_{DD5UVR}		–	4.0	–	V
VDD5 UVLO Hysteresis Voltage $V_{DD5UVhys}$		–	0.2	–	V
Bootstrap UVLO Threshold Voltage V_{BUVF}	$V_{BOOT} = V_{BUV/W1} - V_{SU/V/W1}$	55	60	65	% V_{BB}
Bootstrap UVLO Release Voltage V_{BUVR}	$V_{BOOT} = V_{BUV/W1} - V_{SU/V/W1}$	65	70	75	% V_{BB}
Bootstrap UVLO Hysteresis Voltage V_{BUVhys}		–	10	–	% V_{BB}
Bootstrap OVP Threshold Voltage V_{BOVR}	$V_{BOOT} = V_{BUV/W1} - V_{SU/V/W1}$	175	185	195	% V_{BB}
Bootstrap OVP Release Voltage V_{BOVF}	$V_{BOOT} = V_{BUV/W1} - V_{SU/V/W1}$	165	175	185	% V_{BB}
Bootstrap OVP Hysteresis Voltage V_{BOVhys}		–	10	–	% V_{BB}
High-side VDS OVP Threshold $V_{DSTHU/V/W}$	Power-on Default	–	1.6	–	V
Low-side VDS OVP Threshold $V_{DSTLU/V/W}$	Power-on Default	–	1.6	–	V
VDS OVP Timer Duration $t_{VDQU/V/W}$	Power-on Default	–	3.2	–	μ s
Thermal Shutdown Threshold T_{SD}		–	165	–	$^{\circ}$ C
Thermal Shutdown Hysteresis T_{SDhys}		–	20	–	$^{\circ}$ C

5.5.2 6N Pre-driver1 Electrical Characteristics of FU7565Q1

5.5.2.1 6N Pre-driver1 Electrical Parameters of FU7565Q1

Table 5-18 6N Pre-driver1 Electrical Parameters of FU7565Q1

(T_A = 25 $^{\circ}$ C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Forward Voltage $V_{F,BOOT}$	$I_F = 10\text{mA}$	0.5	0.8	1.1	V
	$I_F = 100\text{mA}$	1.5	2.2	2.8	V
High-side Pull-down Resistor R_{GHDP}	$V_{CC} = 0\text{V}, V_{HU/V/W1} - V_{SU/V/W1} < 0.1\text{V}$	–	100	–	k Ω

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Low-side Pull-down Resistor R_{GLPD}	$V_{CC} = 0V, V_{LU/V/W1} - V_{LSS1} < 0.1V$	-	100	-	$k\Omega$
High-side Drive Sink Current I_{HF}	Turn-off Sink Current	-	800	-	mA
High-side Drive Source Current I_{HR}	Turn-on Source Current	-	400	-	mA
Low-side Drive Sink Current I_{LF}	Turn-off Sink Current	-	800	-	mA
Low-side Drive Source Current I_{LR}	Turn-on Source Current	-	400	-	mA
High-side Output Voltage (On-state) V_{GHIH}	Bootstrap Capacitor Fully Charged	$V_{BU/V/W1} - 0.2$	-	-	V
High-side Output Voltage (Off-state) V_{GHL}	$-10\mu A < I_{GH} < 10\mu A$	-	-	$V_{SU/V/W1} + 0.3$	V
Low-side Output Voltage (On-state) V_{GLH}	Bootstrap Capacitor Fully Charged	$V_{BB} - 0.2$	-	-	V
Low-side Output Voltage (Off-state) V_{GLL}	$-10\mu A < I_{GL} < 10\mu A$	-	-	$V_{LSS1} + 0.3$	V
Turn-off Propagation Delay $t_{P(off)}$	From Input to Unloaded Pre-driver1 Output	-	80	-	ns
Turn-on Propagation Delay $t_{P(on)}$		-	90	-	ns
High-side MOSFET Drain Voltage V_{VDH1}	With the VDS Monitor Active	9	VCC	60	V
VDH1 Input Current I_{VDH1}	VDSTH = Default, $V_{CC} = 12V, 0V < V_{VDH1} < V_{CC}$	-	-	500	μA
VDH1 Sleep-mode Current I_{VDHQ}	$V_{CC} = 12V$, Sleep Mode	-	-	5	μA
Deadtime		-	95	-	ns

5.5.2.2 6N Pre-driver1 Protection Characteristics of FU7565Q1

Table 5-19 6N Pre-driver1 Protection Characteristics of FU7565Q1

($T_A = 25^\circ C$ and $V_{CC} = 15V$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB UVLO Threshold Voltage V_{BBUVF}		6.7	7.2	7.7	V
VBB UVLO Release Voltage V_{BBUVR}		7.5	8	8.5	V
VBB UVLO Hysteresis Voltage $V_{BBUVhys}$		-	0.8	-	V
VCC UVLO Threshold Voltage V_{CCUVF}	VTLW_R[VCCOVS] = 00	-	20	-	V
	VTLW_R[VCCOVS] = 01	-	8	-	V
VCC UVLO Release Voltage V_{CCUVR}	VTLW_R[VCCOVS] = 00	-	22	-	V
	VTLW_R[VCCOVS] = 01	-	8.8	-	V
VCC UVLO Hysteresis Voltage $V_{CCUVhys}$	VTLW_R[VCCOVS] = 00	-	2	-	V
	VTLW_R[VCCOVS] = 01	-	0.8	-	V
VCC OVP Threshold Voltage V_{CCOVPR}	VTLW_R[VCCOVS] = 00	-	60	-	V
	VTLW_R[VCCOVS] = 01	-	40	-	V
VCC OVP Release Voltage V_{CCOVPR}	VTLW_R[VCCOVS] = 00	-	57	-	V
	VTLW_R[VCCOVS] = 01	-	38	-	V
VCC OVP Hysteresis Voltage $V_{CCOVPhys}$	VTLW_R[VCCOVS] = 00	-	3	-	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	VT _{TLW_R} [VCCOV _S] = 01	–	2	–	V
VCC Power-on Reset Threshold Voltage V _{CCPORF}		–	3.9	–	V
VCC Power-On Reset Release Voltage V _{CCPORR}		–	4.0	–	V
VCC Power-On Reset Hysteresis Voltage V _{CCPORhys}		–	0.1	–	V
VDD5 UVLO Threshold Voltage V _{DD5UVF}		–	3.8	–	V
VDD5 UVLO Release Voltage V _{DD5UVR}		–	4.0	–	V
VDD5 UVLO Hysteresis Voltage V _{DD5UVhys}		–	0.2	–	V
Bootstrap UVLO Threshold Voltage V _{BUVF}	V _{BOOT} = V _{Bx1} – V _{Sx1}	55	60	65	%V _{BB}
Bootstrap UVLO Release Voltage V _{BUVR}	V _{BOOT} = V _{Bx1} – V _{Sx1}	65	70	75	%V _{BB}
Bootstrap UVLO Hysteresis Voltage V _{BUVhys}		–	10	–	%V _{BB}
Bootstrap OVP Threshold Voltage V _{BOVR}	V _{BOOT} = V _{Bx1} – V _{Sx1}	150	160	170	%V _{BB}
Bootstrap OVP Release Voltage V _{BOVF}	V _{BOOT} = V _{Bx1} – V _{Sx1}	140	150	160	%V _{BB}
Bootstrap OVP Hysteresis Voltage V _{BOVhys}		–	10	–	%V _{BB}
High-side VDS Over-voltage Threshold V _{DSTHx}	Power-on Default	–	1.6	–	V
Low-side VDS Over-voltage Threshold V _{DSTLx}	Power-on Default	–	1.6	–	V
VDS OVP Timer Duration t _{V_{DQx}}	Power-on Default	–	3.2	–	μs
Thermal Shutdown Threshold T _{SD}		–	165	–	°C
Thermal Shutdown Hysteresis T _{SDhys}		–	20	–	°C

5.5.3 6N Pre-driverx Electrical Characteristics of FU7574Q1

5.5.3.1 6N Pre-driverx Electrical Parameters of FU7574Q1

Table 5-20 6N Pre-driverx Electrical Parameters of FU7574Q1

(T_A = 25°C and VCC_x = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Forward Voltage V _{F,BOOT}	I _F = 10mA	0.5	0.8	1.1	V
	I _F = 100mA	1.5	2.2	2.8	V
High-side Pull-down Resistor R _{GHPD}	V _{CC} = 0V, V _{HU/VWx} – V _{SU/VWx} < 0.1V	–	950	–	kΩ
Low-side Pull-down Resistor R _{GLPD}	V _{CC} = 0V, V _{LU/VWx} – V _{LSSx} < 0.1V	–	950	–	kΩ
High-side Drive Sink Current I _{HF}	Turn-off Sink Current	–	800	–	mA
High-side Drive Source Current I _{HR}	Turn-on Source Current	–	400	–	mA
Low-side Drive Sink Current I _{LF}	Turn-off Sink Current	–	800	–	mA
Low-side Drive Source Current I _{LR}	Turn-on Source Current	–	400	–	mA
High-side Output Voltage (On-state) V _{GHH}	Bootstrap Capacitor Fully Charged	V _{BU/VWx} – 0.2	–	–	V
High-side Output Voltage (Off-state) V _{GHL}	–10μA < I _{GH} < 10μA	–	–	V _{SU/VWx} + 0.3	V
Low-side Output Voltage (On-state) V _{GLH}	Bootstrap Capacitor Fully Charged	V _{BB,x} – 0.2	–	–	V
Low-side Output Voltage (Off-state) V _{GLL}	–10μA < I _{GL} < 10μA	–	–	V _{LSSx} + 0.3	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Turn-off Propagation Delay $t_{P(off)}$	From Input to Unloaded Pre-driverx Output	–	30	–	ns
Turn-on Propagation Delay $t_{P(on)}$		–	40	–	ns
High-side MOSFET Drain Voltage V_{VDHx}	With the VDS Monitor Active	5.5	V_{CC_x}	40	V
VDHx Input Current I_{VDHx}	$V_{DSTH} = \text{Default}$, $V_{CC\_x} = 12V$, $0V < V_{VDHx} < V_{CC\_x}$	–	–	500	μA
VDHx Sleep-mode Current I_{VDHQ}	$V_{CC\_x} = 12V$, Sleep Mode	–	–	5	μA
Deadtime		–	95	–	ns

5.5.3.2 6N Pre-driverx Protection Characteristics of FU7574Q1

Table 5-21 6N Pre-driverx Protection Characteristics of FU7574Q1

($T_A = 25^\circ C$ and $V_{CC\_x} = 15V$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB UVLO Threshold Voltage V_{BBUVF}		4.6	4.7	5.2	V
VBB UVLO Release Voltage V_{BBUVR}		5.0	5.3	5.6	V
VBB UVLO Hysteresis Voltage $V_{BBUVhys}$		–	0.6	–	V
VCC UVLO Threshold Voltage V_{CCUVF}		–	4.8	–	V
VCC UVLO Release Voltage V_{CCUVR}		–	5.3	–	V
VCC UVLO Hysteresis Voltage $V_{CCUVhys}$		–	0.5	–	V
VCC OVP Warning Threshold Voltage V_{CCOVWR}		–	36.1	–	V
VCC OVP Warning Release Voltage V_{CCOVWF}		–	33.8	–	V
VCC OVP Warning Hysteresis Voltage $V_{CCOVWhys}$		–	2.3	–	V
VCC OVP Threshold Voltage V_{CCOVPR}		–	41.5	–	V
VCC OVP Release Voltage V_{CCOVPR}		–	40.0	–	V
VCC OVP Hysteresis Voltage $V_{CCOVPhys}$		–	1.5	–	V
VCC Power-on Reset Threshold Voltage V_{CCPORF}		–	2.3	–	V
VCC Power-On Reset Release Voltage V_{CCPORR}		–	2.4	–	V
VCC Power-On Reset Hysteresis Voltage $V_{CCPORhys}$		–	0.1	–	V
VDD5 UVLO Threshold Voltage V_{DD5UVF}		–	3.8	–	V
VDD5 UVLO Release Voltage V_{DD5UVR}		–	4.0	–	V
VDD5 UVLO Hysteresis Voltage $V_{DD5UVhys}$		–	0.2	–	V
Bootstrap UVLO Threshold Voltage V_{BUVF}	$V_{BOOT} = V_{BUV/Wx} - V_{SU/V/Wx}$	55	60	65	$\%V_{BB}$
Bootstrap UVLO Release Voltage V_{BUVR}	$V_{BOOT} = V_{BUV/Wx} - V_{SU/V/Wx}$	65	70	75	$\%V_{BB}$
Bootstrap UVLO Hysteresis Voltage V_{BUVhys}		–	10	–	$\%V_{BB}$
Bootstrap OVP Threshold Voltage V_{BOVR}	$V_{BOOT} = V_{BUV/Wx} - V_{SU/V/Wx}$	175	185	195	$\%V_{BB}$
Bootstrap OVP Release Voltage V_{BOVF}	$V_{BOOT} = V_{BUV/Wx} - V_{SU/V/Wx}$	165	175	185	$\%V_{BB}$
Bootstrap OVP Hysteresis Voltage V_{BOVhys}		–	10	–	$\%V_{BB}$
High-side VDS OVP Threshold $V_{DSTHU/VW}$	Power-on Default	–	1.6	–	V
Low-side VDS OVP Threshold $V_{DSTLU/VW}$	Power-on Default	–	1.6	–	V
VDS OVP Timer Duration $t_{VDQU/VW}$	Power-on Default	–	3.2	–	μs
Thermal Shutdown Threshold T_{SD}		–	165	–	$^\circ C$
Thermal Shutdown Hysteresis T_{SDhys}		–	20	–	$^\circ C$

5.6 ADC Electrical Characteristics

5.6.1 FU7512Q1

Table 5-22 ADC Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	–	2	–	LSB
DNL (Differential Nonlinearity)	12-bit	–	1.5	–	LSB
OFFSET (Offset Error)	12-bit	–	6	–	LSB
SNR (Signal-to-noise Ratio)	f _{IN} = 350kHz	–	70.8	–	dB
ENOB (Effective Number of Bits)	f _{IN} = 350kHz	–	10.5	–	bit
SFDR (Spurious-free Dynamic Range)	f _{IN} = 350kHz	–	68.2	–	dB
THD (Total Harmonic Distortion)	f _{IN} = 350kHz	–	67	–	dB
RIN Input Resistance		–	800	–	Ω
CIN Input Capacitance		–	30	–	pF
Conversion Time		–	13	–	ADCLK ^[1]
Sampling Time		3	–	63	ADCLK2 ^[2]

5.6.2 FU7564Q1

Table 5-23 ADC Electrical Characteristics of FU7564Q1

(T_A = 25°C and VCC = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	–	2	–	LSB
DNL (Differential Nonlinearity)	12-bit	–	1.5	–	LSB
OFFSET (Offset Error)	12-bit	–	6	–	LSB
SNR (Signal-to-noise Ratio)	f _{IN} = 350kHz	–	70.8	–	dB
ENOB (Effective Number of Bits)	f _{IN} = 350kHz	–	10.5	–	bit
SFDR (Spurious-free Dynamic Range)	f _{IN} = 350kHz	–	68.2	–	dB
THD (Total Harmonic Distortion)	f _{IN} = 350kHz	–	67	–	dB
RIN Input Resistance		–	800	–	Ω
CIN Input Capacitance		–	30	–	pF
Conversion Time		–	13	–	ADCLK ^[1]
Sampling Time		3	–	63	ADCLK2 ^[2]

5.6.3 FU7565Q1

Table 5-24 ADC Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	–	2	–	LSB

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DNL (Differential Nonlinearity)	12-bit	–	1.5	–	LSB
OFFSET (Offset Error)	12-bit	–	6	–	LSB
SNR (Signal-to-noise Ratio)	$f_{IN} = 350\text{kHz}$	–	70.8	–	dB
ENOB (Effective Number of Bits)	$f_{IN} = 350\text{kHz}$	–	10.5	–	bit
SFDR (Spurious-free Dynamic Range)	$f_{IN} = 350\text{kHz}$	–	68.2	–	dB
THD (Total Harmonic Distortion)	$f_{IN} = 350\text{kHz}$	–	67	–	dB
RIN Input Resistance		–	800	–	Ω
CIN Input Capacitance		–	30	–	pF
Conversion Time		–	13	–	ADCLK ^[1]
Sampling Time		3	–	63	ADCLK2 ^[2]

5.6.4 FU7574Q1

Table 5-25 ADC Electrical Characteristics of FU7574Q1

($T_A = 25^\circ\text{C}$ and $V_{CC\_X} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL (Integral Nonlinearity)	12-bit	–	2	–	LSB
DNL (Differential Nonlinearity)	12-bit	–	1.5	–	LSB
OFFSET (Offset Error)	12-bit	–	6	–	LSB
SNR (Signal-to-noise Ratio)	$f_{IN} = 350\text{kHz}$	–	70.8	–	dB
ENOB (Effective Number of Bits)	$f_{IN} = 350\text{kHz}$	–	10.5	–	bit
SFDR (Spurious-free Dynamic Range)	$f_{IN} = 350\text{kHz}$	–	68.2	–	dB
THD (Total Harmonic Distortion)	$f_{IN} = 350\text{kHz}$	–	67	–	dB
RIN Input Resistance		–	800	–	Ω
CIN Input Capacitance		–	30	–	pF
Conversion Time		–	13	–	ADCLK ^[1]
Sampling Time		3	–	63	ADCLK2 ^[2]



Note:

[1] ADCLK = 24MHz

[2] ADCLK2 = 12MHz

5.7 VREF and VHALF Electrical Characteristics

5.7.1 FU7512Q1

Table 5-26 VREF and VHALF Electrical Characteristics of FU7512Q1

($T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$ and $V_{DD5} = 5\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	5.0	5.2	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VHALF	VREF_VHALF_CR[VRVSEL] = 10	2.8	3.0	3.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4.0	4.2	V
	VREF_VHALF_CR[VHALFSEL] = 00	$V_{REF}/8 - 0.1$	$V_{REF}/8$	$V_{REF}/8 + 0.1$	V
	VREF_VHALF_CR[VHALFSEL] = 01	$V_{REF}/4 - 0.12$	$V_{REF}/4$	$V_{REF}/4 + 0.12$	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 10	$25 \cdot V_{REF}/64 - 0.2$	$25 \cdot V_{REF}/64$	$25 \cdot V_{REF}/64 + 0.2$	V
	VREF_VHALF_CR[VHALFSEL] = 11	$V_{REF}/2 - 0.2$	$V_{REF}/2$	$V_{REF}/2 + 0.2$	V

5.7.2 FU7564Q1

Table 5-27 VREF and VHALF Electrical Characteristics of FU7564Q1

($T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$ and $V_{CC} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	5.0	5.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3.0	3.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4.0	4.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 00	$V_{REF}/8 - 0.1$	$V_{REF}/8$	$V_{REF}/8 + 0.1$	V
	VREF_VHALF_CR[VHALFSEL] = 01	$V_{REF}/4 - 0.12$	$V_{REF}/4$	$V_{REF}/4 + 0.12$	V
	VREF_VHALF_CR[VHALFSEL] = 10	$25 \cdot V_{REF}/64 - 0.2$	$25 \cdot V_{REF}/64$	$25 \cdot V_{REF}/64 + 0.2$	V
	VREF_VHALF_CR[VHALFSEL] = 11	$V_{REF}/2 - 0.2$	$V_{REF}/2$	$V_{REF}/2 + 0.2$	V

5.7.3 FU7565Q1

Table 5-28 VREF and VHALF Electrical Characteristics of FU7565Q1

($T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$ and $V_{CC} = 9\text{V} \sim 60\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V
	VREF_VHALF_CR[VRVSEL] = 01	4.8	5.0	5.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3.0	3.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4.0	4.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 00	$V_{REF}/8 - 0.1$	$V_{REF}/8$	$V_{REF}/8 + 0.1$	V
	VREF_VHALF_CR[VHALFSEL] = 01	$V_{REF}/4 - 0.12$	$V_{REF}/4$	$V_{REF}/4 + 0.12$	V
	VREF_VHALF_CR[VHALFSEL] = 10	$25 \cdot V_{REF}/64 - 0.2$	$25 \cdot V_{REF}/64$	$25 \cdot V_{REF}/64 + 0.2$	V
	VREF_VHALF_CR[VHALFSEL] = 11	$V_{REF}/2 - 0.2$	$V_{REF}/2$	$V_{REF}/2 + 0.2$	V

5.7.4 FU7574Q1

Table 5-29 VREF and VHALF Electrical Characteristics of FU7574Q1

($T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$ and $V_{CC\_x} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	VREF_VHALF_CR[VRVSEL] = 00	4.3	4.5	4.7	V

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	VREF_VHALF_CR[VRVSEL] = 01	4.8	5.0	5.2	V
	VREF_VHALF_CR[VRVSEL] = 10	2.8	3.0	3.2	V
	VREF_VHALF_CR[VRVSEL] = 11	3.8	4.0	4.2	V
VHALF	VREF_VHALF_CR[VHALFSEL] = 00	$VREF/8 - 0.1$	$VREF/8$	$VREF/8 + 0.1$	V
	VREF_VHALF_CR[VHALFSEL] = 01	$VREF/4 - 0.12$	$VREF/4$	$VREF/4 + 0.12$	V
	VREF_VHALF_CR[VHALFSEL] = 10	$25 \cdot VREF/64 - 0.2$	$25 \cdot VREF/64$	$25 \cdot VREF/64 + 0.2$	V
	VREF_VHALF_CR[VHALFSEL] = 11	$VREF/2 - 0.2$	$VREF/2$	$VREF/2 + 0.2$	V

5.8 Operational Amplifier Electrical Characteristics

5.8.1 FU7512Q1

Table 5-30 Operational Amplifier Electrical Characteristics of FU7512Q1

($T_A = 25^\circ\text{C}$ and $VDD5 = 5\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VICMR Common-mode Input Voltage Range		0	-	$VDD5 - 1.5$	V
VOS Operational Amplifier Offset Voltage	$T_A = 25^\circ\text{C}$	-	5	10	mV
A_{OL} Open-loop Gain	$RL = 100\text{k}\Omega$	-	80	-	dB
Unity-gain Bandwidth (UGBW)	$CL = 40\text{pF}$	6	10	-	MHz
Slew Rate (SR)	$CL = 40\text{pF}$	10	15	-	$\text{V}/\mu\text{s}$
Operational Amplifier Gain ^[1]	AMP_CR1[AMPxGAIN] = 001	3.76	4	4.24	-
	AMP_CR1[AMPxGAIN] = 010	7.5	8	8.5	-
	AMP_CR1[AMPxGAIN] = 011	15	16	17	-
	AMP_CR1[AMPxGAIN] = 100	18.5	20	21.5	-
	AMP_CR1[AMPxGAIN] = 110, for AMP5/6 only	37	40	43	-

5.8.2 FU7564Q1

Table 5-31 Operational Amplifier Electrical Characteristics of FU7564Q1

($T_A = 25^\circ\text{C}$ and $VCC = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VICMR Common-mode Input Voltage Range		0	-	$VDD5 - 1.5$	V
VOS Operational Amplifier Offset Voltage	$T_A = 25^\circ\text{C}$	-	5	10	mV
A_{OL} Open-loop Gain	$RL = 100\text{k}\Omega$	-	80	-	dB
Unity-gain Bandwidth (UGBW)	$CL = 40\text{pF}$	6	10	-	MHz
Slew Rate (SR)	$CL = 40\text{pF}$	10	15	-	$\text{V}/\mu\text{s}$
Operational Amplifier Gain ^[1]	AMP_CR1[AMPxGAIN] = 001	3.76	4	4.24	-
	AMP_CR1[AMPxGAIN] = 010	7.5	8	8.5	-

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	AMP_CR1[AMPxGAIN] = 011	15	16	17	-
	AMP_CR1[AMPxGAIN] = 100	18.5	20	21.5	-

5.8.3 FU7565Q1

Table 5-32 Operational Amplifier Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VICMR Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
VOS Operational Amplifier Offset Voltage	T _A = 25°C	-	5	10	mV
A _{oL} Open-loop Gain	RL = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (UGBW)	CL = 40pF	6	10	-	MHz
Slew Rate (SR)	CL = 40pF	10	15	-	V/μs
Operational Amplifier Gain ^[1]	AMP_CR1[AMPxGAIN] = 001	3.76	4	4.24	-
	AMP_CR1[AMPxGAIN] = 010	7.5	8	8.5	-
	AMP_CR1[AMPxGAIN] = 011	15	16	17	-
	AMP_CR1[AMPxGAIN] = 100	18.5	20	21.5	-
	AMP_CR1[AMPxGAIN] = 110, for AMP5 only	37	40	43	-

5.8.4 FU7574Q1

Table 5-33 Operational Amplifier Electrical Characteristics of FU7574Q1

(T_A = 25°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VICMR Common-mode Input Voltage Range		0	-	VDD5 - 1.5	V
VOS Operational Amplifier Offset Voltage	T _A = 25°C	-	5	10	mV
A _{oL} Open-loop Gain	RL = 100kΩ	-	80	-	dB
Unity-gain Bandwidth (UGBW)	CL = 40pF	6	10	-	MHz
Slew Rate (SR)	CL = 40pF	10	15	-	V/μs
Operational Amplifier Gain ^[1]	AMP_CR1[AMPxGAIN] = 001	3.76	4	4.24	-
	AMP_CR1[AMPxGAIN] = 010	7.5	8	8.5	-
	AMP_CR1[AMPxGAIN] = 011	15	16	17	-
	AMP_CR1[AMPxGAIN] = 100	18.5	20	21.5	-
	AMP_CR1[AMPxGAIN] = 110, for AMP5/6 only	37	40	43	-



Note:

[1] The operational amplifier gain is measured when both positive and negative inputs of the operational amplifier are connected in series with 1kΩ resistors. The operational amplifier gain varies with external resistors.

5.9 BEMF Electrical Characteristics

5.9.1 FU7512Q1

Table 5-34 BEMF Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor	T _A = -40°C ~ 125°C	5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.2 FU7564Q1

Table 5-35 BEMF Electrical Characteristics of FU7564Q1

(T_A = 25°C and VCC = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor	T _A = -40°C ~ 125°C	5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.3 FU7565Q1

Table 5-36 BEMF Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor	T _A = -40°C ~ 125°C	5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.9.4 FU7574Q1

Table 5-37 BEMF Electrical Characteristics of FU7574Q1

(T_A = 25°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BEMF Built-in Resistor	T _A = -40°C ~ 125°C	5.4	6.8	8.2	kΩ
Relative Accuracy between BEMF Built-in Resistors		-	1	-	%

5.10 Clock Electrical Characteristics

5.10.1 FU7512Q1

Table 5-38 Clock Electrical Characteristics of FU7512Q1

(T_A = -40°C ~ 125°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 1	23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 0	47	48	49	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.2 FU7564Q1

Table 5-39 Clock Electrical Characteristics of FU7564Q1

($T_A = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ and $V_{CC} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 1	23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 0	47	48	49	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.3 FU7565Q1

Table 5-40 Clock Electrical Characteristics of FU7565Q1

($T_A = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ and $V_{CC} = 9\text{V} \sim 60\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 1	23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 0	47	48	49	MHz
Low-speed Clock Rate		29	32.8	37	kHz

5.10.4 FU7574Q1

Table 5-41 Clock Electrical Characteristics of FU7574Q1

($T_A = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ and $V_{CC\_X} = 5.5\text{V} \sim 18\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
System Clock Rate		23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 1	23.5	24	24.5	MHz
System Clock Rate	PLL Enabled and CCFG3[PLLFSEL] = 0	47	48	49	MHz
Low-speed Clock Rate		29	32.8	37	kHz



Note:

Note: SYSCLK refers to system clock rate, and T to system clock cycle. Unless otherwise specified, the system clock rate of chip is 24/48MHz and $T = 1/\text{SYSCLK}$.

5.11 Reset Electrical Characteristics

5.11.1 FU7512Q1

Table 5-42 Reset Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time for RSTN Released to Low		50	–	–	μs
VDD5 Low-voltage Reset Threshold	Reset Voltage LVR = 3.0	2.8	3.0	3.2	V

5.11.2 FU7564Q1

Table 5-43 Reset Electrical Characteristics of FU7564Q1

(T_A = 25°C and VCC = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time for RSTN Released to Low		50	–	–	μs
VDD5 Low-voltage Reset Threshold	Reset Voltage LVR = 3.0	2.8	3.0	3.2	V

5.11.3 FU7565Q1

Table 5-44 Reset Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time for RSTN Released to Low		50	–	–	μs
VDD5 Low-voltage Reset Threshold	Reset Voltage LVR = 3.0	2.8	3.0	3.2	V

5.11.4 FU7574Q1

Table 5-45 Reset Electrical Characteristics of FU7574Q1

(T_A = 25°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum Time for RSTN Released to Low		50	–	–	μs
VDD5 _x Low-voltage Reset Threshold	Reset Voltage LVR = 3.0	2.8	3.0	3.2	V

5.12 LDO Electrical Characteristics

5.12.1 FU7512Q1

Table 5-46 LDO Electrical Characteristics of FU7512Q1

(T_A = 25°C and VDD5 = 5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD2P5 Voltage		2.3	2.5	2.7	V

5.12.2 FU7564Q1

Table 5-47 LDO Electrical Characteristics of FU7564Q1

(T_A = 25°C and VCC = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB Voltage	VCC = 12V, I _{VBB} = 20mA	10	11	12	V
VDD5 Voltage	VCC = 12V, I _{VDD5} = 20mA	4.8	5	5.2	V
VDD2P5 Voltage		2.3	2.5	2.7	V

5.12.3 FU7565Q1

Table 5-48 LDO Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD5 Voltage	VCC = 24V, I _{VDD5} = 20mA	4.8	5	5.2	V
VDD2P5 Voltage		2.3	2.5	2.7	V

5.12.4 FU7574Q1

Table 5-49 LDO Electrical Characteristics of FU7574Q1

(T_A = 25°C and VCC_x = 5.5V ~ 18V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB _x Voltage	VCC _x = 12V, I _{VBB_x} = 20mA	10	11	12	V
VDD5 _x Voltage	VCC _x = 12V, I _{VBB_x} = 20mA	4.8	5	5.2	V
VDD2P5 Voltage		2.3	2.5	2.7	V

5.13 Buck DC-DC Converter Electrical Characteristics (FU7565Q1)

5.13.1 FU7565Q1

Table 5-50 Buck DC-DC Converter Electrical Characteristics of FU7565Q1

(T_A = 25°C and VCC = 9V ~ 60V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VBB Voltage	VCC = 24V, I _{VBB} = 20mA	11	12	13	V
VBB Load Current	VCC = 24V, F _S = 125kHz, L = 100μH	–	–	120	mA
Inductor Peak Current		–	300	–	mA
Switch Frequency F _S	VTLV_R[OSC2_FSE] = 00	–	125	–	kHz

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	VTLV_R[OSC2_FSE] = 01	-	250	-	
	VTLV_R[OSC2_FSE] = 10	-	500	-	
	VTLV_R[OSC2_FSE] = 11	-	1000	-	

5.14 Package Thermal Resistance

5.14.1 FU7512Q1 QFN56

Table 5-51 FU7512Q1 QFN56 Package Thermal Resistance

Parameter	Test Conditions	Min.	Unit
Junction-to-ambient Thermal Resistance $\theta_{JA}^{[1]}$	JEDEC standard, 2S2P PCB	33	°C/W
	JEDEC standard, 1S0P PCB	55	°C/W
Junction-to-case Thermal Resistance $\theta_{JC}^{[1]}$	JEDEC standard, 1S0P PCB	9.2	°C/W

5.14.2 FU7564Q1 QFN56

Table 5-52 FU7564Q1 QFN56 Package Thermal Resistance

Parameter	Test Conditions	Min.	Unit
Junction-to-ambient Thermal Resistance $\theta_{JA}^{[1]}$	JEDEC standard, 2S2P PCB	33	°C/W
	JEDEC standard, 1S0P PCB	55	°C/W
Junction-to-case Thermal Resistance $\theta_{JC}^{[1]}$	JEDEC standard, 1S0P PCB	9.2	°C/W

5.14.3 FU7565Q1 QFN48

Table 5-53 FU7565Q1 QFN48 Package Thermal Resistance

Parameter	Test Conditions	Min.	Unit
Junction-to-ambient Thermal Resistance $\theta_{JA}^{[1]}$	JEDEC standard, 2S2P PCB	27	°C/W
	JEDEC standard, 1S0P PCB	12	°C/W
Junction-to-case Thermal Resistance $\theta_{JC}^{[1]}$	JEDEC standard, 1S0P PCB	15	°C/W

5.14.4 FU7574Q1 QFN88

Table 5-54 FU7574Q1 QFN88 Package Thermal Resistance

Parameter	Test Conditions	Min.	Unit
Junction-to-ambient Thermal Resistance $\theta_{JA}^{[1]}$	JEDEC standard, 2S2P PCB	25	°C/W
	JEDEC standard, 1S0P PCB	48	°C/W
Junction-to-case Thermal Resistance $\theta_{JC}^{[1]}$	JEDEC standard, 1S0P PCB	6	°C/W



Note:

[1] The actual measurements may vary depending on the conditions.

6 Reset Control

6.1 Reset Source (RST_SR)

The chip includes a reset circuitry with 7 reset sources:

- > Power-on Reset (RSTPOW)
- > External Pin Reset (RSTEXT)
- > Low-voltage Detection Reset (RSTLVD)
- > Watchdog Timer Reset (RSTWDT)
- > Flash Error Detection Reset (RSTFED)
- > Debug Reset (RSTDBG)
- > Soft Reset (SOFTRST)

The reset flag can be queried and is recorded in RST_SR register. The most recent reset sets the relevant status flag to “1” while clears all other flag bits to “0”. To clear the status flags, you can set RST_CR[RSTCLR] = 1 so that RST_SR[7:3] and RST_SR[0] are cleared. After reset, MCU starts the program from address 0x0000.

6.2 Reset Enable

See the relevant control register for reset enable configuration.

6.3 External Pin Reset and Power-on Reset

The chip resets when RSTN pin remains low for more than 50μs.

The chip resets when the power supply voltage exceeds the reset threshold voltage.

6.4 Low-voltage Detection Reset

The chip’s internal circuitry monitors VDD5 voltage. When the VDD5 voltage drops below the reset voltage threshold, the internal monitor circuitry sends a LVD reset signal to reset the chip.

Configuring corresponding register enables the low-voltage detection circuit and sets the low-voltage threshold.

6.5 Watchdog Timer Reset

After the watchdog timer (WDT) is enabled, a system reset occurs when WDT overflows or “times out”. If system error occurs or system reset fails, the timer generates an output pulse to reset the chip.

6.6 Flash Error Detection Reset

The Flash memory can be programmed for read/write/erase operations. A Flash error detection reset (RSTFED) occurs if a Flash erase is attempted targeting the last sector (0xFF00 ~ 0xFFFF) or a Flash write is attempted targeting the last byte (0xFFFF). RSTFED is always enabled and cannot be disabled.

6.7 Debug Reset

Click Reset button of IDE to send a debug reset signal when the chip enters the debug state.

6.8 Soft Reset

The chip resets immediately when RST_CR[SFRST] is set to “1”. After reset, the flag bit RST_SR[SOFT_RST] is set to “1”.

6.9 Reset Registers

6.9.1 RST_SR (CSR: 0x4D0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								RSTPOW	RSTEXT	RSTLVD	RSV	RSTWDT	RSTFED	RSTDBG	SOFT_RST
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	-	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit	Name	Description
[31:8]	RSV	Reserved

[7]	RSTPOW	Power-on Reset Flag 0: The last reset is not a power-on reset. 1: The last reset is a power-on reset.
[6]	RSTEXT	External Pin Reset Flag 0: The last reset is not an external pin reset. 1: The last reset is an external pin reset.
[5]	RSTLVD	Low-voltage Detection (LVD) Reset Flag 0: The last reset is not a LVD reset. 1: The last reset is a LVD reset.
[4]	RSV	Reserved
[3]	RSTWDT	Watchdog Timer Reset Flag 0: The last reset is not a watchdog timer reset. 1: The last reset is a watchdog timer reset.
[2]	RSTFED	Flash Error Detector Reset Flag 0: The last reset is not a Flash error detector reset. 1: The last reset is a Flash error detector reset.
[1]	RSTDBG	Debug Reset Flag 0: The last reset is not a debug reset. 1: The last reset is a debug reset.
[0]	SOFTIRST	Soft Reset Flag 0: The last reset is not a soft reset. 1: The last reset is a soft reset.

6.9.2 RST_CR (CSR: 0x4D1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV																								WKRE		WKPOLAR		RSV		SFRST		RSTCLR	
																								rw		rw		-		w1		w1	
																								0		0		-		-		-	
																								-		-		-		-		-	
																								-		-		-		-		-	

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	WKRE	MON Wake-up Enable 0: Disable 1: Enable

[4]	WKPOLAR	MON Input (PA9) Wake-up Level 0: Low Level 1: High Level
[3:2]	RSV	Reserved
[1]	SFRST	Soft Reset 0: No effect. 1: A soft reset is triggered.
[0]	RSTCLR	Reset Flag Clear 0: No effect 1: RST_SR[7:3]&RST_SR[0] are cleared to "0".

7 Interrupt

7.1 Interrupt Introduction

Each interrupt source, except the Reset Interrupt, can be assigned a priority level. A low-priority interrupt can be interrupted by a high-priority interrupt. The low-priority interrupt will not be serviced until the ISR for the high-priority interrupt is completed. An interrupt will not be preempted by another of the same priority level. Each interrupt source can be individually configured to one of eight priority levels in the Interrupt Priority (IP) register. Priority level assigned ascends from 0 to 7 and is defaulted to 0. If two interrupt requests are generated at the same time, the interrupt with the higher priority is serviced first. If two interrupt sources have the same priority level, a fixed priority order is used to arbitrate. See Table 7-1 for the interrupt sources and default priority orders, where the lower the mark the higher the priority level.

7.2 Interrupt Enable

MIE[IRQ_EN] is the global interrupt enable bit. The MCU does not respond to any interrupt request when MIE[IRQ_EN] = 0.

Each interrupt source can be individually enabled or disabled by configuring the corresponding interrupt enable bit in CSR. When the enable bit of the global interrupt or an interrupt is cleared, the interrupt flag that is set to “1” is held in a pending state. Once the enable bit is set to “1”, the MCU immediately enters the interrupt subroutine. Therefore, make sure to clear corresponding interrupt flag bit before enabling the interrupt.

7.3 External Interrupt

The external interrupt has three interrupt sources: EXTI0, EXTI1 and EXTI2. They both can be configured as interrupt on rising edge, interrupt on falling edge or interrupt on edge changes (rise or fall).

GPIOs for triggering external interrupts differ across chip models. See chapter Pin Definitions for details. The digital input signals PD0, PD3, PA0 ~ PA7, and PA9 ~ PA12 can be used to trigger an EXTI0. The interrupt source is selected through the associated EX0IE bit, and is identified by EX0IF register in ISR.

These trigger sources share one interrupt entry point and one interrupt enable bit PIE[EX0]. To enable EXTI0, first set PIE[EX0] to “1” and then configure the corresponding enable bit. The interrupt edge is configured by EXTI_TCON[IT0] bit, and the priority level is set by IP2 register.

The digital input signals from PB2, PA0 ~ PA7, and PA9 ~ PA14 can be used to trigger an EXTI1. The interrupt source is selected through the associated EX1IE bit, and is identified by EX1IF register in ISR. These trigger sources share one interrupt entry point and one interrupt enable bit PIE[EX1]. To enable EXTI1, first set PIE[EX1] to “1” and then configure the corresponding enable bit. The interrupt edge is configured by EXTI_TCON[IT1] bit, and the priority level is set by IP1 register.

The digital input signals from PC0 ~ PC7 and PB0 ~ PB7 can be used to trigger an EXTI2. The interrupt source is selected through the associated EX2IE bit, and is identified by EX2IF register in ISR. These trigger sources share one interrupt entry point and one interrupt enable bit PIE[EX2]. To enable EXTI2, first set PIE[EX2] to “1” and then configure the corresponding enable bit. The interrupt edge is configured by EXTI_TCON[IT2] bit, and the priority level is set by IP3 register.

7.4 Interrupt Summary

Table 7-1 Interrupt Summary

Interrupt Source	Priority Order	Interrupt Vector	Interrupt Flag	Cleared by Software?	Enable Bit	Priority Control
Reset	Highest	None	None	N	Always enabled	Highest
LVW Interrupt TSD Interrupt ECC Interrupt	0	0x00000000	LVSR[0] EXTI_TCON[6] ECC_SR[6] ECC_SR[3:0]	Y	CCFG2[6] PIE[3] ECC_CR[6] ECC_CR[4:0]	IP0[2:0]
EXTI0	1	0x00000004	EXTI0IF[15] EXTI0IF[13:9] EXTI0IF[7:0]	Y	PIE[0]	IP1[2:0]
EXTI1	2	0x00000008	EXTI1IF[15:9] EXTI1IF[7:0]	Y	PIE[1]	IP2[2:0]
EXTI2	3	0x0000000C	EXTI2IF[15:0]	Y	PIE[2]	IP3[2:0]
CMP3/4/5 Interrupt CMP9/10/11 Interrupt	4	0x00000010	CMP_IFR[5:3] CMP_IFR[11:9]	Y	CMP_CR0[11:6] CMP_CR4[11:6]	IP4[2:0]
CMP0/1/2 Interrupt CMP6/7/8 Interrupt	5	0x00000014	CMP_IFR[2:0] CMP_IFR[8:6]	Y	CMP_CR0[5:0] CMP_CR4[5:0]	IP5[2:0]
DRV1 Protection	6	0x00000018	DRV1_PSR[4:0]	Y	DRV1_PER[4:0]	IP6[2:0]

Interrupt Source	Priority Order	Interrupt Vector	Interrupt Flag	Cleared by Software?	Enable Bit	Priority Control
Interrupt					DRV1_PTR[3:0]	
DRV2 Protection Interrupt	7	0x0000001C	DRV2_PSR[4:0]	Y	DRV2_PER[4:0] DRV2_PTR[3:0]	IP7[2:0]
DRV1 Interrupt	8	0x00000020	DRV1_IFR[4:3] DRV1_IFR[0]	Y	DRV1_IER[5:3]	IP8[2:0]
DRV2 Interrupt	9	0x00000024	DRV2_IFR[4:3] DRV2_IFR[0]	Y	DRV2_IER[5:3]	IP9[2:0]
PFC Interrupt	10	0x00000028	PFC_CR2[10]	Y	PFC_CR2[15]	IP10[2:0]
ADC1/2/3 Interrupt	11	0x0000002C	ADC1_CR[0] ADC2_CR[0] ADC3_CR[0]	Y	ADC1_CR[1] ADC2_CR[1] ADC3_CR[1]	IP11[2:0]
DMA0/1 Interrupt	12	0x00000030	DMA0_CR[1:0] DMA1_CR[1:0]	Y	DMA0_CR[12:11] DMA1_CR[12:11]	IP12[2:0]
DMA2/3 Interrupt	13	0x00000034	DMA2_CR[1:0] DMA3_CR[1:0]	Y	DMA2_CR[12:11] DMA3_CR[12:11]	IP13[2:0]
DMA4/5 Interrupt	14	0x00000038	DMA4_CR[1:0] DMA5_CR[1:0]	Y	DMA4_CR[12:11] DMA5_CR[12:11]	IP14[2:0]
Systick Interrupt	15	0x0000003C	SYST_SR[1]	Y	SYST_SR[0]	IP15[2:0]
Timer2 Interrupt	16	0x00000040	TIM2_IFR[2:0]	Y	TIM2_IER[2:0]	IP16[2:0]
Timer3 Interrupt Timer8 Interrupt	17	0x00000044	TIM3_IFR[2:0] TIM8_IFR[2:0]	Y	TIM3_IER[2:0] TIM8_IER[2:0]	IP17[2:0]
Timer4 Interrupt	18	0x00000048	TIM4_IFR[2:0]	Y	TIM4_IER[2:0]	IP18[2:0]
Timer5 Interrupt	19	0x0000004C	TIM5_IFR[2:0]	Y	TIM5_IER[2:0]	IP19[2:0]
Timer6 Interrupt	20	0x00000050	TIM6_IFR[2:0]	Y	TIM6_IER[2:0]	IP20[2:0]
Timer7 Interrupt	21	0x00000054	TIM7_IFR[2:0]	Y	TIM7_IER[2:0]	IP21[2:0]
WWDT Interrupt	22	0x00000058	WWDT_SR[0]	Y	WWDT_CFR[9]	IP22[2:0]
RTC Interrupt MCD Interrupt PLL Interrupt	23	0x0000005C	RTC_CR[6] OSC_SR[0] OSC_SR[1]	Y	PIE[4] OSC_CR[4] OSC_CR[5]	IP23[2:0]
I ² C1 Interrupt I ² C2 Interrupt	24	0x00000060	I2C1_SR[0] I2C2_SR[0]	Y	I2C1_CR[0] I2C2_CR[0]	IP24[2:0]
SPI1 Interrupt	25	0x00000064	SPI1_SR[3]	Y	SPI1_CR[2]	IP25[2:0]
SPI2 Interrupt	26	0x00000068	SPI2_SR[3]	Y	SPI2_CR[2]	IP26[2:0]
UART1 Interrupt	27	0x0000006C	UT1_CR1[10:9]	Y	UT1_CR0[1:0] UT1_CR0[10]	IP27[2:0]
UART2 Interrupt	28	0x00000070	UT2_CR1[10:9]	Y	UT2_CR0[1:0] UT2_CR0[10]	IP28[2:0]
LIN Interrupt	29	0x00000074	LIN_SR[4:0]	Y	LIN_CR[3]	IP29[2:0]
CAN Interrupt	30	0x00000078	CAN_IFR[8:0]	Y	CAN_IER[12:0]	IP30[2:0]
BISS Interrupt	31	0x0000007C	BISS_STATE[2]	Y	BISS_STATE[1]	IP31[2:0]

**Note:**

UTx_CR0[UTRI], UTx_CR0[UTTI], DMAx_CR[DMAIF] and DMAx_CR[DMAHIF] bits can be cleared to “0” or set to “1” by software, and MCU generates an interrupt request when these flags are set to “1”. Other flags can only be cleared to “0” by software, and setting them to “1” has no effect.

7.5 Interrupt Registers

7.5.1 MIE (CSR: 0x300)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												IRQ_EN	RSV		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	-	-	-	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	

Bit	Name	Description
[31:4]	RSV	Reserved
[3]	IRQ_EN	All Interrupts Enable 0: Disable 1: Enable
[2:0]	RSV	Reserved

7.5.2 MTVEC (CSR:0x305)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTVEC																								RSV				NO_USE			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	-	-	-	-	-	-	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	0

Bit	Name	Description
[31:8]	MTVEC	All exception and interrupt jump addresses are computed as (VEC << 8) + vector address.
[7:1]	RSV	Reserved
[0]	NO_USE	The initial value is 0, and any write to MTVEC sets this bit to 1.

7.5.3 IPx (CSR: 0x409 + x) (x = 0/1/2/.../31)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																													IP		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit	Name	Description
[31:3]	RSV	Reserved
[2:0]	IP	Interrupt Priority Control



Note:

Priority level assigned ascends from 0 to 7, totaling 8 levels.

7.5.4 PIE (CSR: 0x400)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit	Name	Description
[31:5]	RSV	Reserved
[4]	RTCIE	RTC Interrupt Enable 0: Disable 1: Enable
[3]	TSDIE	TSD Interrupt Enable 0: Disable 1: Enable
[2]	EX2	EXTI2 Enable 0: Disable 1: Enable
[1]	EX1	EXTI1 Enable 0: Disable 1: Enable
[0]	EX0	EXTI0 Enable

		0: Disable
		1: Enable

7.5.5 EXTI_TCON (CSR: 0x407)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								TSDIF		IT2		IT1		IT0	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:7]	RSV	Reserved
[6]	TSDIF	TSD Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5:4]	IT2	EXTI2 Trigger Level Selection 00: Interrupt on rising edge 01: Interrupt on falling edge 1x: Interrupt on level change (rising or falling)
[3:2]	IT1	EXTI1 Trigger Level Selection 00: Interrupt on rising edge 01: Interrupt on falling edge 1x: Interrupt on level change (rising or falling)
[1:0]	IT0	EXTI0 Trigger Level Selection 00: Interrupt on rising edge 01: Interrupt on falling edge 1x: Interrupt on level change (rising or falling)

7.5.6 EXTIOIE (CSR: 0x401)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX0IE15	RSV	EX0IE13	EX0IE12	EX0IE11	EX0IE10	EX0IE9	RSV	EX0IE7	EX0IE6	EX0IE5	EX0IE4	EX0IE3	EX0IE2	EX0IE1	EX0IE0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX0IE15	PD3 EXTIO Enable 0: Disable 1: Enable
[14]	RSV	Reserved
[13]	EX0IE13	PD0 EXTIO Enable 0: Disable 1: Enable
[12]	EX0IE12	PA12 EXTIO Enable 0: Disable 1: Enable
[11]	EX0IE11	PA11 EXTIO Enable 0: Disable 1: Enable
[10]	EX0IE10	PA10 EXTIO Enable 0: Disable 1: Enable
[9]	EX0IE9	PA9 EXTIO Enable 0: Disable 1: Enable
[8]	RSV	Reserved
[7]	EX0IE7	PA7 EXTIO Enable 0: Disable 1: Enable
[6]	EX0IE6	PA6 EXTIO Enable 0: Disable 1: Enable
[5]	EX0IE5	PA5 EXTIO Enable 0: Disable

		1: Enable
[4]	EX0IE4	PA4 EXTI0 Enable 0: Disable 1: Enable
[3]	EX0IE3	PA3 EXTI0 Enable 0: Disable 1: Enable
[2]	EX0IE2	PA2 EXTI0 Enable 0: Disable 1: Enable
[1]	EX0IE1	PA1 EXTI0 Enable 0: Disable 1: Enable
[0]	EX0IE0	PA0 EXTI0 Enable 0: Disable 1: Enable

7.5.7 EXTI1IE (CSR: 0x402)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX1IE15	EX1IE14	EX1IE13	EX1IE12	EX1IE11	EX1IE10	EX1IE9	RSV	EX1IE7	EX1IE6	EX1IE5	EX1IE4	EX1IE3	EX1IE2	EX1IE1	EX1IE0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX1IE15	PB2 EXTI1 Enable 0: Disable 1: Enable
[14]	EX1IE14	PA14 EXTI1 Enable 0: Disable 1: Enable
[13]	EX1IE13	PA13 EXTI1 Enable 0: Disable 1: Enable
[12]	EX1IE12	PA12 EXTI1 Enable 0: Disable 1: Enable

[11]	EX1IE11	PA11 EXTI1 Enable 0: Disable 1: Enable
[10]	EX1IE10	PA10 EXTI1 Enable 0: Disable 1: Enable
[9]	EX1IE9	PA9 EXTI1 Enable 0: Disable 1: Enable
[8]	RSV	Reserved
[7]	EX1IE7	PA7 EXTI1 Enable 0: Disable 1: Enable
[6]	EX1IE6	PA6 EXTI1 Enable 0: Disable 1: Enable
[5]	EX1IE5	PA5 EXTI1 Enable 0: Disable 1: Enable
[4]	EX1IE4	PA4 EXTI1 Enable 0: Disable 1: Enable
[3]	EX1IE3	PA3 EXTI1 Enable 0: Disable 1: Enable
[2]	EX1IE2	PA2 EXTI1 Enable 0: Disable 1: Enable
[1]	EX1IE1	PA1 EXTI1 Enable 0: Disable 1: Enable
[0]	EX1IE0	PA0 EXTI1 Enable 0: Disable 1: Enable

7.5.8 EXTI2IE (CSR: 0x403)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX2IE15	EX2IE14	EX2IE13	EX2IE12	EX2IE11	EX2IE10	EX2IE9	EX2IE8	EX2IE7	EX2IE6	EX2IE5	EX2IE4	EX2IE3	EX2IE2	EX2IE1	EX2IE0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX2IE15	PC7 EXTI2 Enable 0: Disable 1: Enable
[14]	EX2IE14	PC6 EXTI2 Enable 0: Disable 1: Enable
[13]	EX2IE13	PC5 EXTI2 Enable 0: Disable 1: Enable
[12]	EX2IE12	PC4 EXTI2 Enable 0: Disable 1: Enable
[11]	EX2IE11	PC3 EXTI2 Enable 0: Disable 1: Enable
[10]	EX2IE10	PC2 EXTI2 Enable 0: Disable 1: Enable
[9]	EX2IE9	PC1 EXTI2 Enable 0: Disable 1: Enable
[8]	EX2IE8	PC0 EXTI2 Enable 0: Disable 1: Enable
[7]	EX2IE7	PB7 EXTI2 Enable 0: Disable 1: Enable
[6]	EX2IE6	PB6 EXTI2 Enable 0: Disable 1: Enable

[5]	EX2IE5	PB5 EXTI2 Enable 0: Disable 1: Enable
[4]	EX2IE4	PB4 EXTI2 Enable 0: Disable 1: Enable
[3]	EX2IE3	PB3 EXTI2 Enable 0: Disable 1: Enable
[2]	EX2IE2	PB2 EXTI2 Enable 0: Disable 1: Enable
[1]	EX2IE1	PB1 EXTI2 Enable 0: Disable 1: Enable
[0]	EX2IE0	PB0 EXTI2 Enable 0: Disable 1: Enable

7.5.9 EXTI0IF (CSR: 0x404)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX0IF15	RSV	EX0IF13	EX0IF12	EX0IF11	EX0IF10	EX0IF9	RSV	EX0IF7	EX0IF6	EX0IF5	EX0IF4	EX0IF3	EX0IF2	EX0IF1	EX0IF0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0	-	rw0	rw0	rw0	rw0	rw0	-	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX0IF15	PD3 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[14]	RSV	Reserved
[13]	EX0IF13	PD0 EXTI0 Flag

		Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[12]	EX0IF12	PA12 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[11]	EX0IF11	PA11 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[10]	EX0IF10	PA10 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[9]	EX0IF9	PA9 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[8]	RSV	Reserved
[7]	EX0IF7	PA7 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write:

		0: This bit is cleared to “0” 1: No effect
[6]	EX0IF6	PA6 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	EX0IF5	PA5 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	EX0IF4	PA4 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[3]	EX0IF3	PA3 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	EX0IF2	PA2 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	EX0IF1	PA1 EXTI0 Flag Read: 0: No interrupt pending

		1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	EX0IF0	PA0 EXTI0 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

7.5.10 EXTI1IF (CSR: 0x405)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX1IF15	EX1IF14	EX1IF13	EX1IF12	EX1IF11	EX1IF10	EX1IF9	RSV	EX1IF7	EX1IF6	EX1IF5	EX1IF4	EX1IF3	EX1IF2	EX1IF1	EX1IF0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r0	r0	r0	r0	r0	r0	r0	-	r0	r0	r0	r0	r0	r0	r0	r0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX1IF15	PB2 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[14]	EX1IF14	PA14 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[13]	EX1IF13	PA13 EXTI1 Flag

		Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[12]	EX1IF12	PA12 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[11]	EX1IF11	PA11 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[10]	EX1IF10	PA10 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[9]	EX1IF9	PA9 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[8]	RSV	Reserved
[7]	EX1IF7	PA7 EXTI1 Flag Read:

		0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	EX1IF6	PA6 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	EX1IF5	PA5 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	EX1IF4	PA4 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[3]	EX1IF3	PA3 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	EX1IF2	PA2 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write:

		0: This bit is cleared to “0” 1: No effect
[1]	EX1IF1	PA1 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	EX1IF0	PA0 EXTI1 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

7.5.11 EXTI2IF (CSR: 0x406)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																EX2IF15	EX2IF14	EX2IF13	EX2IF12	EX2IF11	EX2IF10	EX2IF9	EX2IF8	EX2IF7	EX2IF6	EX2IF5	EX2IF4	EX2IF3	EX2IF2	EX2IF1	EX2IF0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	EX2IF15	PC7 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[14]	EX2IF14	PC6 EXTI2 Flag Read: 0: No interrupt pending

		1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[13]	EX2IF13	PC5 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[12]	EX2IF12	PC4 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[11]	EX2IF11	PC3 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[10]	EX2IF10	PC2 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[9]	EX2IF9	PC1 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write:

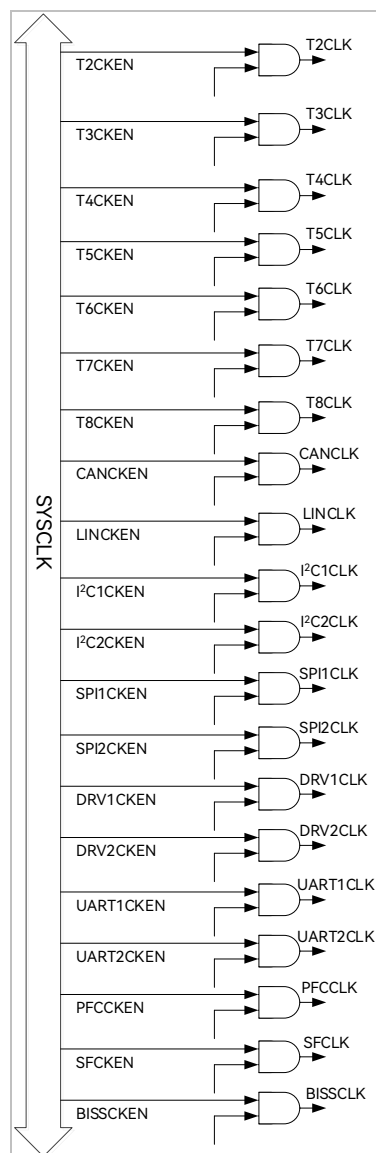
		0: This bit is cleared to “0” 1: No effect
[8]	EX2IF8	PC0 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[7]	EX2IF7	PB7 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	EX2IF6	PB6 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	EX2IF5	PB5 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	EX2IF4	PB4 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

[3]	EX2IF3	PB3 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	EX2IF2	PB2 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	EX2IF1	PB1 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	EX2IF0	PB0 EXTI2 Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

8 Clock Gating

Timer2 ~ Timer8, CAN, LIN, I²C1, I²C2, SPI1, SPI2, DRV1, DRV2, UART1, UART2, PFC, SF and BISS modules are designed with a separate clock gating circuit. The clock enable bits in CK_CR register controls clock gating feature of these modules.

Figure 8-1 Clock Tree



8.1 Clock Gating Register

8.1.1 CK_CR (CSR: 0x080)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												T8CKEN	I2C2EN	SFCKEN	BISSCKEN	DRV2CKEN	DRV1CKEN	PFCKEN	UART2CKEN	UART1CKEN	LINCKEN	SPI2CKEN	SPI1CKEN	I2C1CKEN	CANCKEN	T7CKEN	T6CKEN	T5CKEN	T4CKEN	T3CKEN	T2CKEN
												rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:20]	RSV	Reserved
[19]	T8CKEN	Timer8 Clock Enable 0: Disable 1: Enable
[18]	I2C2EN	I2C2 Clock Enable 0: Disable 1: Enable
[17]	SFCKEN	SF Clock Enable 0: Disable 1: Enable
[16]	BISSCKEN	BISS Clock Enable 0: Disable 1: Enable
[15]	DRV2CKEN	DRV2 Clock Enable 0: Disable 1: Enable  Note This bit shall be disabled before the chip enters sleep mode.
[14]	DRV1CKEN	DRV1 Clock Enable 0: Disable 1: Enable  Note This bit shall be disabled before the chip enters sleep mode.

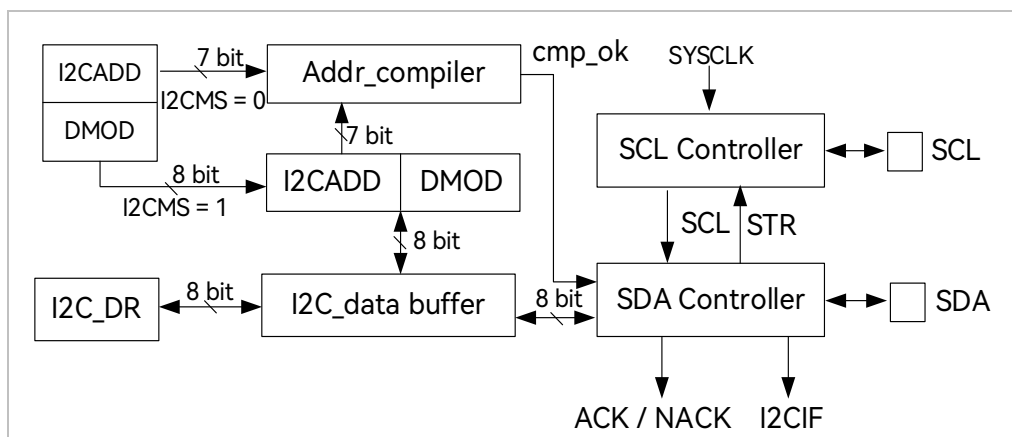
[13]	PFCKEN	PFC Clock Enable 0: Disable 1: Enable
[12]	UART2CKEN	UART2 Clock Enable 0: Disable 1: Enable
[11]	UART1CKEN	UART1 Clock Enable 0: Disable 1: Enable
[10]	LINCKEN	LIN Clock Enable 0: Disable 1: Enable
[9]	SPI2CKEN	SPI2 Clock Enable 0: Disable 1: Enable
[8]	SPI1CKEN	SPI1 Clock Enable 0: Disable 1: Enable
[7]	I2C1CKEN	I ² C1 Clock Enable 0: Disable 1: Enable
[6]	CANCKEN	CAN Clock Enable 0: Disable 1: Enable
[5]	T7CKEN	Timer7 Clock Enable 0: Disable 1: Enable
[4]	T6CKEN	Timer6 Clock Enable 0: Disable 1: Enable
[3]	T5CKEN	Timer5 Clock Enable 0: Disable 1: Enable
[2]	T4CKEN	Timer4 Clock Enable 0: Disable 1: Enable
[1]	T3CKEN	Timer3 Clock Enable 0: Disable 1: Enable
[0]	T2CKEN	Timer2 Clock Enable 0: Disable 1: Enable

9 I²C

9.1 I²C Introduction

The I²C module provides an industry standard two-wire serial interface and is a simple bi-directional synchronous serial bus for the communication between MCU and external I²C devices, as shown in Figure 9-1. The bus consists of two serial lines: SDA (serial data line) and SCL (serial clock line). After I²C is enabled, SDA and SCL automatically switch to open-drain outputs.

Figure 9-1 Block Diagram of I²C Module



Features:

- > Supports standard mode (up to 100kHz), fast mode (up to 400kHz) and fast plus mode (up to 1MHz)
- > Supports master mode and slave mode
- > Supports 7-bit address mode and general call address mode
- > Supports DMA data transfer

Both SDA and SCL lines are high level when the bus is idle, which is the only basis for detecting whether the bus is idle or not. Only one master device and at least one slave device are active on the bus during the transmission. When the bus is occupied, other devices must wait for the bus idle to start an I²C communication. The master starts the bus to transfer data. Clock signal is sent to all devices via SCL and the slave address and read/write mode are sent via SDA. When a device on the bus matches the address, it acts as a slave. The relationships between masters and slaves or data transfer direction on the bus are not constant. The process for the master to send data to the slave is shown in Figure 9-2. The master first

addresses the slave device and waits for the slave response. And then, it sends data to the slave. Finally, the master terminates the data transmission. The process for the master to receive data from the slave is shown in Figure 9-3. The master first addresses the slave and waits for the slave response. And then, it receives the data from the slave. Finally, the master terminates the data transmission. In this case, the master generates the timing clock and stops the data transmission.

Figure 9-2 Master Transmits Data to Slave

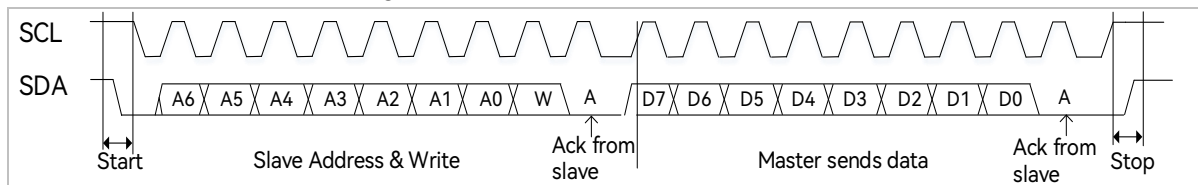
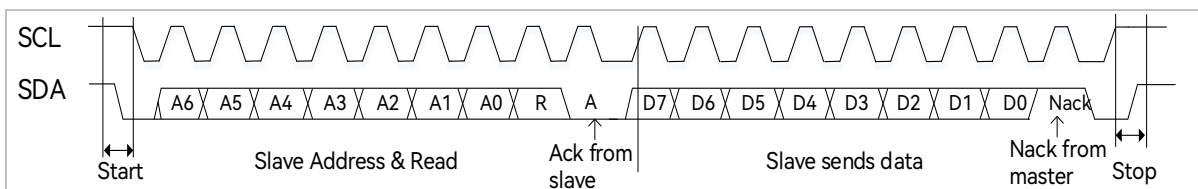


Figure 9-3 Master Receives Data from Slave



9.2 I²C Operations

9.2.1 Master Mode

1. Set I2Cx_CR[I2CMS] = 1 to select master mode;
2. Configure I2Cx_BAUD to set the clock rate of SCL;
3. Configure I2Cx_ID[I2CADD] to set the slave address;
4. Configure I2Cx_SR[DMOD] to set the read/write direction;
5. Set I2Cx_CR[I2CEN] = 1 to enable I²C;
6. Set I2Cx_SR[I2CSTA] to “1” to transmit START and address. After ACK/NACK is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;
7. Sending Data: Write the data to I2Cx_DR register. The master starts to transmit data when I2Cx_SR[STR] is cleared and SCL is released. After the data is transmitted and ACK/NACK is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;

8. **Receiving Data:** The master starts to receive data when I2Cx_SR[STR] is cleared and SCL is released. After the data is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master. Configure ACK/NACK via I2Cx_SR[NACK], and then clear I2Cx_SR[STR] to release SCL to transmit ACK/NACK signal. After the data is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the master;
9. **Stop Communication:** Set I2Cx_SR[STR] to “1” when I2Cx_SR[I2CSTP] is “1” and stop signal is sent after I2Cx_SR[STR] is cleared.

9.2.2 Slave Mode

1. Set I2Cx_CR[I2CMS] to “0” to select slave mode;
2. Configure I2Cx_ID[I2CADD] to set the slave address or set I2Cx_ID[GC] to “1” to enable general call mode;
3. Set I2Cx_CR[I2CEN] to “1” to enable I²C;
4. After START signal and the correct address are received, I2Cx_SR[I2CSTA] and I2Cx_SR[STR] are set to “1” by hardware and SCL is pulled LOW by the slave. ACK/NACK is configured via I2Cx_SR[NACK] and the slave determines whether to receive or send the data via I2Cx_SR[DMOD];
5. **Sending Data:** Write the data to I2Cx_DR register, and clear I2Cx_SR[STR] to release SCL. The data is sent after ACK/NACK is transmitted. After the data is sent and ACK/NACK is received from the master, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave;
6. **Receiving Data:** Clear I2Cx_SR[STR] to release SCL to receive data. After the data is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave. ACK/NACK is configured via I2Cx_SR[NACK] to clear I2Cx_SR[STR] to release SCL for ACK/NACK transmission. If the data is received, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW by the slave;
7. **RESTART:** If the slave is processing a service when receiving START signal, it stops the current routine and waits for receiving address.

9.2.3 I²C Interrupt Sources

The interrupt sources of I²C include:

- > I2Cx_SR[STR] = 1 generates an interrupt. This interrupt source is valid in both master and slave modes.
- > I2Cx_SR[I2CSTP] = 1 generates an interrupt. This interrupt source is only valid in slave mode.

9.3 I²C Registers

9.3.1 I2Cx_CR (CSR: 0x160/0x170) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								I2CEN	I2CMS	RSV	I2CDMANAKIG	I2CDMASEND AUTO	RSV	I2CFSEL	I2CIE
																								r/w	r/w	-	r/w	r/w	-	r/w	r/w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	-	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	I2CEN	I ² C Enable The associated GPIO is enabled to switch to I ² C mode, serving as open-drain output. The pull-up setting decides whether to pull I ² C HIGH. 0: Disable 1: Enable
[6]	I2CMS	Master/Slave Mode Selection 0: Slave 1: Master
[5]	RSV	Reserved
[4]	I2CDMANAKIG	An interrupt is generated when the chip does not acknowledge (NACK) the received the data during DMA transmission. 0: Disable 1: Enable
[3]	I2CDMASEND AUTO	The first byte of data is automatically transferred during DMA transmission. 0: Disable 1: Enable
[2]	RSV	Reserved

[1]	I2CFSEL	I ² C Filtering 0: 50ns glitch filter on SCL, and 125ns on SDA (fast plus mode) 1: 100ns glitch filter on SCL, and 175ns on SDA (standard or fast mode)
[0]	I2CIE	I ² C Interrupt Enable 0: Disable 1: Enable

9.3.2 I2Cx_ID (CSR: 0x161/0x171) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								I2CADD				GC			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0	1	0	1	0	1	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:1]	I2CADD	Slave address
[0]	GC	General call, valid only in Slave Mode 0: Disable 1: Enable. The receiving device responds at address 0x00.

9.3.3 I2Cx_DR (CSR: 0x162/0x172) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								I2C_DR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	I2C_DR	I ² C Data Register Read: Data to be sent or received Write: Data to be sent

9.3.4 I2Cx_SR (CSR: 0x163/0x173) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								I2CBSY	DMOD	RSV	I2CSTA	I2CSTP	STR	NACK	I2CIF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	rw	-	rw	rw	rw0	rw	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	I2CBSY	I²C Busy Flag When I2Cx_CR[I2CEN] = 0, I2Cx_SR[I2CBSY] is cleared to “0” by hardware. Master Mode: After START is transmitted, this bit is set to “1” by hardware, and after STOP is transmitted, it is cleared to “0” by hardware. Slave Mode: After START is received and address matches, this bit is set to “1” by hardware, and after STOP is received, it is cleared to “0” by hardware.
[6]	DMOD	I²C R/W Flag 0: Write (master sends the data, and slave receives the data) 1: Read (master receives the data, and slave sends the data)  Note: It is read-only in slave mode.
[5]	RSV	Reserved
[4]	I2CSTA	Master Mode: When this bit is configured with “1”, START and address bytes are transmitted after both SCL and SDA are HIGH confirmed by the hardware. This bit is cleared to “0” by hardware automatically after the transmission is completed. I2Cx_SR[I2CSTA] writing is forbidden during data transmission. After the data is sent or received, I2Cx_SR[I2CSTA] is set to “1” to transmit RESTART. 0: No START and address bytes are transmitted 1: START or RESTART and address bytes are transmitted Slave Mode: This bit is set to “1” after hardware receives START and address matches,

		and cleared to “0” by software. The relationship between I2Cx_SR[I2CSTA]/I2Cx_SR[I2CSTP] and I²C data type in slave mode is shown in Table 9-1. Table 9-1 Mapping of I2Cx_SR[I2CSTA]/I2Cx_SR[I2CSTP] and I²C Data Type in Slave Mode <table><tr><th>I2CSTA</th><th>I2CSTP</th><th>I²C Data Type</th></tr><tr><td>0</td><td>0</td><td>Data byte</td></tr><tr><td>0</td><td>1</td><td>STOP</td></tr><tr><td>1</td><td>0</td><td>START + address bytes</td></tr><tr><td>1</td><td>1</td><td>STOP received first, then START + address bytes</td></tr></table>  Note: When I2Cx_CR[I2CEN] = 0, I2Cx_SR[I2CSTA] is automatically cleared to “0”	I2CSTA	I2CSTP	I ² C Data Type	0	0	Data byte	0	1	STOP	1	0	START + address bytes	1	1	STOP received first, then START + address bytes
I2CSTA	I2CSTP	I ² C Data Type															
0	0	Data byte															
0	1	STOP															
1	0	START + address bytes															
1	1	STOP received first, then START + address bytes															
[3]	I2CSTP	Master Mode: This bit cannot be written to “1” by software unless I2Cx_SR[I2CBSY] = 1; STOP is transmitted after I2Cx_SR[STR] is cleared to release SCL. After the transmission, this bit is cleared to “0” automatically by hardware. If I2Cx_SR[I2CSTA] and I2Cx_SR[I2CSTP] are written to “1” at the same time and I2Cx_SR[I2CBSY] is “1”, I²C first sends STOP, then START and address bytes. After START and address bytes are transmitted, I2Cx_SR[STR] is set to “1” by hardware. I2Cx_SR[I2CSTP] writing is not allowed during data transmission. 0: STOP is not transmitted. 1: STOP is transmitted. Slave Mode: This bit is set to “1” by hardware after STOP is received, and cleared to “0” by software. See Table 9-1 for status flags.  Note: When I2Cx_CR[I2CEN] = 0, I2Cx_SR[I2CSTP] is automatically cleared to “0”.															
[2]	STR	I²C Bus Pending Flag Master Mode: After START and address or DATA bytes are transmitted, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW. SCL is released after I2Cx_SR[STR] is cleared by software.															

		When I2Cx_SR[I2CSTA] and I2Cx_SR[I2CSTP] are both “1”, I2Cx_SR[STR] is set to “1” only after hardware sends STOP and START & address bytes. Slave Mode: When DATA byte is received or START is received and address matches, I2Cx_SR[STR] is set to “1” by hardware and SCL is pulled LOW. SCL is released after I2Cx_SR[STR] is cleared by software.  Note: The bit is set to “1” by hardware and cleared to “0” by software. When I2Cx_CR[I2CEN] = 0, I2Cx_SR[STR] is automatically cleared to “0”.
[1]	NACK	This bit refers to the feedback from a receiver to a sender after a byte is transferred via I²C. It is automatically cleared to “0” if I2Cx_SR[I2CEN] = 0. 0: ACK, indicating that the receiver can continue to receive data. 1: NACK, indicating that the receiver attempts to stop data transmission. When the device is in READ mode, I2Cx_SR[NACK] is configured to transmit ACK/NACK after the 8th bit of data is received. 0: Bit9 transmits ACK 1: Bit9 transmits NACK When the device is in WRITE mode, I2Cx_SR[NACK] is read to receive ACK/NACK after the 8th bit of data is transmitted. 0: Bit9 receives ACK 1: Bit9 receives NACK
[0]	I2CIF	I²C Interrupt Flag 0: No Interrupt Pending 1: Interrupt Pending When I2Cx_SR[STR] = 1, an interrupt is generated in both Master and Slave modes. When I2Cx_SR[I2CSTP] = 1, an interrupt is generated only in Slave mode.

9.3.5 I2Cx_BAUD (CSR: 0x164/0x174) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								I2Cx_BAUD							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	I2Cx_BAUD	I ² C Baud Rate. Baud rate = I ² CxCLK / I2Cx_BAUD

in a high-impedance state when the SPI module is disabled or when the SPI operates in 4-wire mode as a slave that is not selected. When the SPI acts as a slave in 3-wire mode or operates in 4-wire mode as a slave that is selected, MISO is used to serially transfer data from the slave to the master. Data is transferred with most-significant bit (MSB) first, namely, the master begins its transmission by driving the MSB of the shift register on its MISO pin.

10.2.4 Serial Clock (SCLK)

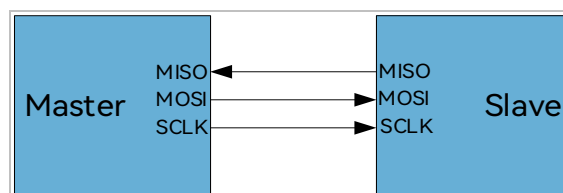
The serial clock (SCLK) signal is an output from the master device and an input to slave devices. It is used to synchronize serial data transmission between the master and slave. SCLK signal is generated by SPI operating as a master. In 4-wire slave mode, SCLK is ignored when the slave device is not selected (NSS=1).

10.2.5 Slave Select (NSS)

The slave-select (NSS) is dependent on the setting of SPIx_CR[NSSMOD] bit. SPI can communicate in 3-wire mode, 4-wire slave/multi-master mode, 4-wire single master mode or single-wire half-duplex mode (namely, 3-wire mode, 4-wire mode or half-duplex mode). When SPI operates in 4-wire slave/multi-master mode, NSS is enabled as an input. In this mode, a particular SPI master function is disabled to prevent SPIx bus collision where two or more masters simultaneously initiate data transfer. When SPI operates in 4-wire single master mode, the master NSS is configured as chip select output. When SPI operates in 3-wire mode, NSS is disabled. When SPI operates as a master, multiple addressed slave devices can be selected using general-purpose I/O pins.

When SPIx_CR[NSSMOD] = 00, SPIx communicates in 3-wire mode. NSS port is not necessary in this mode and there is only one master and one slave on the SPI bus. The connection diagram is shown in Figure 10-2.

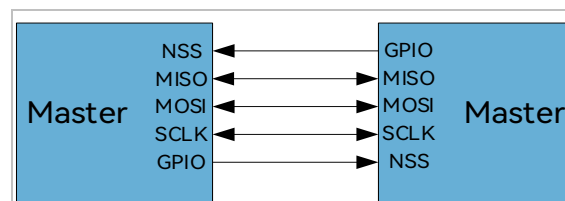
Figure 10-2 Connection Diagram of 3-wire SPI Mode



When SPIx_CR[NSSMOD] = 01, SPIx communicates in 4-wire slave/multi-master mode. In this mode, SPIx NSS pin is configured as an input, waiting to be addressed by the master. When SPIx_CR[SPIMS] = 0, SPIx

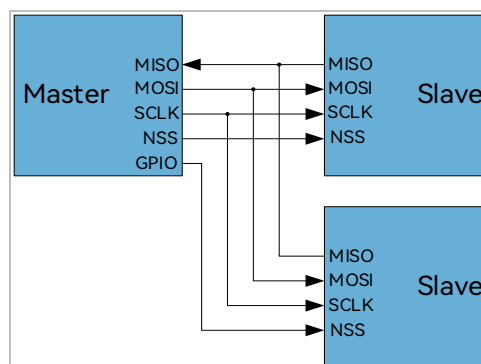
operates in 4-wire slave mode. If NSS is set to “0” (low level), the slave SPIx is selected; while NSS is set to “1” (high level), the slave SPIx is not selected. When SPIx_CR[SPIMS] = 1, SPIx operates in master mode and defaults to multi-master mode. In multi-master mode, NSS is configured as an input to disable the master SPIx. When NSS pin of a master on the SPI bus is pulled low, SPIx_CR[SPIMS] and SPIx_CR[SPIEN] are cleared to “0” by hardware to disable the SPIx, and the interrupt flag bit SPIx_CR[MODF] is set to “1”. In this case, SPI communication remains halted before the SPI is re-enabled by software. In this mode, multiple masters are allowed for communication on the SPI bus. The connection diagram is shown in Figure 10-3.

Figure 10-3 Connection Diagram of 4-wire Multi-Master Mode



When SPIx_CR[NSSMOD] = 1x, SPIx communicates in 4-wire Single Master Mode. In this mode, NSS pin of the master on SPI bus is configured as an output, and NSS pin of the slave is configured as an input. SPIx_CR[NSSMOD0] setting decides the output level of NSS pin serving as signal to select a slave. Other slaves can be selected using GPIO pins. The connection diagram is shown in Figure 10-4.

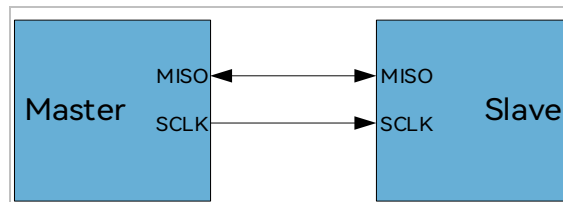
Figure 10-4 Connection Diagram of 4-wire Single Master Mode



10.2.6 Single-wire Half-duplex Mode (SLINE)

When SPIx_CR[SLINE] = 1, SPIx communicates in single-wire half-duplex mode. In this mode, SPIx begins data transmission by driving the MSB of the shift register on its MISO pin. The direction of data flow is selected by SPIx_CR[SCKRQ]. When SPIx_CR[SCKRQ] = 1, the slave starts data transmission. The connection diagram is shown in Figure 10-5.

Figure 10-5 Connection Diagram of Single-wire Half-duplex Mode



10.2.7 SPI Master Mode

When $\text{SPIx\_CR}[\text{SPIMS}] = 1$, SPIx operates in master mode, which provides SCLK signal for SPI bus. When the data is written to SPIx_DR, it is firstly written to the transmit buffer and SPIx_SR[TXBMT] is cleared to “0”. If the shift register is empty, the data in the transmit buffer will be transferred to the shift register for the transmission. The master SPIx begins its transmission by driving the MSB of shift register on its MOSI pin. After the transmission is completed, SPIx_SR[SPIIF] and SPIx_SR[TXBMT] are set to “1”. While the SPI master transfers data to a slave on the MOSI line, the addressed SPI slave simultaneously transfers data in the shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, SPIx_SR[SPIIF] flag serves as both a transmit-complete flag and a receive-data-ready flag, and the data in the shift register is that received by MISO, which is transferred to the receive buffer. The data from SPIx_DR is that of the receive buffer. If the data is written to SPIx_DR when SPIx_SR[TXBMT] = 0, the write conflict flag bit SPIx_SR[WCOL] will be set to “1” and the data in the transmit buffer keeps unchanged.

10.2.7.1 Master Mode Configurations

1. Configure SPIx_CR[NSSMOD] to set the SPIx operating mode;
2. Configure SPIx_CR[SLINE] = 1/0 to select half-duplex/full-duplex mode;
3. Configure SPIx_CR[CPOL] to set the clock polarity;
4. Configure SPIx_CR[CPHA] to set the clock phase;
5. Set SPIx_CR[SPIMS] to “1” to select master mode;
6. Configure SPIx_CLK to set the SCLK rate;
7. Set SPIx_CR[SPIEN] to “1” to enable SPI;
8. Write the data to SPIx_DR. SPIx transmits data for each write;

9. After SPIx_SR[SPIIF] is set to “1”, read SPIx_DR to obtain the data;
10. Set SPIx_CR[SCKRQ] = 1 to start data receiving in half-duplex mode.

10.2.8 SPI Slave Mode

When SPIx_CR[SPIMS] = 0, SPIx operates in slave mode. In this mode, SCLK signal is sent by the master SPI. The data is shifted in from MOSI pin and shifted out from MISO pin. If no SCLK signal is detected, shift register of the slave is in the stop state. If SCLK signal is detected, the shift register of slave starts to receive and send data through MOSI and MISO pins. The slave device cannot initiate transfers. The data sent to the master device is pre-loaded into the shift register by writing to SPIx_DR. If the shift register is empty, the data in the transit buffer is transferred into the shift register. After the transmission is completed, SPIx_SR[SPIIF] and SPIx_SR[TXBMT] are set to “1”. The received data that is transferred into receive buffer and receive buffer empty flag bit SPIx_SR[RXBMT] is cleared, indicating the data has not been read. If SPIx_SR[RXBMT] is “0” and there is data ready to be sent to the receive buffer, SPIx_SR[RXOVRN] is set to “1” and the data in the receive buffer remains unaffected. When data is written to SPIx_DR, SPIx_SR[TXBMT] is cleared. If data is written in this case, the write conflict flag bit SPIx_SR[WCOL] is set to “1” and the data in the transmit buffer keeps unchanged.

10.2.8.1 Slave Mode Configurations

1. Configure SPIx_CR[NSSMOD] to set the SPIx operating mode;
2. Configure SPIx_CR[SLINE] = 1/0 to select half-duplex/full-duplex mode
3. Configure SPIx_CR[CPOL] to set the clock polarity;
4. Configure SPIx_CR[CPHA] to set the clock phase;
5. Set SPIx_CR[SPIMS] to “0” to select slave mode;
6. Set SPIx_CR[SPIEN] to “1” to enable SPI;
7. Write data to SPIx_DR and wait for the master to transmit the clock signal.

10.2.9 SPI Interrupt Sources

The interrupt sources of SPI include:

- SPIx interrupt flag SPIx_SR[SPIIF] is set to “1” each time after the byte is transferred.
- If SPIx_DR is written when the data in transmit buffer has not been transferred to the shift register, the write conflict flag SPIx_SR[WCOL] is set to “1” and the write operation will not be implemented.
- When SPIx works as a master in a multi-master system and NSS pin is pulled LOW, the mode error flag SPIx_SR[MODF] is set to “1”. When a mode error occurs, SPIx_CR[SPIMS] and SPIx_CR[SPIEN] are cleared. SPIx is forbidden to allow another master to control the bus.
- The receive overflow flag SPIx_SR[RXOVRN] is set to “1” when SPIx operates in slave mode and a transmission is completed while the receive buffer still holds unread data from a previous transfer. The received data will not be transferred to the receive buffer.

10.2.10 Serial Clock Timing

Four combinations of serial clock phase and idle polarity can be selected using the CPHA and CPOL bits in the SPIx_CR Register. SPIx_CR[CPHA] selects the clock phase (the edge of the SCLK signal used to latch the data in shift register). SPIx_CR[CPOL] selects the polarity. Both master and slave devices must be configured with the same clock phase and polarity. When the clock phase and polarity is configured, SPIx shall be disabled (SPIx_CR[SPIEN] = 0). The timing relationships of clock line and data line in clock phase and polarity combinations are shown in Figure 10-6 and Figure 10-7.

Figure 10-6 Data/Clock Line Timing Diagram (SPIx_CR[CPHA] = 0)

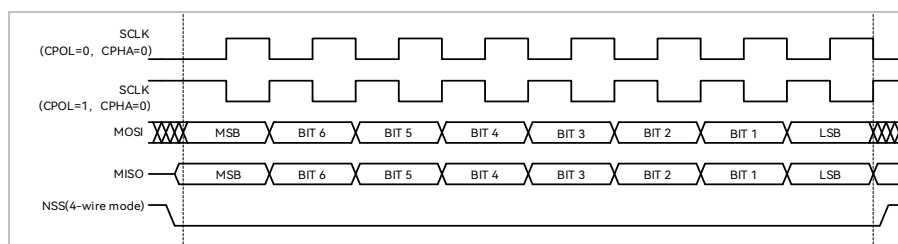
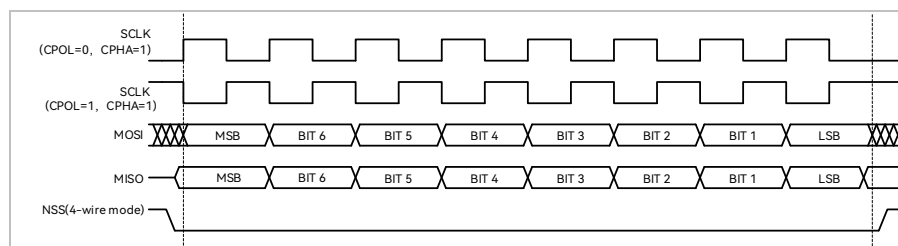


Figure 10-7 Data/Clock Line Timing Diagram (SPIx_CR[CPHA] = 1)



10.3 SPI Registers

10.3.1 SPIx_CR (CSR: 0x180/0x190) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																						SAMSEL	SCKRQ	CPHA	CPOL	NSSMOD	SLINE	SPIE	SPIMS	SPIEN	
																						rw	r0w1	rw	rw						rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:10]	RSV	Reserved
[9]	SAMSEL	SPI Master Edge Sampling Selection 0: The master samples data at the valid sampling edges. 1: The master delays sampling by half an SCLK cycle.
[8]	SCKRQ	Single-wire Master Request Slave Data Enable 0: Disable 1: Enable
[7]	CPHA	Clock Phase 0: Data is received on leading edge and transmitted on trailing edge of active SCLK. 1: Data is transmitted on leading edge and received on trailing edge of active SCLK.  Note: > 00: Data is received on the rising edge, and sent on the falling edge. Idle level is low. > 01: Data is sent on the rising edge, and received on the falling edge. Idle level is high. > 10: Data is sent on the rising edge, and received on the falling edge. Idle level is low. > 11: Data is received on the rising edge, and sent on the falling edge. Idle level is high.
[6]	CPOL	Clock Polarity in Idle State 0: Low Level 1: High Level

		 Note: > 00: Data is received on the rising edge, and sent on the falling edge. Idle level is low. > 01: Data is sent on the rising edge, and received on the falling edge. Idle level is high. > 10: Data is sent on the rising edge, and received on the falling edge. Idle level is low. > 11: Data is received on the rising edge, and sent on the falling edge. Idle level is high.
[5:4]	NSSMOD	SPI Mode Selection 00: 3-wire slave or 3-wire master mode. NSS signal is not routed to a port pin. 01: 4-wire slave or multi-master mode (default). NSS pin is configured as an input. 1x: 4-wire single-master mode. NSS pin is configured as an output and outputs the value held by NSSMOD0 bit.
[3]	SLINE	Single-wire Half-duplex Mode Enable 0: Disable 1: Enable
[2]	SPIIE	SPI Interrupt Enable 0: Disable 1: Enable
[1]	SPIMS	Master/Slave Mode Selection 0: Slave 1: Master
[0]	SPIEN	SPI Enable 0: Disable 1: Enable

10.3.2 SPIx_SR (CSR: 0x181/0x191) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																						SLVSEL	NSSIN	SRMT	RXBMT	TXBMT	SPIBSY	SPIIF	WCOL	MODF	RXOVRN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	rW0	rW0	rW0	rW0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	0	0	0	0	0

Bit	Name	Description
[31:10]	RSV	Reserved
[9]	SLVSEL	NSS Selection Flag This bit is set to “1” when the filtered signal of NSS is low, indicating that the device is selected as a slave. When NSS is high, this bit is cleared to “0”, indicating that the device is not selected as a slave. 0: The device is not selected as a slave. 1: The device is selected as a slave.
[8]	NSSIN	NSS real-time signal, unfiltered. 0: Chip selected 1: Chip not selected
[7]	SRMT	Shift Register Empty Flag (valid only in Slave Mode) 0: Data has been shifted out of the transit buffer into the shift register or SCLK changes. 1: There is no data in the shift register or transmit and receive buffers.  Note: SPIx_SR[SRMT] = 1 in Master Mode.
[6]	RXBMT	Receive Buffer Empty Flag (valid only in Slave Mode) 0: Data in the receive buffer has not been read. 1: Data has been read and there is no unread data in the receive buffer.  Note: SPIx_SR[RXBMT] = 1 in Master Mode.
[5]	TXBMT	Transmit Buffer Empty Flag This bit is cleared to “0” when the data is written to the Transit Buffer. It is set to “1” when the data in the Transit Buffer is transferred to the SPI shift register, indicating that it is safe to write a new byte to the transmit buffer. 0: The data is written to the transmit buffer. 1: The data in the transmit buffer has been transferred to the shift register.
[4]	SPIBSY	SPI Busy Flag 0: No data is transferring via SPI. 1: Data is transferring via SPI.
[3]	SPIIF	SPI Interrupt Flag This bit is set to “1” by hardware each time after a data frame (8-bit) is transferred. Read: 0: No interrupt pending

		1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	WCOL	Write Conflict Interrupt Flag When SPIx_SR[TXBMT] is “0”, a write to SPIx_DR sets this bit to “1”. This bit can be cleared to “0” by software only. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	MODF	Master Mode Fault Interrupt Flag This bit is set to “1” when a master mode conflict is detected (SPIx_SR[NSSIN] = 0, SPIx_CR[SPIMS] = 1 and SPIx_CR[NSSMOD] = 01). This bit can be cleared to “0” by software only. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	RXOVRN	Receive Overflow Interrupt Flag (Slave Mode only) This bit is set to “1” by hardware (and generates an SPIx interrupt) when the Receive Buffer still holds unread data from a previous transfer and the last bit of the current transfer has been shifted into the SPIx shift register. This bit cannot be automatically cleared to “0” by hardware, and can be cleared to “0” by software only. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

10.3.3 SPIx_CLK (CSR: 0x182/0x192) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								SPICLK							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	SPICLK	SPI Baud Rate Setting This bit is valid in master mode only, and can be written only when SPIx_CR[SPIEN] = 0. Baud rate = SPIxCLK/2/(SPICLK + 1)  Note: > When SPIx_CR[SAMSEL] is enabled: >> Maximum Transmit Baud Rate for SPI Master: SYSCLK/2 >> Maximum Receive Baud Rate for SPI Master: SYSCLK/4 >> Maximum Transmit Baud Rate for SPI Slave: SYSCLK/4 >> Maximum Receive Baud Rate for SPI Slave: SYSCLK/4 > When SPIx_CR[SAMSEL] is disabled: >> Maximum Transmit Baud Rate for SPI Master: SYSCLK/2 >> Maximum Receive Baud Rate for SPI Master: SYSCLK/6 >> Maximum Transmit Baud Rate for SPI Slave: SYSCLK/10 >> Maximum Receive Baud Rate for SPI Slave: SYSCLK/10

10.3.4 SPIx_DR (CSR: 0x183/0x193) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								SPIDR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	SPIDR	SPIx Data Register SPIx_DR Register is used to transmit and receive SPI data. Read: Read the received data of Receive Buffer Write: Write the data into Transit Buffer and initiate a transfer

11 UART

11.1 UART1 and UART2 Introduction

UART is a full-duplex or half-duplex serial data exchange interface as shown in Figure 11-1. The baud rate is configurable and supports DMA transmission. Figure 11-2 describes the UART timing.

Figure 11-1 Block Diagram of UART Module

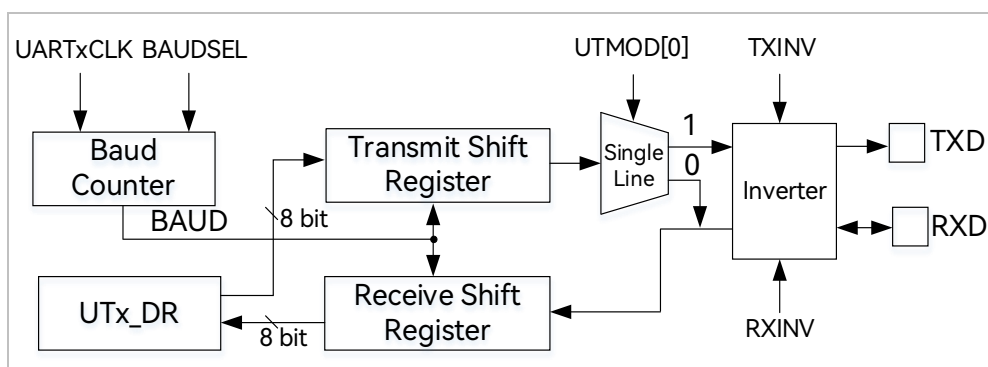
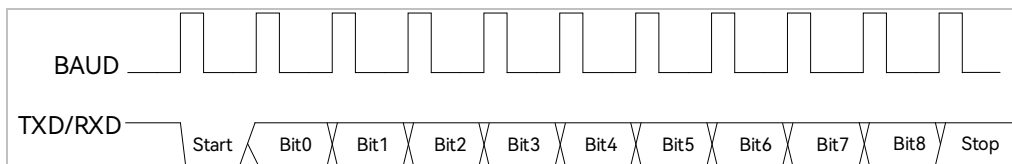


Figure 11-2 UART Timing Diagram



11.2 UART1 and UART2 Operations

11.2.1 Mode0

Mode0 works in single-wire half-duplex mode. RXD pin is configured as both an output (Transmit Data Bus) and an input (Receive Data Bus). It uses a total of 10 bits (1 start bit, 8 data bits and 1 stop bit) to receive or send data. If parity check feature is enabled, a check bit shall be added after the data bits. The baud rate is configured by UTx_BAUD[BAUD].

Sending Data: Write the data to UTx_DR and clear UTx_CR0[TI]. RXD outputs 10-bit data. UTx_CR0[TI] is set to “1” after the transmission is completed. If parity check feature is enabled, a check bit shall be added after the data bits.

Receiving Data: Set UTx_CR0[REN] to “1” to receive the data and clear UTx_CR0[UTRI]. The data is

received via RXD. After the data is received, `UTx_CR0[UTRI]` is set to “1” and `UTx_DR` is read to obtain the data. The parity check result is stored in `UTx_CR0[CHKERR]` if any.

11.2.2 Mode1

Mode1 works in full-duplex or half-duplex mode. TXD pin is configured as an output (Transmit Data Bus) and RXD as an input (Receive Data Bus). It uses a total of 10 bits (1 start bit, 8 data bits and 1 stop bit) to receive or send data. If parity check feature is enabled, a check bit shall be added after the data bits. The baud rate is configured by `UTx_BAUD[BAUD]`.

Sending Data: Write the data to `UTx_DR` and clear `UTx_CR0[UTTI]`. TXD outputs 10-bit data. `UTx_CR0[UTTI]` is set to “1” after the transmission is completed. If parity check feature is enabled, a check bit shall be added after the data bits.

Receiving Data: Set `UTx_CR0[REN]` to “1” to receive the data and clear `UTx_CR0[UTRI]`. The data is received via RXD. After the data is received, `UTx_CR0[UTRI]` is set to “1” and `UTx_DR` is read to obtain the data. The parity check result is stored in `UTx_CR0[CHKERR]` if any.

11.2.3 Mode2

Mode2 works in single-wire half-duplex mode. RXD pin is configured as both an output (Transmit Data Bus) and an input (Receive Data Bus). It uses a total of 11 bits (1 start bit, 9 data bits and 1 stop bit) to receive or send data. If parity check feature is enabled, the 9th data bit acts as the check bit. The baud rate is configured by `UTx_BAUD[BAUD]`.

Sending Data: Write the first 8 bits of the data to `UTx_DR` and the 9th bit to `UTx_CR1[CHKMOD]`, and clear `UTx_CR0[UTTI]`. TXD outputs 11-bit data. `UTx_CR0[UTTI]` is set to “1” after the transmission is completed.

Receiving Data: Set `UTx_CR0[UTREN]` to “1” to receive the data and clear `UTx_CR0[UTRI]`. The data is received via RXD. After the data is received, `UTx_CR0[UTRI]` is set to “1”. `UTx_CR0[UTRB8]` stores the 9th bit of the data, and `UTx_DR` stores the first 8 bits. The parity check result is stored in `UTx_CR0[CHKERR]` if any.

11.2.4 Mode3

Mode3 works in full-duplex or half-duplex mode. TXD pin is configured as an output (Transmit Data Bus)

and RXD as an input (Receive Data Bus). It uses a total of 11 bits (1 start bit, 9 data bits and 1 stop bit) to receive or send data. If parity check feature is enabled, the 9th data bit acts as the check bit. The baud rate is configured by UTx_BAUD[BAUD].

Sending Data: Write the first 8 bits of the data to UTx_DR and the 9th bit to UTx_CR1[CHKMOD], and clear UTx_CR0[UTTI]. TXD outputs 11-bit data. UTx_CR0[UTTI] is set to “1” after the transmission is completed.

Receiving Data: Set UTx_CR0[UTREN] to “1” to receive the data and clear UTx_CR0[UTRI]. The data is received via RXD. After the data is received, UTx_CR0[UTRI] is set to “1”. UTx_CR0[UTRB8] stores the 9th bit of the data, and UTx_DR stores the first 8 bits. The parity check result is stored in UTx_CR0[CHKERR] if any.

11.3 UART1 and UART2 Interrupt Sources

UART interrupt sources include:

- UTx_CR0[UTTI]: After the data is sent via UARTx, UTx_CR0[UTTI] is set to “1” by hardware.
- UTx_CR0[UTRI]: After the data and STOP are received via UARTx, UTx_CR0[UTRI] is set to “1” by hardware.
- UTx_CR0[RTO]: If the data is not received via UARTx within a certain amount of time, the interrupt flag bit UTx_CR0[RTO] is generated.

11.4 UART Registers

11.4.1 UTx_CR0 (CSR: 0x0140/0x150) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																						RTO	CHKERR	UTRB8	UTMOD		UTSM2	UTREN	UTEN	UTTI	UTRI
																						rw0	r	rw	rw	rw	rw	rw	rw	rw	rw
																						0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:10]	RSV	Reserved

[9]	RTO	Receiving Data Timeout Interrupt Flag Read: 0: No timeout occurs in receive operations. 1: A timeout occurs in receive operations. Write: 0: This bit is cleared to “0” 1: An interrupt event is generated.
[8]	CHKERR	Parity Error 0: No parity error is detected. 1: Parity error is detected.
[7]	UTRB8	Bit9 of the Received Data in Mode2 and Mode3
[6:5]	UTMOD	Mode Selection 00: Mode0 01: Mode1 10: Mode2 11: Mode3
[4]	UTSM2	Communication Mode Selection 0: Single-device Communication 1: Multi-device Communication
[3]	UTREN	UARTx Receive Enable 0: Disable 1: Enable
[2]	UTEN	UARTx Enable 0: Disable 1: Enable
[1]	UTTI	Data Transmitting Completed Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: An interrupt event is generated.
[0]	UTRI	Data Receiving Completed Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write:

		0: This bit is cleared to “0” 1: An interrupt event is generated.

11.4.2 UTx_CR1 (CSR: 0x0141/0x151) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																					RTOIE	UTIE	BAUDSEL	RXINV	TXINV	RSV		RTOSEL		CHKMOD	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	-	-	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	-	0	0	0	0

Bit	Name	Description
[31:11]	RSV	Reserved
[10]	RTOIE	Receiving Data Timeout Interrupt Enable 0: Disable 1: Enable
[9]	UTIE	Data Receiving and Sending Interrupt Enable 0: Disable 1: Enable
[8]	BAUDSEL	Frequency Multiplier Enable 0: Disable 1: Enable
[7]	RXINV	Transmit Polarity Inversion Enable 0: Disable 1: Enable
[6]	TXINV	Receive Polarity Inversion Enable 0: Disable 1: Enable
[5:4]	RSV	Reserved
[3:2]	RTOSEL	Receiving Data Timeout Selection 00: One frame of the data 01: Two frames of the data 10: Four frames of the data 11: Eight frames of the data
[1:0]	CHKMOD	Manually Sent Bit9 and Parity Bit 00: Manual Mode TB9=0 01: Even parity

10: Odd parity
11: Manual Mode TB9=1

11.4.3 UTx_DR (CSR: 0x0142/0x152) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								UTx_DR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	UTx_DR	Send/Receive Data Read: Data received Write: Data to be sent  Note: The UARTx data buffer consists of two independent buffers, i.e., a receive buffer and a transmit buffer, which can send and receive data at the same time. The transmit buffer can be written only but not read, while the receive buffer can be read only but not written. Both buffers share a same address.

11.4.4 UTx_BAUD (CSR: 0x0143/0x153) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																BAUD																
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	BAUD	Baud Rate Setting Baud rate = $\text{UARTxCLK} / (16 / (1 + \text{UTx\_CR1}[\text{BAUDSEL}])) / (\text{UTx\_BAUD}[\text{BAUD}] + 1)$ For example, UARTxCLK = 24M, baud rate = 9600, UTx_CR1[BAUDSEL] = 0, then UTx_BAUD[BAUD] = $(24\text{M} / 16 / 9600 / (1 + 0)) - 1 = 155$ (0x9B)

11.5 Serial Frame Communication Registers

Please contact us for more details on serial frame (S-format) communication.

11.5.1 SF_CR (0x144)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										rw	w1	rw	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit	Name	Description
[31:3]	RSV	Reserved
[2]	AUTO_EN	Serial Encoder Decoding Auto Enable 0: Disable 1: Enable
[1]	SEND_REQ	Serial Encoder Decoding Request 0: Disable 1: Enable
[0]	SF_EN	Serial Encoder Decoding Enable 0: Disable 1: Enable

11.5.2 SF_SR (0x145)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										rw0	rw0	rw0	rw0	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit	Name	Description
[31:6]	RSV	Reserved

[5]	SF_SUC	Data Receiving Succeeded Flag. The data is received successfully and it passes CRC verification. Read: 0: Data fails to be received. 1: Data is received successfully. Write: 0: This bit is cleared to “0” 1: No effect
[4]	SF_DONE	Data Receiving Completed Flag. The data is received but it may contain an error (e.g.: This flag appears if CRC verification fails) 0: Data is being received. 1: Data is received. Write: 0: This bit is cleared to “0” 1: No effect
[3]	REQ_OUT	Request Timeout Error. The request command cannot be returned. Read: 0: No request timeout error occurs 1: A request timeout error occurs Write: 0: This bit is cleared to “0” 1: No effect
[2]	REQ_ERR	Request Command Error. The sent and returned IDs are different. Read: 0: No request command error occurs 1: A request command error occurs Write: 0: This bit is cleared to “0” 1: No effect
[1]	SYN_ERR	Frame Synchronization Error. For example, Sink Code of the control field (CF) is not detected. Read: 0: No frame synchronization error occurs 1: A frame synchronization error occurs Write: 0: This bit is cleared to “0” 1: No effect

[0]	CRC_ERR	CRC Error Read: 0: No CRC error occurs 1: A CRC error occurs Write: 0: This bit is cleared to “0” 1: No effect

11.5.3 SF_BAUD (0x146)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																												SF_BAUD				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0	0	1	1

Bit	Name	Description
[31:5]	RSV	Reserved
[4:0]	SF_BAUD	Baud Rate for Serial Frame (S-format) Communication Baud rate = SFCLK /(SF_BAUD + 1)

12 BISS

12.1 BISS Introduction

BISS (Bidirectional Synchronous Serial Interface) was introduced by IC-HAUS as an open-source protocol for sensors and actuators. The most current version of BISS protocol is BISS-C. For more information about BISS-C, please visit <https://www.ichauschina.com/biss.htm>.

BISS is a bus protocol that provides fast, synchronous, full-duplex communications between sensors and actuators. It is hardware compatible to the industrial standard SSI (Serial Synchronous Interface), and mainly used in position control applications, such as the communication between servo driver and encoder.

Figure 12-1 Timing Diagram of BISS

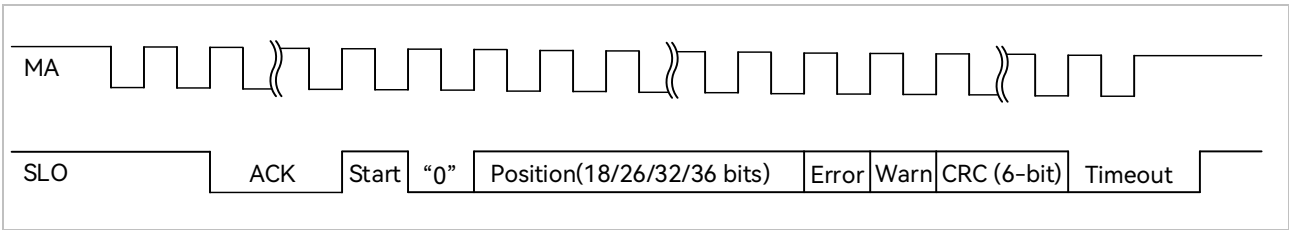


Table 12-1 BISS Master Specifications

Item	Description
Number of Slave	One by default. Multiple slaves are supported, but the total data length cannot exceed 64 bits
Protocol	BISS-C CRC calculation with 0x00 as initial value and 0x43 as polynomial The register cannot be read and written.
Connection	Point-to-point connection only
Clock Rate	BISSCLK/(N+1), N = 0, 1, 2, 3, ..., 65535
Line Delay Compensation	Available
Interrupt Source	An interrupt is generated when the communication is completed.
Error Detection	Warning Bit (Warn) Error Error Bit (Error) Error CRC Error Communication Timeout Error

12.2 BISS Registers

12.2.1 BISS_CLK_CNT (CSR: 0x701)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																BISS_CLK_CNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	BISS_CLK_CNT	Count Value for Calculation of Clock Rate on MA Line. If the clock runs at 24MHz and this register is set as “N”, then $BISS\_MA = BISSCLK/2/(N + 1)$

12.2.2 BISS_OVERTIME_CNT (CSR: 0x702)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																BISS_OVERTIME_CNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	BISS_OVERTIME_CNT	This bit is used to set the BISS timeout interrupt. The counter starts after BISSBUSY is pulled high. The counting is based on MA line. If this register is “N” and BISS communication is not completed after $N * MA\_clk$, an overtime interrupt is generated and the flag bits BISSOTIF and BISSENDIF are pulled high. It is recommended to set $N = BISS\_DATA\_LEN + 10 + (\text{Safety Margin})$

12.2.3 BISS_DATA_LEN (CSR: 0x703)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
RSV		BISS_DATA_LEN																													
-	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	
-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31]	RSV	Reserved
[30:0]	BISS_DATA_LEN	BISS data frame (Position) length + error bits (Error and Warn) length (2 bits)

12.2.4 BISS_STATE (CSR: 0x704)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0													
																							RSV														BISSAUTOEN	BISSWRNERR	BISSALMERR	BISSCRCERR	BISSOTIF	BISENDIF	BISSDEN	BISSBUSY
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	r	r	r	rw0	rw0	rw	rw1													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0													

Bit	Name	Description
[31:9]	RSV	Reserved
[8]	BISSAUTOEN	BISS Auto Decode Enable 0: Disable 1: Enable
[7]	BISEN	BISS Enable (by software)
[6]	BISSWRNERR	BISS warning bit (Warn) is the inverted state, where “1” indicates a warning occurs. (Read Only)
[5]	BISSALMERR	BISS error bit (Error) is the inverted state, where “1” indicates an error occurs. (Read Only)
[4]	BISSCRCERR	BISS CRC Error Flag (Read Only)

[3]	BISSOTIF	BISS Communication Timeout Flag This bit is cleared to “0” by software, and set to “1” by hardware.
[2]	BISENDIF	BISS Communication Completed Flag This bit is cleared to “0” by software, and set to “1” by hardware.
[1]	BISENDEN	BISS Transmission Completed Interrupt Enable The BISENDIF flag bit is pulled high when BISS communication is completed. In this case, a BISEND interrupt is generated. This bit is configured via software.
[0]	BISSBUSY	This bit is always high during BISS transmission. BISS transmission starts after “1” is written by software (all configurations shall be completed before this operation). After BISS transmission (timeout or completed), it is automatically cleared to “0” by hardware.

12.2.5 BISS_SDATAL (CSR: 0x705)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BISS_SDATAL																															
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	Name		Description																												
[31:0]	BISS_SDATAL		Low-order 32 bits of the input data received by BISS interface from the slave. BISS_SDATAL includes BISS data frame (Position) + error bits (Error and Warn)																												

12.2.6 BISS_SDATAH (CSR: 0x706)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BISS_SDATAH																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	BISS_SDATAH	High-order 32 bits of the input data received by BISS interface from the slave

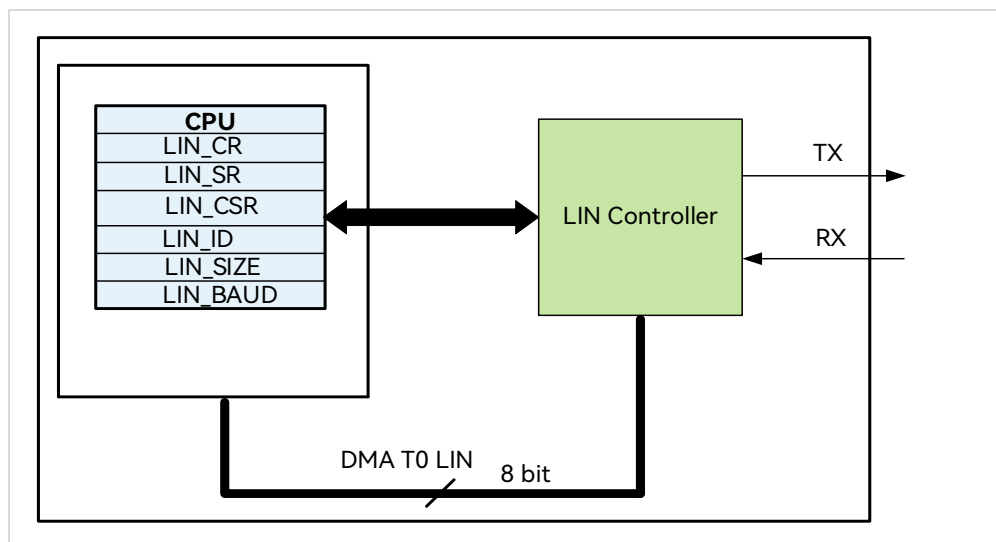
13 LIN

13.1 LIN Introduction

LIN is an asynchronous and serial communication interface mainly used in automotive network. LIN controller complies with ISO 17987 (backward compatible). As shown in Figure 13-1, the controller implements a complete LIN hardware interface, which works in slave mode and supports baud rate adaption. PA0/PA1 and PA4/PA5 (function switching) are translated into LIN pins, and data transmission between LIN and DMA is possible by setting DMAx_CR[DMACFG] = 0111. The R/W direction is determined by LIN_CR[LINRW].

For more information regarding LIN protocol, see LIN Consortium (<http://www.lin-subbus.org>).

Figure 13-1 Block Diagram of LIN Module



The LIN controller has three main components, as shown in Figure 13-1:

- > LIN access register: Provide the interface between the CPU and the LIN controller
- > LIN data buffer: Transmit and receive the data by configuring DMAx (x = 0~5)
- > LIN control register: Process data transmission and control states of the LIN bus

13.2 LIN Slave Mode Operations

When LIN is configured for slave mode operation, it must wait for a command from a master node.

When LIN Interrupt is enabled, an interrupt is generated in any of the following seven cases as shown in Table 13-1.

Table 13-1 LIN Interrupt Sources and Descriptions

Interrupt Source	Description	Interrupt Flag	Clear Flag
Bus Idle	Bus remains idle for 4s or more	LIN_SR[LINIDLE]	Write “0” to LIN_SR[LINIDLE]
External Wakeup	Wake signal is received	LIN_CSR[LINWAKEUP]	Write “0” to LIN_CSR[LINWAKEUP]
Reception of Break Field	Rising edge of the break field is detected.	LIN_SR[BREAKFLAG]	Write “0” LIN_SR[BREAKFLAG]
Sync Completed	Sync field is received successfully without errors	LIN_SR[SYSCFLAG]	Write “0” LIN_SR[SYSCFLAG]
Reception of Frame Header	Frame header is received and the ID is successfully verified.	LIN_SR[LINREQ]	Write “1” to LIN_SR[LINACK]/ Write “0” to LIN_SR[LINREQ]/ A new frame header is detected
Data Transmission or Reception Completed	Data is received or sent by the slave.	LIN_SR[LINDONE]	Write “0” to LIN_SR[LINDONE]/ A new frame header is detected
Errors	Frame error/ Bit error/ Sync error/ ID check error/ Data check error	LIN_SR[ERRFRAME] LIN_SR[ERRBIT] LIN_SR[ERRSYNC] LIN_SR[ERRPRTY] LIN_SR[ERRCHK]	Write “0” to LIN_SR[LINERR]/ A new frame header is detected

LIN slave transmits and receives the data as follows:

1. Before LIN controller works, its baud rate mode shall be selected and the associated baud rate register shall be properly configured as well. See section 13.5 for details.
2. LIN controller detects the header (break field and sync field signals) of a message frame from the master on LIN bus. LIN_SR[BREAKFLAG] is set to “1” if the sync field meets the minimum length requirement. The baud rate of the data is automatically identified by the synchronization signal, and LIN_SR[SYSCFLAG] is set to “1” upon successful synchronization. LIN_SR[LINREQ] is set to “1” when the slave recognizes the ID and the ID checksum is correct. Otherwise, LIN_SR[ERRPRTY] is set to “1” and ID checksum error occurs;
3. Sending Data: Set LIN_CR[LINRW] to “1” to load the data length into LIN_SIZE and data bytes

into DMA buffer. Set LIN_CSR[LINACK] to “1” and frame header transfers data to the master;

4. Receiving Data: Clear LIN_CR[LINRW] to “0” and set LIN_CSR[LINACK] to “1”, and frame header receives the data sent by the master;
5. LIN_SR[LINDONE] is set to “1” after the slave receives or sends the data.

13.3 Sleep and Wakeup

LIN Protocol Specification defines a sleep mode to reduce the system’s power consumption.

After the slave receives and correctly decodes a sleep mode request from the master, the software sets LIN_CSR[LINSLP] to “1” to initiate the sleep mode.

LIN_SR[IDLE] is set to “1” when the bus stays idle for more than 4s and the LIN slave is not in the sleep mode.

When a wake-up signal from the master or any slave node (setting LIN_SR[LINWAKEUP] to “1”) is detected, LIN slave automatically exits the sleep mode. The LIN slave can also send a wake-up signal (setting LIN_CSR[TXWAKEUP] to “1”) to wake up the master or other slaves.

13.4 Error Detection and Process

When LIN slave detects an error, LIN_SR[LINERR] is set to “1”, and LIN generates an error interrupt request and stops the processing of current frame. The type of error, i.e., frame error, bit error, sync error, data check error or ID check error, is determined via LIN_SR[ERRFRAME], LIN_SR[ERRBIT], LIN_SR[ERRSYNC], LIN_SR[ERRCHK] and LIN_SR[ERRPTY] respectively. LIN_SR[LINERR] is cleared to “0” after the error is removed.

13.5 Baud Rate Modes

LIN module supports automatic baud rate mode and fixed baud rate mode.

Automatic Baud Rate Mode: LIN module detects LIN bus at a frequency of 20k and enters data receiving or sending mode if a break field greater than 12 bit is detected. When the byte "0x55" is identified in the sync field, LIN module calculates baud rate of LIN message based on the field length. If the sync field

waveform fails to meet the requirement, a synchronization error is generated (this error detection is enabled by default, and can be disabled by setting `LIN_CR[AB_SCHKERRDIS] = 1`). After successful synchronization, LIN module sends or receives the next LIN message based on the synchronized baud rate. The break field length can be determined by `LIN_BRKCNT` and the baud rate detected by the LIN module.

Fixed Baud Rate Mode: LIN module operates in fixed baud rate mode after `LIN_CR[MBAUD]` is set to “1”. The baud rate (1000–20000) is configured through `LIN_BAUD` register, and the received baud rate is generally $\pm 10\%$ of the configured value. LIN module receives LIN message according to the configured baud rate. If LIN message is carried with unmatched baud rate, sync error occurs and LIN module refuses receiving the LIN message.

13.6 Other Matters

When LIN slave mode is enabled and the device is not in sleep mode, the slave can detect a new frame header (including Synch Break Field, Synch Field and PID). When the LIN bus is idle, `LIN_IDLECNT` starts counting with a clock rate of 32.768kHz. The inter-frame space can be obtained from the register `LIN_IDLECNT`. The counter resets to “0” upon transmission or reception of a LIN message.

Configuring `LIN_CSR[LINSTOP]` to “1” aborts the processing of the current frame during data transmission at slave mode. In this case, the flag bit `LIN_SR[ABORT]` is set to “1”.

13.7 LIN Transceiver (FU7564Q1/FU7565Q1/FU7574Q1)

The chip integrates a Local Interconnect Network (LIN) physical layer transceiver, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V), and SAE J2602 standards. It is primarily intended for automotive networks operating at data rates from 1 kbps to 20 kbps.

Key features include:

- Compliance with LIN 2.x, ISO 17987-4:2016 (12V), and SAE J2602 standards
- LIN wake-up
- LIN data rate up to 20kbps

- LIN pin withstand voltage with respect to ground: -40V~40V

The chip controls the LIN bus state via the LIN transceiver, which converts the transmit data stream from the protocol controller into bus signals with optimized slew rate and waveform shaping to minimize electromagnetic emissions (EME). The LIN bus output pin features an internal pull-up resistor. The transceiver also receives data streams from the bus through the LIN pin and transfers them to the internal control module.

Functional modes of the LIN transceiver:

- Normal Mode

In normal mode, data can be transmitted and received over the LIN bus. A high bus level indicates recessive state, while a low level indicates dominant state. Upon detecting data on the LIN bus, the transceiver forwards it to the internal control module; the module can also send data to the bus.

- Sleep Mode and Wake-up

» FU7564Q1/FU7565Q1: After the chip enters sleep mode, the LIN transceiver maintains low-power operation. If a low-level signal longer than 80 μ s is detected on the LIN bus, the chip will be woken up. Upon wake-up, the chip resets and the LIN transceiver resumes normal data reception and transmission.

» FU7574Q1: After the chip enters sleep mode, the LIN transceiver maintains low-power operation. If a low-level signal longer than 80 μ s is detected on the LIN bus and the MON_HV2 input level changes, the chip will be woken up. Upon wake-up, the chip resets and the LIN transceiver resumes normal data reception and transmission.

13.8 LIN Registers

13.8.1 LIN_CR (CSR: 0x1A0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				rw	rw	rw	w1	rw	RSV			rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AB_BKLEN_RPTDIS	AB_SCHKERRDIS	AB_ERRINTEN	AUTOAUDINIT	MBAUD	-	-	-	LINIE	CHKMOD	LINRW	AUTOSIZE

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	-	-	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11]	AB_BKLEN_RPTDIS	Break Field Length Recording Disable in LIN Auto Baud Rate Mode 0: Disable 1: Enable
[10]	AB_SCHKERRDIS	Sync Field Error Detection Disable in LIN Auto Baud Rate Mode In automatic baud rate mode, LIN module verifies if the sync field waveform meets the requirement. If not, a synchronization error occurs. 0: Disable 1: Enable
[9]	AB_ERRINTEN	Error Initialization Enable in LIN Auto Baud Rate Mode In automatic baud rate mode, if LIN module detects an error, it restarts monitoring LIN messages at 20kHz. 0: Disable 1: Enable
[8]	AUTOBAUDINIT	LIN Auto Baud Rate Initialization In automatic baud rate mode, when this bit is set to “1”, LIN module restarts monitoring LIN messages at 20kHz. 0: No effect 1: LIN automatic baud rate initialization is triggered
[7]	MBAUD	Fixed Baud Rate Mode Selection 0: Automatic Baud Rate Mode 1: Fixed Baud Rate Mode
[6:4]	RSV	Reserved
[3]	LINIE	LIN Interrupt Enable 0: Disable 1: Enable  Note: See Table 13-1 for the LIN interrupt flag bits.
[2]	CHKMOD	Checksum Selection 0: Enhanced checksum 1: Classic checksum
[1]	LINRW	Send/Receive Selection 0: Current frame is a receive operation 1: Current frame is a send operation
[0]	AUTOSIZE	Data Length Enable Dependent on ID Bit (LIN_ID[5:4])

		0: Disable 1: Enable Mapping between LIN_ID[5:4] and Data Length: 0X: 2 bytes 10: 4 bytes 11: 8 bytes

13.8.2 LIN_SR (CSR: 0x1A1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		SYSCFLAG	BREAKFLAG	ERRFRAME	ERRBIT	ERRSYNC	ERRCHK	ERRPTY	ABORT	LINACT	LINERR	LINWAKEUP	LINIDLE	LINDONE	LINREQ
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0	rw0	r	r	r	r	r	r	r	rw0	rw0	rw0	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13]	SYSCFLAG	LIN Sync Completed Flag Read: 0: LIN sync is in progress or not performed 1: LIN sync is completed Write: 0: This flag is cleared 1: No effect
[12]	BREAKFLAG	LIN Break Field Detection Flag Read: 0: No break field is detected 1: Break field is detected Write: 0: This flag is cleared 1: No effect
[11]	ERRFRAME	Frame Error This bit is set to “1” when LIN read-back feature is enabled (by setting LIN_CSR[RDBAKDIS]) and the logic level of LIN TXD pin is different from LIN bus level. 0: No frame error occurs

		1: A frame error occurs
[10]	ERRBIT	Read-back Bit Error This bit is set to “1” when LIN read-back feature is enabled (by setting LIN_CSR[RDBAKDIS]) and the logic level of LIN TXD pin is different from LIN bus level. 0: No bit error occurs 1: A bit error occurs
[9]	ERRSYNC	Sync Error (synchronization timeout or synchronization overhead). This bit is cleared to “0” by hardware when a new frame arrives or when LIN_SR[LINERR] is cleared to “0”. 0: No sync error occurs 1: A sync error occurs
[8]	ERRCHK	Data Check Error This bit is cleared to “0” by hardware when a new frame arrives or when LIN_SR[LINERR] is cleared to “0”. 0: No data check error occurs 1: A data check error occurs
[7]	ERRPRTY	ID Check Error This bit is cleared to “0” by hardware when a new frame arrives or when LIN_SR[LINERR] is cleared to “0”. 0: No ID check error occurs 1: An ID check error occurs
[6]	ABORT	Transmission Completed Interrupt Flag This bit is set to “1” after the slave receives or sends the data, and cleared to “0” when a new frame arrives or “0” is written to LIN_SR[LINDONE] by software. Read: 0: No interrupt pending 1: Interrupt pending
[5]	LINACT	LIN Bus Active Flag 0: No data is transmitting on LIN bus 1: Data is transmitting on LIN bus
[4]	LINERR	LIN Error Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared

		1: No effect
[3]	LINWAKEUP	LIN Bus Wakeup Interrupt Flag This bit is set to “1” when the bus line stays idle for more than 4s. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[2]	LINIDLE	LIN Bus Idle Interrupt Flag This bit is set to “1” when the bus line stays idle for more than 4s. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	LINDONE	Transmission Completed Interrupt Flag This bit is set to “1” after the slave receives or sends the data, and cleared to “0” when a new frame arrives or “0” is written to LIN_SR[LINDONE] by software. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	LINREQ	Header Reception Interrupt Flag This bit is set to “1” after a frame header is received and its ID is correct. This bit is cleared to “0” when a new frame arrives, or “1” is written to LIN_CSR[LINACK] by software or “0” to LIN_SR[LINREQ]. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

13.8.3 LIN_CSR (CSR: 0x1A2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																										RDBAKDIS	LINSLP	RSV	TXWAKEUP	LINACK	LINSTOP	LINEN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	-	w1	w1	w1	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	

Bit	Name	Description
[31:7]	RSV	Reserved
[6]	RDBAKDIS	LIN Read-back Enable 1: Enable 1: Disable
[5]	LINSLP	LIN Sleep Mode Enable Read: 0: LIN is active 1: LIN is in sleep mode Write: 0: LIN exits sleep mode 1: LIN enters sleep mode
[4]	RSV	Reserved
[3]	TXWAKEUP	LIN Wake-up Write: 0: No effect 1: A wake-up signal is sent
[2]	LINACK	This bit is used to send an ACK for the frame header. The checksum, R/W mode, data content and length must be configured before this bit is set to "1". 0: No effect 1: An ACK for the frame header is sent.
[1]	LINSTOP	After this bit is set to "1", LIN stops sending or receiving the data and waits for a new frame header. LIN_SR[ABORT] is set to "1" as well. 0: No effect 1: Stop processing the current frame and wait for a new frame header
[0]	LINEN	LIN Enable 0: Disable 1: Enable

13.8.4 LIN_ID (CSR: 0x1A3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										LIN_ID					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5:0]	LIN_ID	ID received by LIN

13.8.5 LIN_SIZE (CSR: 0x1A4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												LIN_SIZE			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0

Bit	Name	Description
[31:4]	RSV	Reserved
[3:0]	LIN_SIZE	Frame length of the data received/sent

13.8.6 LIN_BAUD (CSR: 0x1A5)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																LIN_BAUD															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	1	0	0	1	0	1	0	1	1	1	1	1

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	LIN_BAUD	Baud Rate Setting Baud rate = LINCLK/(LIN_BAUD + 1)

13.8.7 LIN_IDLECNT (CSR: 0x1A6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																LIN_IDLECNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:17]	RSV	Reserved
[16:0]	LIN_IDLECNT	LIN Idle Counter Instantaneous value during counting. Timing duration = LIN_IDLECNT / 32768Hz

13.8.8 LIN_BRKCNT (CSR: 0x1A7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												LIN_BRKCNT																			
-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:20]	RSV	Reserved
[19:0]	LIN_BRKCNT	LIN Break Field Counter Timing duration = LIN_BRKCNT / LINCLK

14 CAN

14.1 CAN Introduction

CAN, also known as Controller Area Network, implements as an ISO standard-compliant serial communication protocol, supporting safe, convenient and reliable data communication for automotive networks.

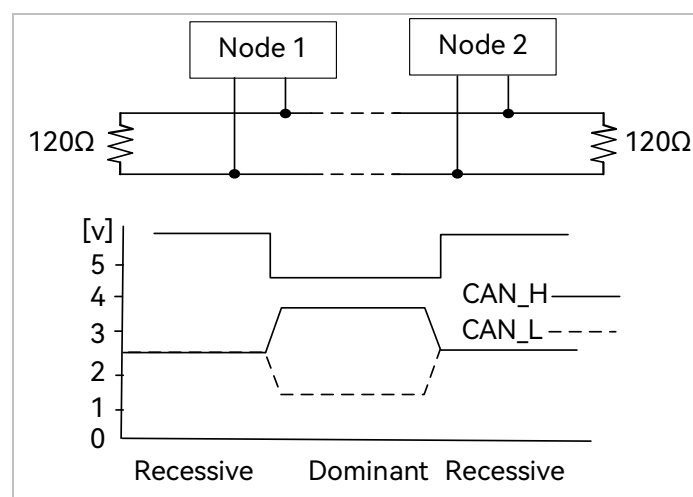
As a CAN interface, the CAN controller implements CAN 2.0A, CAN 2.0B, ISO11898-1:2015, as well as the high-performance BOSCH CAN FD protocols. It supports acceptance filtering in single filter and double filter modes to filter and receive the required messages. The CAN module includes three transmit mailboxes with a configurable transmit priority (by the transmission scheduler), and a FIFO buffer (FIFO depth: 3) that is completely controlled by hardware. Also, the CAN controller supports time-triggered communication feature.

14.2 Physical Layer Characteristics

CAN controller reads the bus level according to voltage difference between the two bus conductors CAN_H and CAN_L. The bus voltage is either recessive or dominant. The transmitter sends messages to the receiver by changing the bus voltage.

The figure below gives ISO11898-compliant physical layer characteristics of CAN.

Figure 14-1 ISO11898-compliant Physical Layer Characteristics



The above characteristics show that the dominant bus level corresponds to logic 0, with 2.5V voltage difference between CAN_H and CAN_L. The recessive bus level corresponds to logic 1, with 0V voltage difference between CAN_H and CAN_L. The dominant level has bus access priority, meaning that when any node sends a dominant bit, the result is dominant. The recessive level is somewhat inclusive so that the result is recessive only when all nodes send a recessive bit. In addition, an 120Ω termination resistor is mounted onto both start and stop points of CAN bus for impedance matching with an effort to minimize echoed or reflected signals.

14.3 Frame Structure

CAN Protocol is implemented with the following five types of frames:

- > Data Frame
- > Remote Frame
- > Error Frame
- > Overload Frame
- > Interframe Space

Data frame and remote frame support two frame formats known as Standard Frame and Extended Frame, which contain an 11-bit identifier and 29-bit identifier respectively.

Table 14-1 CAN Protocol-supported Frame Types and Their Functions

Type	Function
Data Frame	It transfers a frame from the transmitter to the receiver.
Remote Frame	The receiver requests a transmission from the transmitter with same ID. CAN FD does not support remote frames.
Error Frame	It broadcasts an error to all other nodes when a node detects a fault.
Overload Frame	The receiver sends the frame to notify that it is busy.
Interframe Space	It separates data frame and remote frame from the preceding frame.

The following section provides a detailed introduction of data frame (other frames are omitted for the sake of brevity). Date frame typically comprises seven parts, including:

- > Start of Frame (SOF): It signifies the start of a frame.
- > Arbitration Field: It determined the priority of the current frame.

- Control Field: It signifies the bytes and reserved bit of a frame.
- Data Field: It contains 0 ~ 64 bytes of data.
- CRC Field: It detect errors.
- ACK Field: It signifies that a node has received the frame correctly.
- End of Frame (EOF): It signifies the end of a frame.

Refer to ISO-11898-1: 2015(E) for more details. The figure below presents the structure of data frame.

Figure 14-2 Structure of CAN Standard Frame

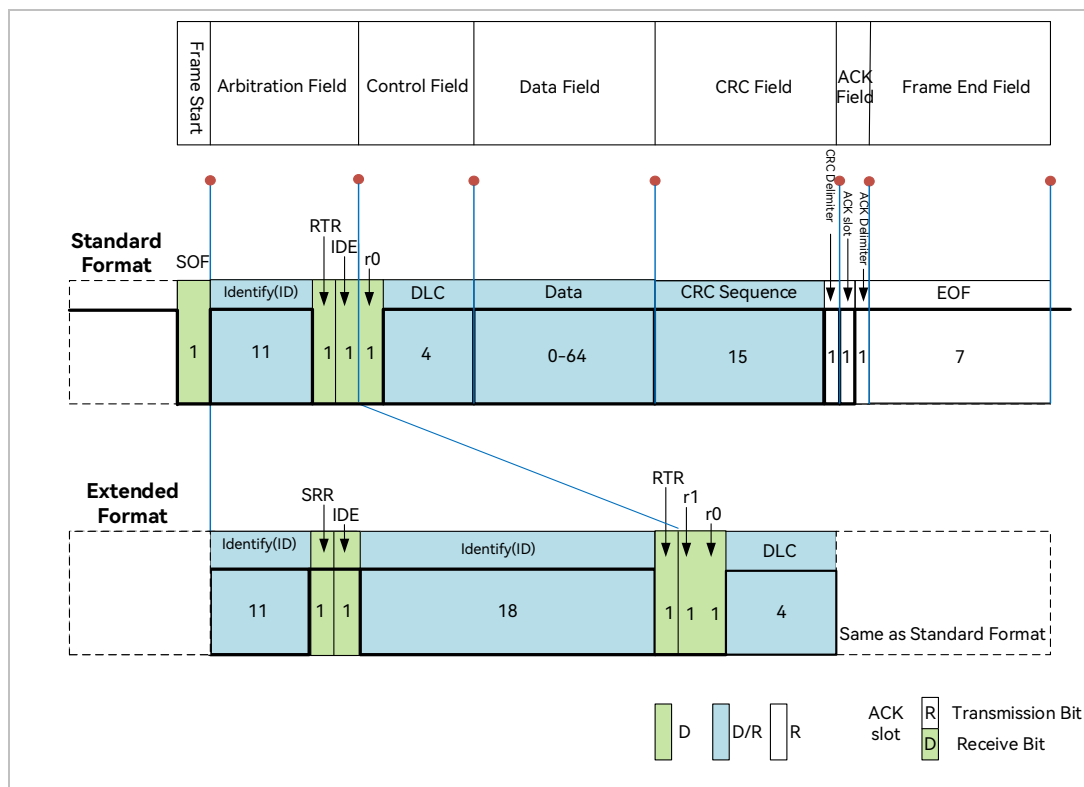
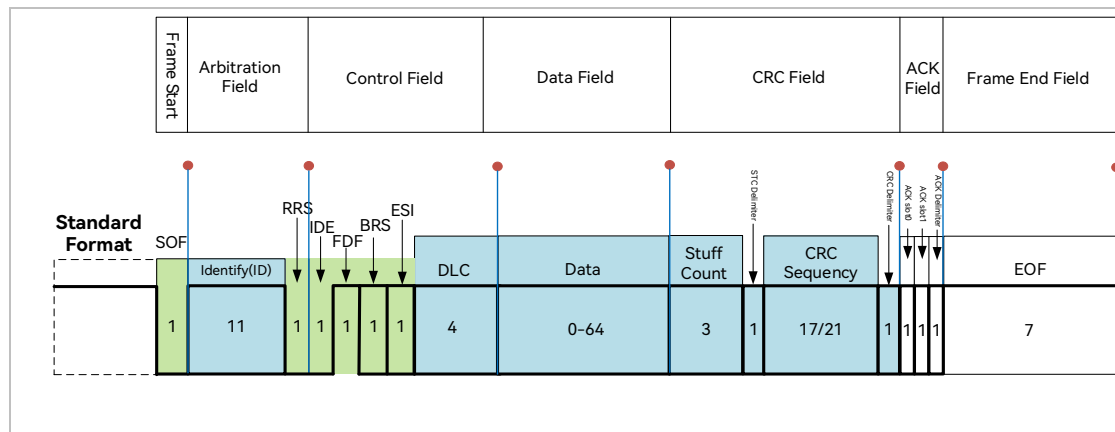


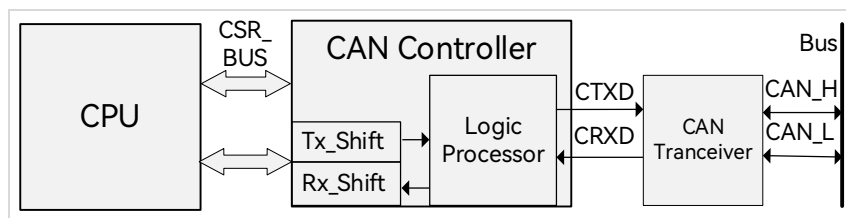
Figure 14-3 Structure of CAN FD Frame



14.4 General Descriptions on CAN Controller

The figure below presents topological structure of the CAN bus. CPU configures the CAN controller registers via CSR addressing, including initialization, bit time, operating mode, acceptance filtering and interrupt, and it completes communication between CAN module and Message SRAM so as to receive or transmit messages. The message SRAM consists of three Transit Buffers and three Receive Buffers.

Figure 14-4 Topological Block Diagram of CAN Bus



14.5 Key Features

- > Support CAN 2.0A and CAN 2.0B
- > Support CAN FD frame (ISO11898-1 and CAN FD protocol V1.0)
- > General-purpose frames up to 1Mbit/s
- > CAN FD frame up to 4Mbit/s
- > Support transmission delay compensation
- > Support time-triggered communication feature
- > CAN interrupt enable and clear
- > Three transmit mailboxes

- Configurable transmit priority
- Support Automatic Retransmission Disable mode
- A FIFO buffer (FIFO depth: 3), where CPU reads the received messages using FIFO pointer `CAN_TSPT[RDPTR]`
- Sleep mode with low-power consumption, supporting auto wakeup and manual wakeup
- Error processing

14.6 Operating Modes

14.6.1 Reset Mode

In Reset Mode, CAN controller is in reset status and cannot receive or send messages from or to CAN bus. The CAN controller enters the Reset Mode after CAN_CR0[RSTMOD] is set to “1”.

14.6.2 Normal Operation Mode

Before CAN controller enters the normal operation mode, it is necessary to configure parameters for bit time characteristics (including CAN_DBTR and CAN_NBTR) and acceptance filtering (including CAN_CR0[FILMOD], CAN_ACR and CAN_AMR) and program CAN_CR0[CANEN] = 1 to enable CTXD and CRXD pins and initialize CAN. After initialization, the CAN controller starts to synchronize itself to the CAN bus. Synchronization is implemented after CRXD detects a sequence of 11 consecutive recessive bits (= Bus Idle). After synchronization, CAN controller enters normal operation mode and can receive or send messages from or to CAN bus.

14.6.3 Sleep Mode

CAN controller can operate in the power-efficient sleep mode. Programming CAN_CR1[SLPREQ] to “1” sends a sleep mode request. CAN controller enters the sleep mode only when there is no activity on the bus. It acknowledges the sleep mode by reading CAN_STS[SLPACK] bit. In this mode, CAN stops receive or send messages but the receive buffer is accessible by software.

CAN provides two wake-up modes:

- Manual Wakeup by Software: Clearing CAN_CR1[SLPREQ] to “0” enables this feature.
- Auto Wakeup by Hardware: Setting CAN_CR0[AWU] to “1” enables this feature. When any activity is detected on the bus, CAN_CR1[SLPREQ] bit is cleared to “0” by hardware to wake up CAN controller. CAN controller re-synchronizes itself with CAN bus before exiting the sleep mode. Reading CAN_STS[SLPACK] bit acknowledges that CAN bus exits the sleep mode.

14.7 Feature Descriptions

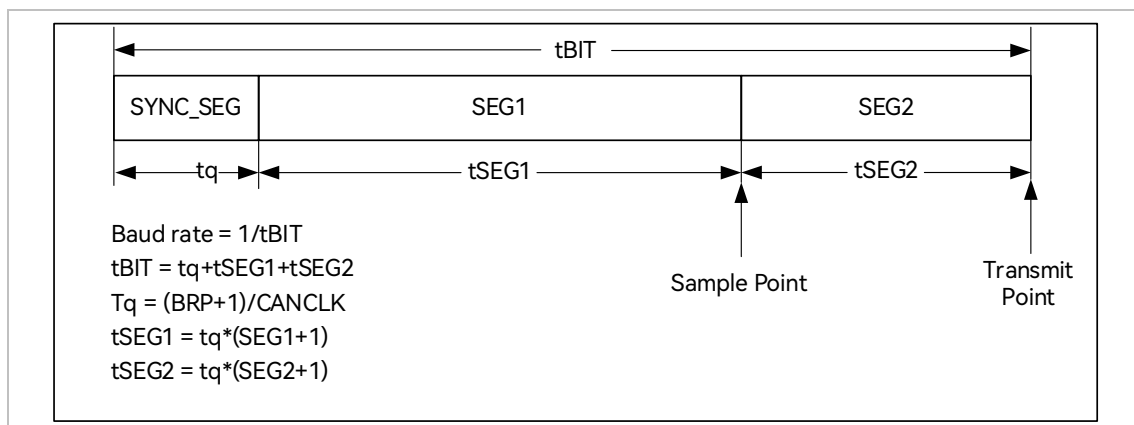
14.7.1 Bit Time Characteristics

CAN controller monitors the CAN bus by sampling edges. It adjusts the Sample Point and Transit Point by synchronizing to the falling edge of Start of Frame (SOF) and re-synchronizing to the falling edge of the subsequent bits.

As shown in Figure 14-5, the bit time is divided into three segments: Synchronization Segment (SYNC_SEG), Time Segment 1 (SEG1) and Time Segment 2 (SEG2). The length of these segments is an integral multiple of time quanta (tq), the smallest unit of time defined by BRP ($\text{CAN\_NBTR}[\text{NBRP}] / \text{CAN\_DBTR}[\text{DBRP}]$).

- SYNC_SEG: That part of the bit time where edges of CAN bus level are expected to occur. It is used for synchronizing different nodes on CAN bus. SYNC_SEG is a constant 1 tq.
- SEG1: It is used for defining position of the Sample Point. It consists of the Propagation Time Segment (PROP_SEG) and Phase Buffer Segment 1 (PHASE_SEG1) specified in CAN Specification. SEG1 is programmed by $\text{CAN\_NBTR}[\text{SEG1}] / \text{CAN\_DBTR}[\text{DSEG1}]$ over 1~64 tq, provided however that it can be automatically lengthened to compensate for forward phase drift caused by frequency difference between different nodes connected to CAN bus.
- SEG2: It is used for defining position of the Transit Point. It is the Phase Buffer Segment 2 (PHASE_SEG2) specified in the CAN Specification. SEG2 is programmed by $\text{CAN\_NBTR}[\text{SEG2}] / \text{CAN\_DBTR}[\text{DSEG2}]$ over 1~32 tq, provided however that it can be automatically shortened to compensate for backward phase drift.

Figure 14-5 Bit Time Structure



A synchronization error may occur during message transfer due to clock rate deviation, delay time and other factors. In this case, CAN_NBTR[SJW]/CAN_DBTR[DSJW] is used to set t_{SJW} for re-synchronization of different CAN nodes. t_{SJW} is configured over the range of 1~4 t_q . If an effective edge (from recessive to dominant) is detected in SEG1 instead of SYNC_SEG, SEG1 is lengthened up to t_{SJW} to shift the position of Sample Point backward. If an effective edge (from recessive to dominant) is detected in SEG2 instead of SYNC_SEG, SEG2 is shortened up to t_{SJW} to shift the position of Sample Point forward.

14.8 Sending Management

The process of sending a message is as follows. Select an empty transmit mailbox by software and then set the identifier, data length and data to be sent. Configure CAN_TMIDx[TREQ] = 1 to generate a transmit request. Note that after CAN_TMIDx[TREQ] is set to “1”, the selected mailbox is no longer empty and the software has no write access to the associated mailbox register. Immediately after CAN_TMIDx[TREQ] is set to “1”, the mailbox enters pending state and waits to become the highest priority mailbox, see Figure 14-6 for the transmit priority. As soon as the mailbox has the highest priority, it will be scheduled for transmission. The transmission starts (enter transmit state) once the CAN bus becomes idle. After the transmission, the mailbox becomes empty again. If the transmission succeeds, CAN_TMSTA[MOKx] is set to “1” by hardware, and if the transmission fails, the failure flag bits are set to “1” by hardware, including arbitration lost flag bit CAN_TMSTA[MALx] and transmit error flag bit CAN_TMSTA[MERRx].

14.8.1 Transmit Priority

Configuring CAN_CR1[TMOD] selects mailbox mode. When the bit is set to “0”, the mailbox works in ID mode, and when it is set to “1”, the mailbox works in FIFO mode.

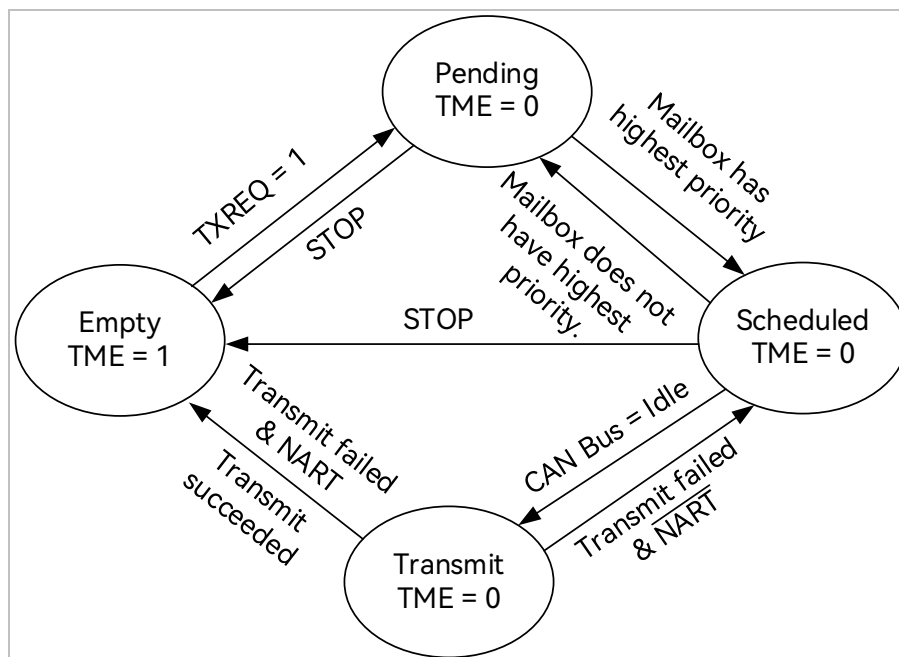
In ID mode, when more than one transmit mailbox is pending, the transmission order is determined by the identifier of the message stored in the mailbox. According to CAN protocol, the message with the lowest identifier value has the highest priority. If the identifier values are equal, the lower mailbox number is scheduled first.

In FIFO mode, the priority order is determined by the transmit request order.

14.8.2 Transmit Abort

A transmission request can be aborted by setting $CAN\_TMSTA[MSTPx] = 1$. If the mailbox is in pending or scheduled state, the request is aborted immediately. If the mailbox is in transmission state, one of the following two situations may occur. The message in the mailbox is transmitted successfully, and the mailbox becomes empty with $CAN\_TMSTA[MOKx]$ setting as “1” by hardware. Or the message in the mailbox fails to be transmitted, and the mailbox becomes scheduled. And then, the request is aborted and the mailbox becomes empty with $CAN\_TMSTA[MOKx]$ setting as “0” by hardware. In all cases, the mailbox becomes empty at the end of the current transmission.

Figure 14-6 Transit Mailbox Status



14.8.3 Automatic Retransmission Disable Mode

The automatic retransmission disable mode is used to implement time-triggered communication feature of the CAN standard. Configuring $CAN\_CR1[NOART] = 1$ enables this mode. In this mode, each transmission is started only once. If it fails, due to an arbitration loss or an error, the hardware will not automatically restart the transmission. At the end of the first transmission attempt, the hardware considers that the request has been completed and sets $CAN\_TMSTA[MDONE]$ bit to “1”. The result of the transmission is indicated by $CAN\_TMSTA[MOKx]$ and $CAN\_TMSTA[MERRx]$ bits.

14.9 Receiving Management

CAN controller consists of three Receive Buffers, including Receive Buffer0, Receive Buffer1 and Receive Buffer2. Each receive buffer contains the following bits: CAN_RXIDx, CAN_RXDTx and CAN_RXxDATy (x = 0,1,2 and y = 0 ~15). CAN controller implements the receiving management by FIFO principle.

After resetting, FIFO write pointer targets Receive Buffer0. During receiving period, the hardware automatically writes bytes to Receive Buffer targeted by the FIFO writer pointer. If no error is detected until the last byte of EOF and the message passes acceptance filtering, the message is considered valid and FIFO write pointer targets the next Receive Buffer. If FIFO write pointer currently targets Receive Buffer2, the pointer re-targets Receive Buffer0. When an error is detected or acceptance filtering fails, FIFO write pointer remains unchanged, suggesting that the next data packet is written to the original Receive Buffer. A Receive Buffer is full when it is loaded with three sets of message object. In such case, the buffer overruns when receiving the next data packet which will be discarded.

CAN_TSPT[MESCNT] is an indicator of valid message counter, and CAN_TSPT[RDPTR] is an indicator of the buffer targeted by FIFO read pointer. The software accesses data bytes by reading Receive Buffers. After that, CAN_CR1[RFD] is set to “1” to free the Receive Buffer targeted by FIFO read pointer which then points to the next Receive Buffer. If FIFO read pointer currently points to Receive Buffer2, it re-points to Receive Buffer0.

14.9.1 Receive Filtering

The Filter Mode, Identifier and Mask Bit are configured to receive desired messages only.

CAN_CR0[FILMOD] bit selects between the Single Filter mode and the Double Filter mode. In single filter mode, only one filter works for acceptance filtering. In double filter mode, two filters work for acceptance filtering.

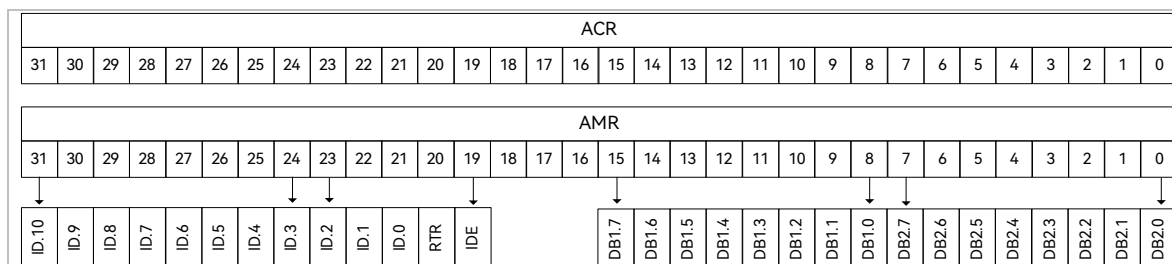
The Identifier is defined by CAN_ACR register.

The Mask Bit is defined by CAN_AMR register. If any bit in CAN_AMR register is “0”, the data packet must match with its associated bit in CAN_ACR register, otherwise, the data packet is filtered. If any bit in CAN_AMR register is “1”, it has no effect.

14.9.1.1 Standard Frame Single Filter Mode

In Standard Frame Single Filter Mode, the filtering part contains a 11-bit ID, RTR, IDE and the first two bytes of data (DB0 and DB1), with its configuration shown in Figure 14-7. If Data Field of a message reads “0” in length, the filter feature of CAN_AMR[15:0] and CAN_ACR[15:0] are disabled; if the Data Field reads “1”, the filter feature of CAN_AMR[7:0] and CAN_ACR[7:0] are disabled.

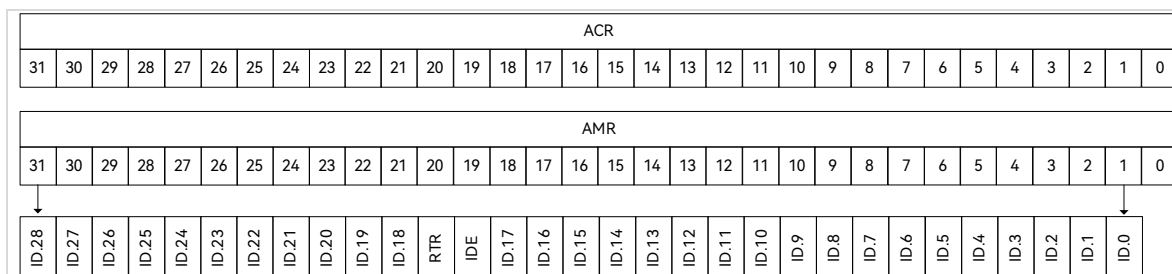
Figure 14-7 Standard Frame Single Filter Mode



14.9.1.2 Extended Frame Single Filter Mode

In Extended Frame Single Filter mode, the filtering part contains a 29-bit ID, RTR and IDE, with its configuration shown in Figure 14-8.

Figure 14-8 Extended Frame Single Filter Mode

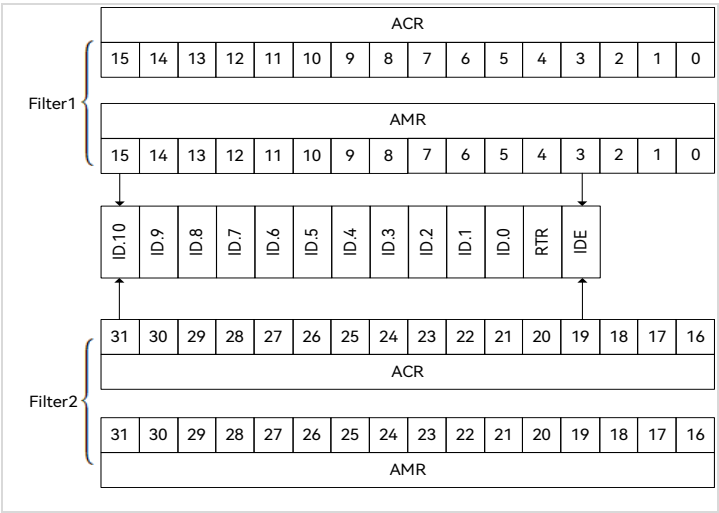


In this mode, if CAN is configured to receive standard frames only, then CAN_AMR[19] and CAN_ACR[19] are set to “0”, and CAN_AMR[15:0] and CAN_ACR[15:0] are set to filter frames containing byte 0 or 1. If CAN is configured to receive extended frames only, then CAN_ACR[19] is set to “1” and CAN_AMR[19] is set to “0”, then CAN_ACR[18:1] and CAN_AMR[18:1] are set to filter data containing extended frames carrying ID[17:0]. If CAN is configured to receive both standard and extended frames, then CAN_ACR[19] is set to “0” or “1” and CAN_AMR[19] is set to “1”.

14.9.1.3 Standard Frame Double Filter Mode

In Standard Frame Double Filter mode, both the Filter 1 and Filter 2 contain an 11-bit ID, RTR and IDE respectively, with its configuration shown in Figure 14-9.

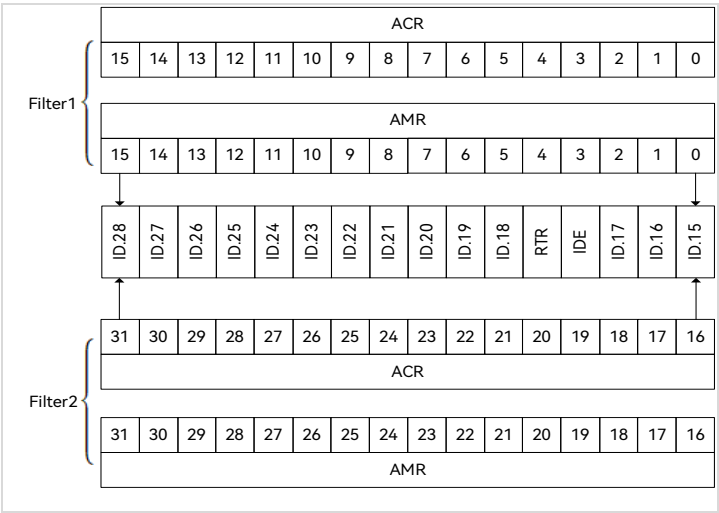
Figure 14-9 Standard Frame Double Filter Mode



14.9.1.4 Extended Frame Double Filter Mode

Error Management In Extended Frame Double Filter mode, the filtering part contains a 14-bit ID, RTR and IDE, with its configuration shown in Figure 14-10.

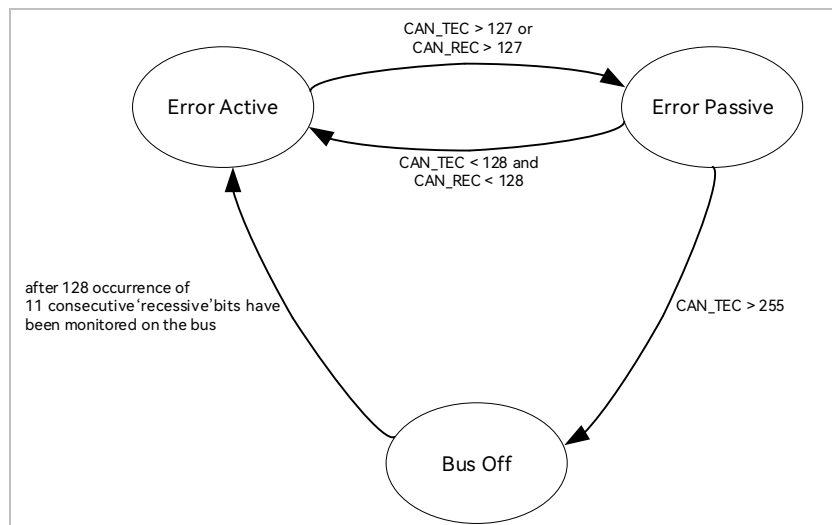
Figure 14-10 Extended Frame Double Filter Mode



14.9.2 Error Management

CAN error processing is implemented by hardware sending the Transmit Error Counter CAN_TEC and Receive Error Counter CAN_REC. CAN_TEC and CAN_REC increases or decreases with the errors. Error states are divided into Error Active, Error Passive and Bus Off, as shown in Figure 14-11. In Bus Off state, CAN cannot receive or transmit messages. The current error state and type are accessed by reading CAN_ERR.

Figure 14-11 CAN Error Processing



14.9.3 CAN FD Operations

There are two modes in CAN FD protocol, Long Frame Mode (LFM) and Fast Frame Mode (FFM). In LFM, the data field of a CAN frame can be longer than eight bytes. In FFM, the control field, data field and CRC field of a CAN frame are transmitted at a higher bit rate compared to the beginning and to the end of the frame. LFM can work with FFM.

The first reserved bit of CAN2.0 frame is now decoded as FDF bit. “FDF = recessive” signifies a CAN FD frame, and “FDF = dominant” signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF, res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by “res = dominant” and “BRS = recessive”. The coding of “res = recessive” is reserved for future expansion of the protocol. When the CAN receives a frame with “FDF = recessive” and “res = recessive”, it signals a Protocol Exception Event by setting bit CAN_CR0[PEX]. If Protocol Exception Handling Disable is enabled (CAN_CR0[PEX] = 0), it causes the operation state to change from Receiver to synchronizing on CAN communication at the next sample point. If Protocol Exception Handling Disable is disabled (CAN_CR0[PEX] = 1), the CAN treats a recessive res bit as a format error and responds with an error frame.

When CAN_CR0[CFDEN] = 1, CAN FD operation is enabled and the CAN bus controller can send or receive both Classic CAN frames (standard frames or extended frames) and CAN FD frames. When CAN_CR0[CFDEN] = 0, the CAN bus controller only sends or receives Classic CAN frames (standard frames

or extended frames). It transmits an error frame if a CAN FD frame is received. When CAN FD operation is disabled, no CAN FD frame is transmitted even if $\text{CAN\_TMDTx[FDF]} = 1$.

After $\text{CAN\_CR0[CFDEN]} = 1$, if $\text{CAN\_TMDTx[FDF]} = 1$ and $\text{CAN\_TMDTx[BRS]} = 0$, the transmission of CAN FD frames without bit rate switching is enabled. If $\text{CAN\_TMDTx[FDF]} = 1$ and $\text{CAN\_TMDTx[BRS]} = 1$, the transmission of CAN FD frames with bit rate switching is enabled.

In CAN FD format, the encoding of DLC differs from that in the standard CAN format. The DLC codes 0 to 8 have the same coding as those in standard CAN, and the codes 9 to 15 (data fields contain 8 bytes in in standard CAN) are encoded according to the table below.

Table 14-2 Encoding of DLC in CAN FD

DLC	9	10	11	12	13	14	15
Number of Data Bytes	12	16	20	24	32	48	64

In CAN FD frames, if BRS bit is recessive, the bit timing is switched inside the frame after the BRS (Bit Rate Switch) bit. Before the BRS bit, in the CAN FD arbitration phase, the standard CAN bit timing is defined by the Nominal Bit Timing and Prescaler Register (CAN_NBTR). In the following CAN FD data phase, the fast CAN bit timing is defined by the Data Bit Timing and Prescaler Register (CAN_DBTR). The bit timing switches back from the fast timing at the CRC delimiter or when an error is detected.

In both data frame formats, CAN FD long and CAN FD fast, the value of the bit ESI (Error Status Indicator) is determined by transmitter's error state at the start of the transmission. If the transmitter is error passive, ESI is transmitted recessive, otherwise, it is transmitted dominant. In CAN FD remote frames, the bit ESI is always transmitted dominant and its value is not determined by transmitter's error state. The data length code of CAN FD remote frame is always transmitted as "0".

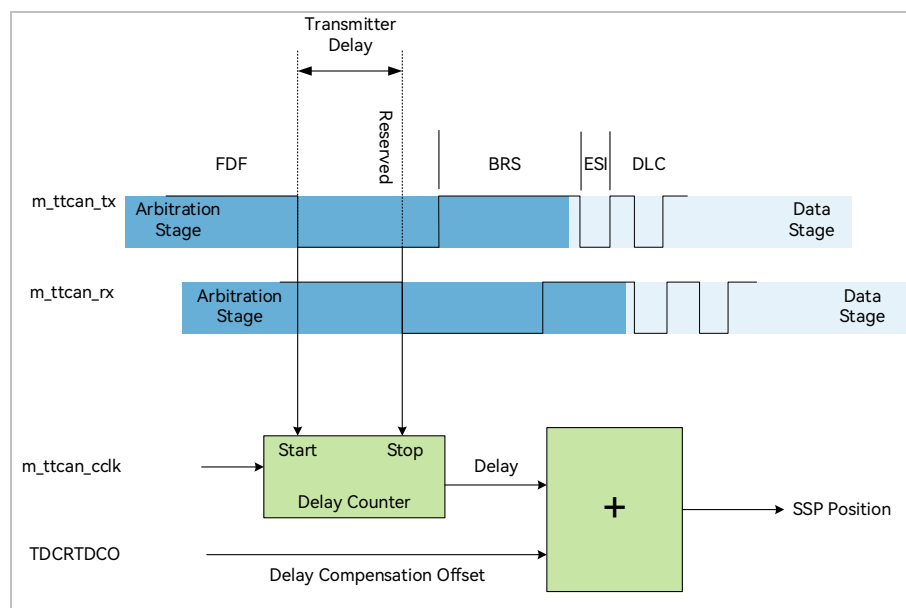
14.9.4 Transmission Delay Compensation

During the data phase of a CAN FD transmission, only one node is transmitting and all others are receivers. The length of the bus line has no effect. When transmitting via pin CTXD, the CAN controller receives data from its local CAN transceiver via pin CRXD after a delay, which is known as CAN transceiver's loop delay. If this delay is greater than T_{SEG1} (time segment before sample point), a bit error is detected. Without the delay compensation, the bit rate in the data phase of a CAN FD frame is limited by the CAN transceiver's loop delay.

The CAN FD unit has implemented a delay compensation mechanism to compensate the CAN transceiver's loop delay, so that it can transmit the data at a higher bit rate during CAN FD data phase. To check bit errors during the data phase of transmitting nodes, the delayed transmitted data is compared with the received data at the secondary sampling point (SSP). If a bit error is detected, the transmitter reacts on this bit error at the next following regular sample point. The delay compensation is always disabled during arbitration phase. It enables configurations where the data bit time is shorter than the transmitter delay, which is described in the new version of ISO11898-1. Configuring `CAN_CR0[TDCEN] = 1` enables transmission delay compensation feature. The received bit is compared with the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the CAN FD unit's output pin CTXD through the transceiver to the receive input pin CRXD plus the transmission delay compensation offset configured by `CAN_TDCR[SSP_OFFSET]`. The transmission delay compensation offset is used to adjust the position of the SSP in the received bit (for example, half of the bit time in the data phase). The position of the second sampling point is rounded down to the next integer number of mtq (minimum time quantum, or one system clock).

When transmission delay compensation is enabled (`CAN_CR0[TDCEN] = 1`), the measurement starts within each transmitted CAN FD frame at the falling edge of bit FDF to bit res, and stops when this edge is seen at the receive input CRXD of the transmitter. The resolution of this measurement is one mtq. The register `CAN_TDCR[TDCO]` displays the delay value in real time.

Figure 14-12 Transmission Delay Compensation



To avoid a dominant glitch inside the received FDF bit that ends the delay compensation measurement before the falling edge of the received res bit (leading to a too early SSP position), a transmitter delay compensation filter window can be enabled by programming CAN_TDCR[TDCF]. This defines a minimum value for the SSP position. When measuring transmitter delay, Dominant edges on the CRXD that may cause an earlier SSP position are ignored for the delay measurement. The measurement stops when the SSP position is at least CAN_TDCR[TDCF] and the CRXD is low.

14.10 CAN Interrupt Sources

CAN supports 11 interrupt sources. An interrupt is generated by setting the corresponding enable bit in CAN_IER. After an interrupt is generated, the associated interrupt flag bit of CAN_IFR is set to “1”.

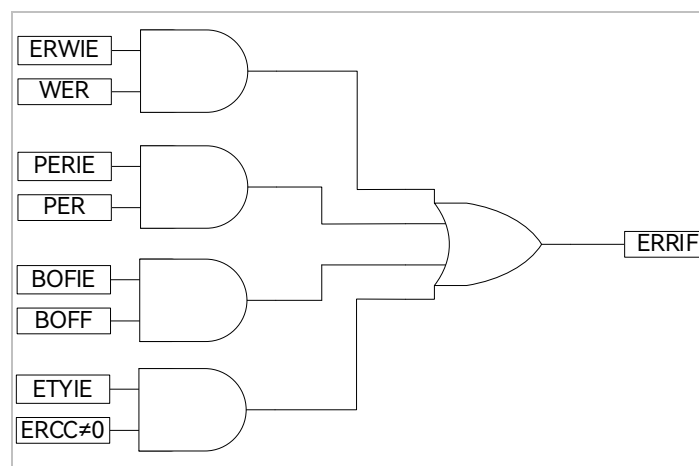
- Receive Interrupt: If no error is detected until the last byte of EOF and the frame passes acceptance filtering, the current frame received is considered valid and CAN_IFR[RXIF] is set to “1”. In this case, a receiver interrupt is generated if Receive Interrupt is enabled (CAN_IER[RXIE] is set to “1”).
- Transmit Completed Interrupt: CAN_IFR[TXIF] is set to “1” at the end of each transmission. In this case, a transmit completed interrupt is generated if Transmit Completed Interrupt is enabled (CAN_IER[TXIE] is set to “1”).
- Overflow Interrupt: In the case of FIFO overflow, CAN_IFR[OVIF] is set to “1”. An overflow interrupt is generated if Overflow Interrupt is enabled (CAN_IER[OVIE] is set to “1”).
- Arbitration Lost Interrupt: CAN_IFR[ARBIF] is set to “1” when a node loses arbitration to other nodes and thus loses priority in CAN bus access. In this case, an arbitration loss interrupt is generated if Arbitration Lost Interrupt is enabled (CAN_IER[ARBIE] is set to “1”).
- Sleep Mode Interrupt: CAN_IFR[SLPIF] is set to “1” when CAN controller enters the Sleep Mode. In this case, a sleep mode interrupt is generated if Sleep Mode Interrupt is enabled (CAN_IER[SLPIE] is set to “1”).
- Wake-up Interrupt: In Auto Wakeup mode, CAN_IFR[WKUIF] is set to “1” when a SOF bit is detected. In this case, a wake-up interrupt is generated if Wake-up Interrupt is enabled (CAN_CR0[AWU] and CAN_IER[WKUIE] are set to “1”).
- Overload Frame Interrupt: CAN module automatically sends an overload frame when the overload interrupt is enabled and the conditions for transmitting the overload frame are met. An overload frame interrupt is generated after the first byte of the overload frame is successfully sent.

> Error Interrupt

- » Error Warning Interrupt: The Error Warning Flag CAN_ERR[WER] is set to “1” when $CAN\_TEC \geq CAN\_LIM$ or $CAN\_REC \geq CAN\_LIM$. An interrupt is generated if Error Warning Interrupt is enabled (CAN_IER[ERWIE] is set to “1”), Error Interrupt is enabled (CAN_IER[ERRIE] is set to “1”) and an error is detected.
- » Error Passive Interrupt: The Error Passive Flag CAN_ERR[PER] is set to “1” when $CAN\_TEC > 127$ or $CAN\_REC > 127$. An interrupt is generated if Error Passive Interrupt is enabled (CAN_IER[PERIE] is set to “1”), Error Interrupt is enabled (CAN_IER[ERRIE] is set to “1”) and an error is detected.
- » Bus Off Interrupt: The Bus Off Flag CAN_ERR[BOFF] is set to “1” when $CAN\_TEC > 255$. An interrupt is generated if Bus Off Interrupt is enabled (CAN_IER[BOFIE] is set to “1”), Error Interrupt is enabled (CAN_IER[ERRIE] is set to “1”) and an error is detected.
- » Error Type Interrupt: When any of bit error, format error, stuff error, ACK error and CRC error is detected, CAN_ERR[ETY] changes into a non-zero value indicating the error type. An interrupt is generated if Error Type Interrupt is enabled (CAN_IER[ETYIE] is set to “1”), Error Interrupt is enabled (CAN_IER[ERRIE] is set to “1”) and an error is detected.

Error Interrupts are divided into Error Warning Interrupt, Error Passive Interrupt, Bus Off Interrupt and Error Type Interrupt. Relationship among CAN_IFR[ERRIF], CAN_ERR[WER], CAN_ERR[PER], CAN_ERR[BOFF] and CAN_ERR[ERCC] and their enable bits are illustrated in Figure 14-13. CAN_IFR[ERRIF] bit is an Error Interrupt indicator, while CAN_ERR[WER], CAN_ERR[PER], CAN_ERR[BOFF] and CAN_ERR[ERCC] are status indicators. Thus, when an Error Interrupt is triggered, the error information is accessed by reading the Status flag bits. CAN_IFR[ERRIF] bit is cleared by software.

Figure 14-13 Relationship among ERRIF, WER, PER, BOFF, ERCC Bits and Their Enable Bits



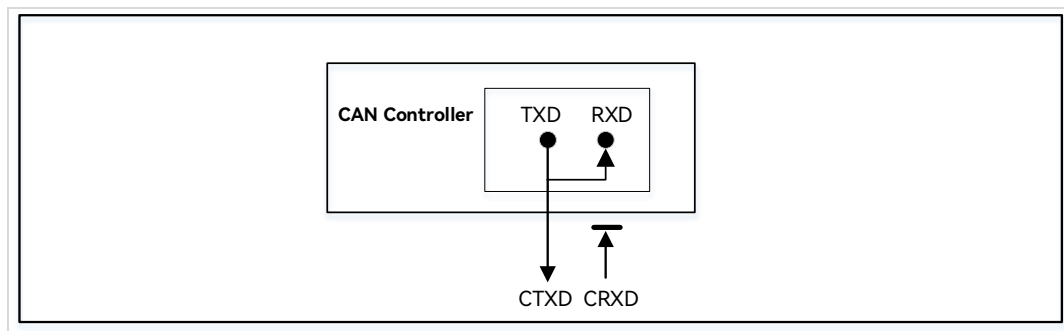
14.11 Test Mode

CAN controller can operate in Self-test Mode, Monitoring Mode and Self-test Mode & Monitoring Mode by programming CAN_CR0[SELFTST] and CAN_CR0[LISTEN] bits.

14.11.1 Self-test Mode

CAN controller operates in Self-test Mode after CAN_CR0[SELFTST] is set to “1” and CAN_CR0[LISTEN] is cleared to “0”. The connection diagram is shown in Figure 14-14 . CRXD pin is disconnected from CAN controller. CAN controller performs internal feedback from its CTXD output to its CRXD input, and ignores the actual status on CRXD pin and ACK errors (recessive bit is not sampled in the ACK slot of a frame). In this mode, when CAN_CR1[RSELF] is set to “1”, CAN controller internally reroutes the sent frames and writes back to a Receive Buffer if the frames are considered valid. When CAN_TMIDx[TREQ] is set to “1”, CAN controller only sends the frames and does not perform a write-back to any Receive Buffer, regardless of whether the frames are valid or not.

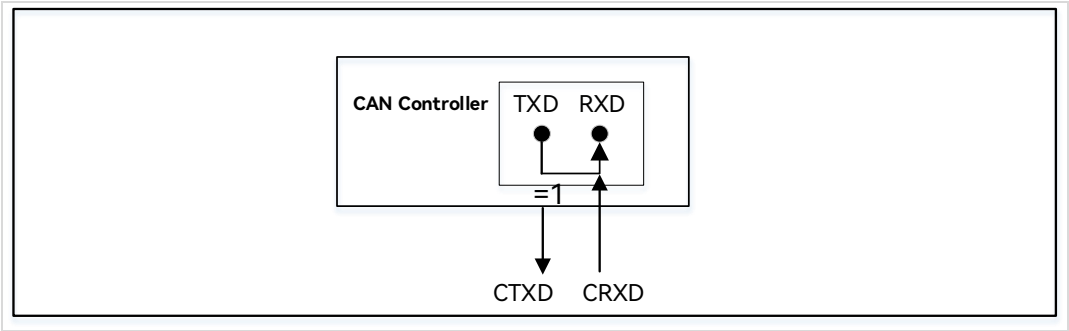
Figure 14-14 Self-test Mode



14.11.2 Monitoring Mode

CAN controller operates in Monitoring Mode when CAN_CR0[SELFTST] is set to “0” and CAN_CR0[LISTEN] to “1”. The connection diagram is shown in Figure 14-15. In this mode, CTXD pin is driven HIGH (recessive). CAN controller receives the data frames normally, but the dominant bit transmitted is rerouted internally instead of sending to CTXD pin, so the frames cannot be transferred to CAN bus. It is used to analyze CAN bus activities without affecting the bus.

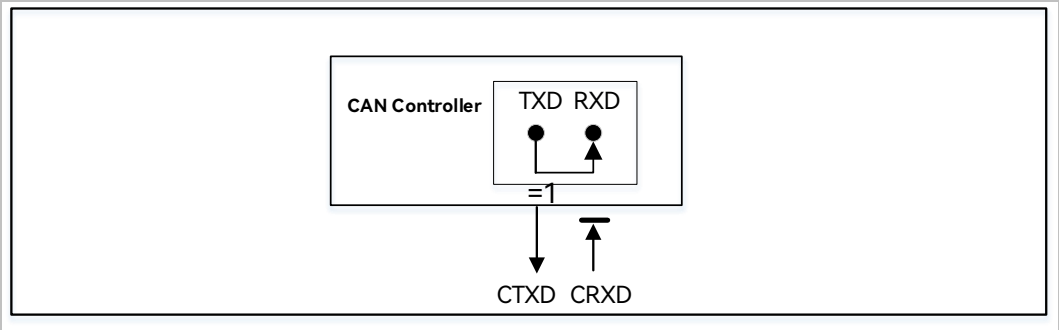
Figure 14-15 Monitoring Mode



14.11.3 Self-test Mode & Monitoring Mode

CAN controller operates in Self-test Mode & Monitoring Mode when CAN_CR0[SELFTST] and CAN_CR0[LISTEN] are set to “1” at the same time. The connection diagram is shown in Figure 14-16. CRXD pin is disconnected from CAN controller and CTXD pin is driven HIGH (recessive). In this mode, CAN controller operates without affecting CAN bus, performs internal feedback from its TXD output to its RXD input, and ignores ACK errors.

Figure 14-16 Self-test Mode & Monitoring Mode



14.12 CAN Registers

14.12.1 CAN_CR0 (CSR: 0x1C0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																			TDCSEL	TDCEN	PEX	NISO	CFDEN	CANEN	RSV		AWU	FILMOD	SELFST	LISTEN	RSTMOD
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	-	-	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	-	-	0	0	0	0	0

Bit	Name	Description
[31:13]	RSV	Reserved
[12]	TDCSEL	Transmission Delay Compensation Mode Selection 0: The measured value plus software offset 1: Software offset only
[11]	TDCEN	Transmission Delay Compensation Enable 0: Disable 1: Enable
[10]	PEX	Protocol Exception Handling Disable 0: Disable 1: Enable
[9]	NISO	ISO/BOSCH 0: ISO 1: BOSCH
[8]	CFDEN	CAN FD Enable 0: Disable 1: Enable
[7]	CANEN	CTXD and CRXD Pin Multiplex and CAN Enable 0: No Multiplexing; CAN Disabled. 1: Multiplexing; CAN enabled and initialized.
[6:5]	RSV	Reserved
[4]	AWU	Auto Wakeup Enable When Auto Wakeup feature is enabled, CAN_CR1[SLPREQ] and CAN_STS[SLPACK] are automatically cleared to “0” by hardware after CAN controller detects a frame to wake up the device. 0: Disable 1: Enable
[3]	FILMOD	Filter Mode 0: Double Filter Mode 1: Single Filter Mode
[2]	SELFTST	Self-test Mode Enable 0: Disable 1: Enable
[1]	LISTEN	Monitoring Mode Enable 0: Disable 1: Enable
[0]	RSTMOD	Reset Mode Read:

		0: CAN controller is not in Reset Mode 1: CAN controller is in Reset Mode Write: 0: After initialization, CAN controller synchronizes itself with CAN bus to enter Normal Operation Mode. 1: Enter the Reset Mode

14.12.2 CAN_CR1 (CSR: 0x1C1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																	TTCM	RSV						TMOD	OLREQ	SLPREQ	RSELF	RSV	RFD	NOART	RSV
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	-	-	-	-	-	-	rw	rw	rw	rw	-	w1	rw	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	0	0	0	0	-	0	0	-

Bit	Name	Description
[31:15]	RSV	Reserved
[14]	TTCM	Sample Mode by Two out of Three Options Enable 0: Disable 1: Enable
[13:8]	RSV	Reserved
[7]	TMOD	Transmit Mailbox Mode 0: ID Mode 1: FIFO Mode
[6]	OLREQ	Overload Frame Request 0: No request pending 1: Request pending
[5]	SLPREQ	Sleep Mode Request CAN controller requests to enter sleep mode when this bit is programmed to "1" by software, and enters the sleep mode after processing (transmitting or receiving) of the current frame on CAN bus. A request to exit the sleep mode is sent by programming this bit to "0", after which CAN controller starts re-synchronization to the CAN bus. 0: No request pending 1: Request pending
[4]	RSELF	Self-receiving Mode The sent message is received by the transmitter and stored in FIFO buffer.

		0: Disable 1: Enable
[3]	RSV	Reserved
[2]	RFD	Free Receive Buffer Targeted by the Read Pointer CAN_TSPT[RDPTR]. Write: 0: Do not free the Receive Buffer, and the read pointer CAN_TSPT[RDPTR] targets the original buffer. 1: Free the Receive Buffer, and the read pointer CAN_TSPT[RDPTR] targets the next buffer
[1]	NOART	Automatic Retransmission Disable Mode 0: Disable, where messages are automatically re-transmitted if the transmission fails. 1: Enable, where messages are transmitted just once no matter the transmission is successful or not.
[0]	RSV	Reserved

14.12.3 CAN_STS (CSR: 0x1C2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								SLPACK	TXING	RXING	RSV		FOV	FEMP	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	-	-	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	0	0

Bit	Name	Description
[31:7]	RSV	Reserved
[6]	SLPACK	Sleep Mode Acknowledge CAN controller enters sleep mode when this bit is programmed to “1” by hardware. It is used to acknowledge a sleep mode request by software. This bit is cleared to “0” by hardware after CAN controller exits the sleep mode. Read: 0: CAN is not in sleep mode 1: CAN is in sleep mode Write: 0: This bit is cleared to “0” and CAN controller exits the sleep mode. 1: No effect

[5]	TXING	Transmitting Flag 0: CAN is not transmitting messages. 1: CAN is transmitting messages.
[4]	RXING	Receiving Flag 0: CAN is not receiving messages. 1: CAN is receiving messages.
[3:2]	RSV	Reserved
[1]	FOV	FIFO Overflow Flag 0: FIFO does not overflow. 1: FIFO overflows.
[0]	FEMP	FIFO Empty Flag 0: FIFO is empty. 1: FIFO is not empty.

14.12.4 CAN_IER (CSR: 0x1C3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				WKUIE	SLPIE	OVLIE	ERRIE	ETYLE	BOFIE	PERIE	ERWIE	OVIE	ARBIE	TXIE	RXIE
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11]	WKUIE	Wakeup Interrupt Enable 0: Disable 1: Enable
[10]	SLPIE	Sleep Mode Interrupt Enable 0: Disable 1: Enable
[9]	OVLIE	Overload Interrupt Enable 0: Disable 1: Enable
[8]	ERRIE	Error Interrupt Enable 0: Disable 1: Enable

[7]	ETYIE	Error Type Interrupt Enable 0: Disable 1: Enable
[6]	BOFIE	Bus Off Interrupt Enable 0: Disable 1: Enable
[5]	PERIE	Passive Error Interrupt Enable 0: Disable 1: Enable
[4]	ERWIE	Error Warning Interrupt Enable 0: Disable 1: Enable
[3]	OVIE	Overflow Interrupt Enable 0: Disable 1: Enable
[2]	ARBIE	Arbitration Lost Interrupt 0: Disable 1: Enable
[1]	TXIE	Transmit Completed Interrupt Enable 0: Disable 1: Enable
[0]	RXIE	Receive Interrupt Enable 0: Disable 1: Enable

14.12.5 CAN_IFR (CSR: 0x1C4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							WKUIF	SLPIF	OVLIF	ERRIF	OVIF	ARBIF	TXIF	RXIF	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0	rw0	rw0	rw0	rw0	rw0	rw0	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	WKUIF	Wakeup Interrupt Flag This bit is set to “1” by hardware whenever CAN controller detects a SOF bit in auto wakeup mode.

		Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[6]	SLPIF	Sleep Mode Interrupt Flag This bit is programmed to “1” by hardware when CAN controller enters the sleep mode. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	OVLIF	Overload Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[4]	ERRIF	Error Interrupt Flag This bit is set to “1” by hardware when an Error Interrupt is enabled and CAN controller detects an associated error. See CAN Interrupt Sources for details. This bit is cleared to “0” by software. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[3]	OVIF	Overflow Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

[2]	ARBIF	Arbitration Lost Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[1]	TXIF	Transmit Completed Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[0]	RXIF	Receive Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending  Note: This bit can be set to “1” by hardware only and cannot be cleared to “0” by software. It is cleared to “0” by setting CAN_CR1[RFD] to “1” to free Receive Buffers.

14.12.6 CAN_TSPT (CSR: 0x1C5)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												RDPTR		MESCNT	
																												r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	

Bit	Name	Description
[31:4]	RSV	Reserved
[3:2]	RDPTR	FIFO Read Pointer 00: FIFO read pointer targets Receive Buffer0

		01: FIFO read pointer targets Receive Buffer1 10: FIFO read pointer targets Receive Buffer2 11: Reserved
[1:0]	MESCNT	Valid Message Counter

14.12.7 CAN_NBTR (CSR: 0x1C6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV			SEG2					RSV		SEG1					SJW					RSV	NBRP										
-	-	-	rw	rw	rw	rw	rw	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	0	0	0	0	0	-	-	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:29]	RSV	Reserved
[28:24]	SEG2	Nominal time period after the sampling point
[23:22]	RSV	Reserved
[21:16]	SEG1	Nominal time period before the sampling point
[15:11]	SJW	Re-synchronization Jump Width $t_{SJW} = tq \cdot (SJW + 1)$
[10]	RSV	Reserved
[9:0]	NBRP	Nominal baud rate prescaler

14.12.8 CAN_DBTR (CSR: 0x1C7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV				DSEG2				RSV			DSEG1				RSV	DSJW				RSV			DBRP								
-	-	-	-	rw	rw	rw	rw	-	-	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	-	-	-	-	-	rw	rw	rw	rw	rw	rw
-	-	-	-	0	0	0	0	-	-	-	0	0	0	0	0	-	0	0	0	0	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:28]	RSV	Reserved
[27:24]	DSEG2	Data time period after the sampling point
[23:21]	RSV	Reserved
[20:16]	DSEG1	Data time period before the sampling point

[15]	RSV	Reserved
[14:11]	DSJW	Re-synchronization Jump Width $t_{DSJW} = tq \cdot (DSJW + 1)$
[10:6]	RSV	Reserved
[5:0]	DBRP	Data baud rate prescaler

14.12.9 CAN_TDCR (CSR: 0x1C8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV									TDCO							RSV	TDCFLT							RSV	SSP_OFFSET						
-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	-	w	w	w	w	w	w	w	-	w	w	w	w	w	w	w
-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

Bit	Name	Description
[31:23]	RSV	Reserved
[22:16]	TDCO	Transmission Delay Compensation Value Position of the secondary sampling point (SSP) defined as the sum of the measured delay from CTXD to CRXD pin plus the transmission delay compensation offset configured by CAN_TDCR[SSP_OFFSET]. In data phase, SSP position is the minimum of mtq (minimum time quantum) between the start of the transmitted bit and the secondary sample point, ranging from 0 to 127 mtq.
[15]	RSV	Reserved
[14:8]	TDCFLT	Transmission Delay Compensation Filter Window Length It defines the minimum SSP position for the delay measurement.
[7]	RSV	Reserved
[6:0]	SSP_OFFSET	Transmission Delay Compensation Offset It defines the offset value of the measured delay from CTXD to CRXD pin plus the distance between the second sampling point, ranging from 0 to 127 mtq.

14.12.10 CAN_ACR (CSR: 0x1C9)

CAN_ACR																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	CAN_ACR	Filter Identifier Register

14.12.11 CAN_AMR (CSR: 0x1CA)

CAN_AMR																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	CAN_AMR	Filter Mask Register

14.12.12 CAN_ERR (CSR: 0x1CB)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CTEC								CREC								RSV			ALCC				ERCC			RSV		BOFF	PER	WER		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	-	-	r	r	r	r	r	r	r	r	r	-	-	r	r	r
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0	0	0	0	0	-	-	0	0	0

Bit	Name	Description
[31:24]	CTEC	CAN Transmit Error Counter
[23:16]	CREC	CAN Receive Error Counter
[15:13]	RSV	Reserved

[12:8]	ALCC	This bit is used to indicate the position where arbitration fails in the arbitration field.
[7:5]	ERCC	Error Type 000: None 001: Bit Error 010: Format Error 011: Stuff Error 100: ACK Error 101: CRC Error 110: Reserved 111: Reserved
[4:3]	RSV	Reserved
[2]	BOFF	Bus Off Flag 0: CAN module is not in bus off state. 1: CAN module is in bus off state.
[1]	PER	Error Passive Flag 0: The CAN module is error active when CAN_TEC ≤ 127 and CAN_REC ≤ 127. 1: The CAN module is error passive when CAN_TEC > 127 or CAN_REC > 127.
[0]	WER	Error Warning Flag 0: No error warning occurs when CTEC < CAN_LIM and CREC < CAN_LIM. 1: An error warning occurs when CTEC ≥ CAN_LIM or CREC ≥ CAN_LIM.

14.12.13 CAN_ERLIM (CSR: 0x1CC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								ERLIM							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0	0	1	0	1	1	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	ERLIM	Error warning counter. An error warning occurs when CAN_ERR[CTEC] ≥ CAN_LIM or CAN_ERR[CREC] ≥ CAN_LIM

14.12.14 CAN_TMSTA (CSR: 0x1CD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSL2	MSL1	MSL0	MNUM		ME2	ME1	ME0	MSTP2	RSV			MERR2	MAL2	MOK2	MDONE2	MSTP1	RSV			MERR1	MAL1	MOK1	MDONE1	MSTP0	RSV			MERR0	MAL0	MOK0	MDONE0
r	r	r	r	r	r	r	r	rw	-	-	-	rw1	rw1	rw1	rw1	rw	-	-	-	rw1	rw1	rw1	rw1	rw	-	-	-	rw1	rw1	rw1	rw1
0	0	0	0	0	1	1	1	0	-	-	-	0	0	0	0	0	-	-	-	0	0	0	0	0	-	-	-	0	0	0	0

Bit	Name	Description
[31]	MSL2	Mailbox 2 has lower priority in the transmit FIFO buffer When this bit is set as “1”, it indicates that mailbox 2 has lower priority in the transmit FIFO buffer if two or more frames are to be sent.
[30]	MSL1	Mailbox 1 has lower priority in the transmit FIFO buffer When this bit is set as “1”, it indicates that mailbox 1 has lower priority in the transmit FIFO buffer if two or more frames are to be sent.
[29]	MSL0	Mailbox 0 has lower priority in the transmit FIFO buffer When this bit is set as “1”, it indicates that mailbox 0 has lower priority in the transmit FIFO buffer if two or more frames are to be sent.
[28:27]	MNUM	When the transmit FIFO buffer is not full, MNUM refers to the number of the next mailbox to be sent. When the transmit FIFO buffer is full, MNUM refers to the number of the last mailbox to be sent.
[26]	ME2	Transmit Mailbox 2 Status 0: Transmit Mailbox 2 is not empty. 1: Transmit Mailbox 2 is empty.
[25]	ME1	Transmit Mailbox 1 Status 0: Transmit Mailbox 1 is not empty. 1: Transmit Mailbox 1 is empty.
[24]	ME0	Transmit Mailbox 0 Status 0: Transmit Mailbox 0 is not empty. 1: Transmit Mailbox 0 is empty.
[23]	MSTP2	Mailbox 2 Transmission Stop Setting this bit to “1” stops the transmission of mailbox 2. When mailbox 2 becomes empty, this bit is automatically cleared to “0” by hardware.
[22:20]	RSV	Reserved
[19]	MERR2	Mailbox 2 Transmission Error This bit is set to “1” by hardware when mailbox 2 transmission error occurs. A write of “1” by software or to CAN_TMSTA[MDONE2] clears this bit to “0”.

		It can also be cleared to “0” by hardware at the beginning of the next transmission.
[18]	MAL2	Mailbox 2 Arbitration Loss This bit is set to “1” by hardware when mailbox 2 arbitration loss occurs. A write of “1” by software or to CAN_TMSTA[MDONE2] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission.
[17]	MOK2	Mailbox 2 Transmission Succeeded This bit is set to “1” by hardware if the transmission is completed and no error occurs. A write of “1” by software or to CAN_TMSTA[MDONE2] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: The transmission is completed and an error occurs. 1: The transmission is completed and no error occurs. Write: 0: No effect 1: This bit is cleared to “0”.
[16]	MDONE2	Mailbox 2 Transmission Completed This bit is set to “1” by hardware when the transmission is completed or aborted. A write of “1” by software clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: Mailbox 2 is transmitting the message. 1: Mailbox 2 has transmitted the message. Write: 0: No effect 1: This bit is cleared to “0”.
[15]	MSTP1	Mailbox 1 Transmission Stop Setting this bit to “1” stops the transmission of mailbox 1. When mailbox 1 becomes empty, this bit is automatically cleared to “0” by hardware.
[14:12]	RSV	Reserved
[11]	MERR1	Mailbox 1 Transmission Error This bit is set to “1” by hardware when mailbox 1 transmission error occurs. A write of “1” by software or to CAN_TMSTA[MDONE1] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission.

[10]	MAL1	Mailbox 1 Arbitration Loss This bit is set to “1” by hardware when mailbox 1 arbitration loss occurs. A write of “1” by software or to CAN_TMSTA[MDONE1] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission.
[9]	MOK1	Mailbox 1 Transmission Succeeded This bit is set to “1” by hardware when the transmission is completed and no error occurs. A write of “1” by software or to CAN_TMSTA[MDONE1] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: The transmission is completed and an error occurs. 1: The transmission is completed and no error occurs. Write: 0: No effect 1: This bit is cleared to “0”
[8]	MDONE1	Mailbox 1 Transmission Completed This bit is set to “1” by hardware if the transmission is completed or aborted. A write of “1” by software clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: Mailbox 1 is transmitting the message. 1: Mailbox 1 has transmitted the message. Write: 0: No effect 1: This bit is cleared to “0”
[7]	MSTP0	Mailbox 0 Transmission Stop Setting this bit to “1” stops the transmission of mailbox 1. When mailbox 0 becomes empty, this bit is automatically cleared to “0” by hardware.
[6:4]	RSV	Reserved
[3]	MERR0	Mailbox 0 Transmission Error This bit is set to “1” by hardware when mailbox 0 transmission error occurs. A write of “1” by software or to CAN_TMSTA[MDONE0] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission.
[2]	MAL0	Mailbox 0 Arbitration Loss This bit is set to “1” by hardware when mailbox 0 arbitration loss occurs. A write of “1” by software or to CAN_TMSTA[MDONE0] clears this bit to “0”.

		It can also be cleared to “0” by hardware at the beginning of the next transmission.
[1]	MOK0	Mailbox 0 Transmission Succeeded This bit is set to “1” by hardware if the transmission is completed and no error occurs. A write of “1” by software or to CAN_TMSTA[MDONE0] clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: The transmission is completed and an error occurs. 1: The transmission is completed and no error occurs. Write: 0: No effect 1: This bit is cleared to “0”
[0]	MDONE0	Mailbox 0 Transmission Completed This bit is set to “1” by hardware if the transmission is completed or aborted. A write of “1” by software clears this bit to “0”. It can also be cleared to “0” by hardware at the beginning of the next transmission. Read: 0: Mailbox 0 is transmitting the message. 1: Mailbox 0 has transmitted the message. Write: 0: No effect 1: This bit is cleared to “0”

14.12.15 CAN_TMIDx (CSR: 0x1CE/0x1D0/0x1D2) (x = 0/1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDID[10:0]/ EXTID[28:18]											EXTID[17:0]																RSV		TREQ		
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	-	-	w1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	0

Bit	Name	Description
[31:21]	STDID[10:0]/ EXTID[28:18]	Identifier STDID [10:0]: Identifier in Standard Frame EXTID[28:18]: Identifier in Extended Frame

[20:3]	EXTID[17:0]	EXTID[17:0]: Identifier in Extended Frame
[2:1]	RSV	Reserved
[0]	TREQ	Mailbox X TX Request 0: No request is generated 1: A request is generated

14.12.16 CAN_TMDTx (CSR: 0x1CF/0x1D1/0x1D3) (x = 0/1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							IDE	RTR	FDF	BRS	ESI	DLC			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:9]	RSV	Reserved
[8]	IDE	Extended Identifier 0: 11-bit identifier in standard frame. 1: 29-bit identifier in extended frame.
[7]	RTR	Remote Transmission Request 0: Data Frame 1: Remote Frame
[6]	FDF	CAN Frame Selection 0: Classic CAN Frame (standard frame or extended frame) 1: CAN FD Frame
[5]	BRS	Bit Rate Switching Enable 0: Disable 1: Enable
[4]	ESI	Error State Indicator 0: This bit is determined by the error passive flag bit. 1: This bit is transmitted recessive.
[3:0]	DLC	Data Length Code 0-8: CAN + CAN FD: The received frame contains 0-8 bytes of data. 9-15: CAN: The received frame contains 8 bytes of data. 9-15: CAN FD: The received frame contains 12/16/20/24/32/48/64 bytes of data.

14.12.17 CAN_TX0DATx (0x400000A0 + x*4)

x refers to offset address of the mailbox where x = 0,1,2,...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y+3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y+2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y+1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

14.12.18 CAN_TX1DATx (0x400000E0 + x*4)

x refers to offset address of the mailbox where x = 0,1,2, ...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y + 3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y + 2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y + 1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

14.12.19 CAN_TX2DATx (0x40000120 + x*4)

x refers to offset address of the mailbox where x = 0,1,2, ...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y + 3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y + 2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y + 1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

14.12.20 CAN_RXIDx (0x40000160 + x*72)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDID[10:0]/ EXTID[28:18]												EXTID[17:0]												RSV							
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	-	-	-
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-

Bit	Name	Description
[31:21]	STDID[10:0]/ EXTID[28:18]	Identifier STDID [10:0]: Identifier in Standard Frame EXTID[28:18]: Identifier in Extended Frame
[20:3]	EXTID[17:0]	EXTID[17:0]: Identifier in Extended Frame
[2:0]	RSV	Reserved

14.12.21 CAN_RXDTx (0x40000164 + x*72)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							IDE	RTR	FDF	BRS	ESI	DLC			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:9]	RSV	Reserved
[8]	IDE	Extended Identifier 0: 11-bit identifier in standard frame. 1: 29-bit identifier in extended frame.
[7]	RTR	Remote Transmission Request 0: Data Frame 1: Remote Frame
[6]	FDF	CAN Frame Selection 0: Classic CAN Frame (standard frame or extended frame) 1: CAN FD Frame
[5]	BRS	Bit Rate Switching Enable 0: Disable 1: Enable
[4]	ESI	Error State Indicator 0: This bit is determined by the error passive flag bit. 1: This bit is transmitted recessive.
[3:0]	DLC	Data Length Code 0–8: CAN + CAN FD: The received frame contains 0–8 bytes of data. 9–15: CAN: The received frame contains 8 bytes of data. 9–15: CAN FD: The received frame contains 12/16/20/24/32/48/64 bytes of data.

14.12.22 CAN_RX0DATx (0x40000168 + x*4)

x refers to offset address of the mailbox where x = 0,1,2,...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y + 3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y + 2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y + 1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

14.12.23 CAN_RX1DATx (0x40000168 + x*4)

x refers to offset address of the mailbox where x = 0,1,2,...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y + 3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y + 2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y + 1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

14.12.24 CAN_RX2DATx (0x40000168 + x*4)

x refers to offset address of the mailbox where x = 0,1,2,...,15.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAT(y+3)								DAT(y+2)								DAT(y+1)								DAT(y+0)							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

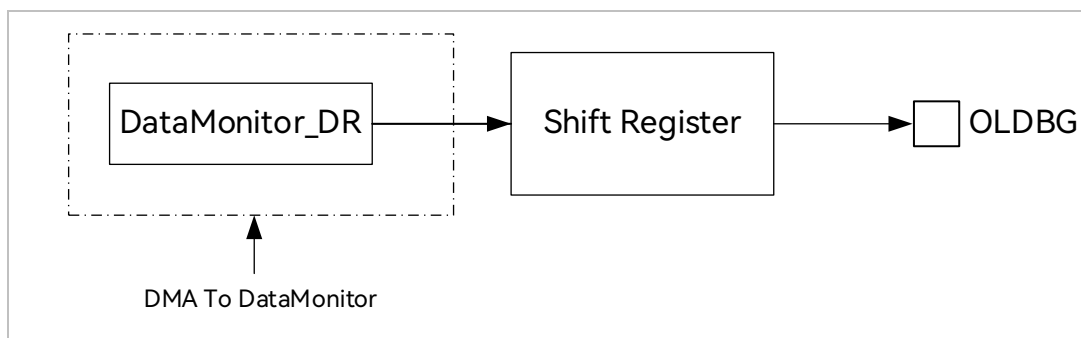
Bit	Name	Description
[31:24]	DAT(y+3)	Data byte y + 3 (y = x*4)
[23:16]	DAT(y+2)	Data byte y + 2 (y = x*4)
[15:8]	DAT(y+1)	Data byte y + 1 (y = x*4)
[7:0]	DAT(y+0)	Data byte y + 0 (y = x*4)

15 DataMonitor

15.1 DataMonitor Introduction

DataMonitor is a high-speed simplex asynchronous serial communication interface, and its functional block diagram is shown in the figure below.

Figure 15-1 Schematic Diagram of DataMonitor



15.2 DataMonitor Operations

DataMonitor is configured via DMA, which controls the transmission enable signal and sets the specific data content and data length. For detailed configurations, see section 29 DMA.

16 Timer2/5/6

16.1 Timer2/5/6 Instructions

Timer2/5/6 supports the following six working modes:

- > Output mode: PWM generation
- > Input capture mode: Detect the duration of high and low level of input PWM
- > Input counter mode: Detect input time of the set PWM wave numbers
- > QEP input mode & RSD mode: Quadrature encoder pulse & tailwind/headwind detection mode
- > Step mode: Detect rotation direction, position and speed of step motor
- > QEP output mode: Quadrature encoder pulse output mode

Timer2/5/6 has the following features:

- > 3-bit programmable prescaler divides the system clock
- > 16-bit up-counting basic counter. Counting clock source serves as the output of prescaler
- > 16-bit up/down-counting special counter for input counter mode, with external input signal selected as clock source
- > 16-bit up/down-counting special counter for QEP input/output mode
- > Input filter module
- > Edge detection module
- > PWM generation module
- > Interrupt event

16.1.1 Prescaler

Prescaler divides the system clock frequency and generates clock source for basic counter. 8 frequency division coefficients of prescaler are available and can be selected by TIMx_CR0[TxPSC]. Since this register has no buffer, the clock source frequency is updated immediately after TIMx_CR0[TxPSC] is written. Therefore, the frequency division coefficients shall be configured when basic counter is not working. The

clock source frequency formula is: $\text{clk\_psc} = \text{TxCLK} / (2^{\text{TIMx\_CR0[TxPSC]}})$. The clock rate corresponding to different TIMx_CR0[TxPSC] value is shown in Table 16-1.

Table 16-1 Mapping between Clock Rate and TIMx_CR0[TxPSC]

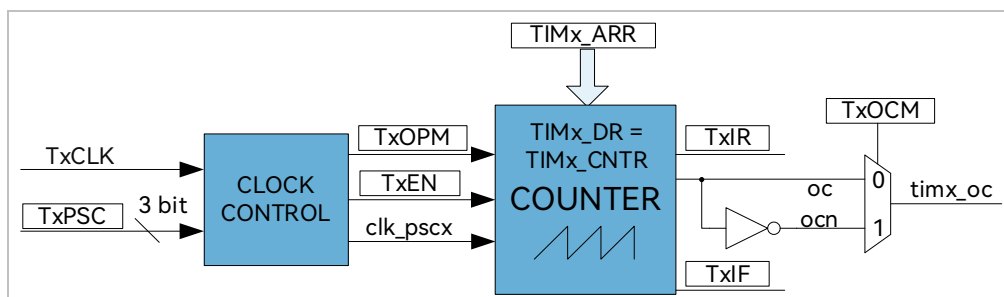
TIMx_CR0[TxPSC]	Division Factor	TIMx_CR0[TxPSC]	Division Factor
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128

16.2 Reading, Writing, and Counting of TIMx_CNTR

When TIMx_CR1[TxEN] = 1, TIMx_CNTR starts to count. The write operation to TIMx_CNTR directly changes the value of the register, so basic counter shall be disabled before the write operation.

16.2.1 Output Mode

Figure 16-1 Output Mode Block Diagram



The output mode generates output signals according to TIMx_CR1[TxOCM], and the comparison results between TIMx_CNTR and registers TIMx_DR, TIMx_ARR. Meanwhile, corresponding interrupts events are generated.

16.2.1.1 Reading and Writing of TIMx_ARR/TIMx_DR

In output mode, TIMx_ARR/TIMx_DR contains preload registers and shadow registers. When the software writes TIMx_ARR/TIMx_DR register, the data is saved in the preload register. When the overflow event TIMx_SR[TxIF] is generated or basic counter stops working (TIMx_CR1[TxEN] = 0), the set value is transferred to the shadow register.

For example, TIMx_DR is a preload register and DR_SH is a shadow register. PWM is generated by comparing TIMx_CNTR with DR_SH. When software writes TIMx_DR, the register value is not immediately

updated to DR_SH, instead, the update occurs at the end of a PWM cycle (TIMx_CNTR overflow event).

16.2.1.2 High-/Low-level Output Mode

When TIMx_CR1[TxOCM] = 0, if TIMx_DR > TIMx_ARR, the output signal is always low. When TIMx_CR1[TxOCM] = 1, if TIMx_DR > TIMx_ARR, the output signal is always high.

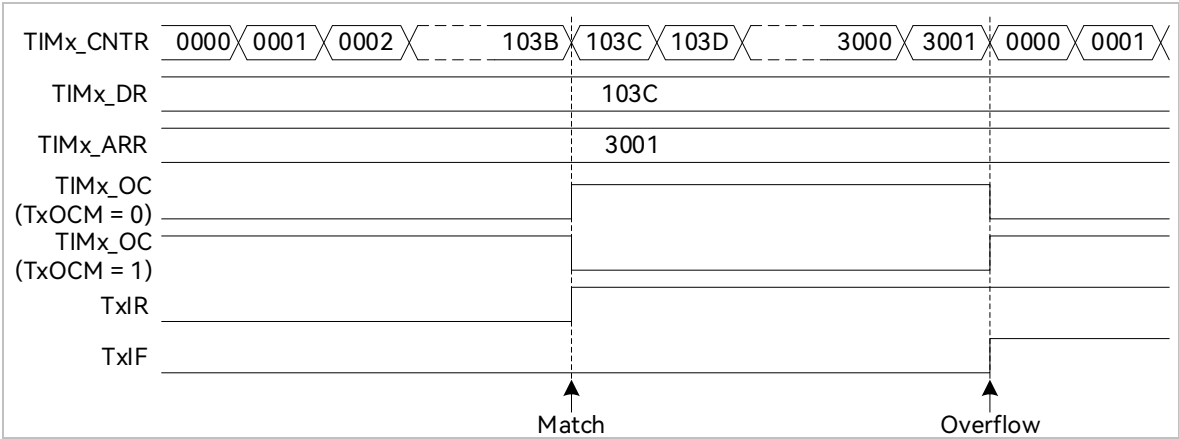
16.2.1.3 PWM Generation

In PWM generation mode, TIMx_ARR determines PWM cycle, TIMx_DR determines duty cycle, and duty cycle = TIMx_DR/TIMx_ARR*100%. If TIMx_CR1[TxOCM] = 0, the low level is output when TIMx_CNTR < TIMx_DR, and the high level is output when TIMx_CNTR ≥ TIMx_DR. If TIMx_CR1[TxOCM] = 1, the high level is output when TIMx_CNTR < TIMx_DR, and the low level is output when TIMx_CNTR ≥ TIMx_DR. When TIMx_CNTR is increased to TIMx_ARR, the output signal is reversed.

16.2.1.4 Interrupt Events

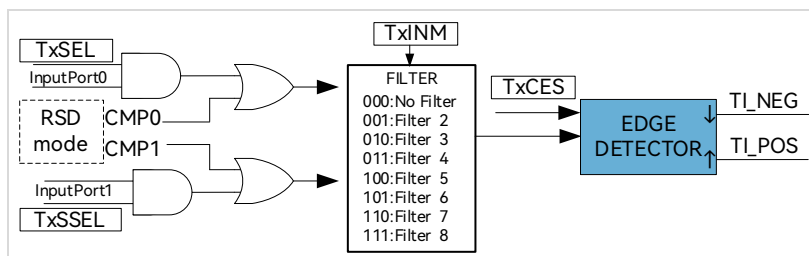
- > When TIMx_CNTR = TIMx_DR, a compare match event is generated and the interrupt flag bit TIMx_SR[TxIR] is set to “1”. The timer continues.
- > When TIMx_CNTR = TIMx_ARR, an overflow event is generated, and the interrupt flag bit TIMx_SR[TxIF] is set to “1”. The timer is cleared to “0” and then restarts.

Figure 16-2 Output Mode Waveform



16.2.2 Input Signal Filtering and Edge Detection

Figure 16-3 Block Diagram of Input Signal Filtering and Edge Detection



Input pins of the Timer 2/5/6 is shown in Table 16-2 , set by PH_SEL[TxACT] and PH_SEL[TxBCT] (See section 25.3.13). The filter of input signal is optional.

Table 16-2 Input Pins and Configurations of Timer2/5/6

Timer	TxSEL		TxSSEL	
	Input Pin 0	Configuration Bit	Input Pin 1	Configuration Bit
Timer2	PA10	PH_SEL[T2ACT]	PA11	PH_SEL[T2BCT]
Timer5	PA13	PH_SEL[T5SEL] : PH_SEL[T5ACT] = 01	PA14	PH_SEL[T5SEL] : PH_SEL[T5BCT] = 01
	PA4	PH_SEL[T5SEL] : PH_SEL[T5ACT] = 11	PA5	PH_SEL[T5SEL] : PH_SEL[T5BCT] = 11
Timer6	PA7	PH_SEL[T6ACT] = 10	/	/
	PA3	PH_SEL[T6ACT1] = 11		

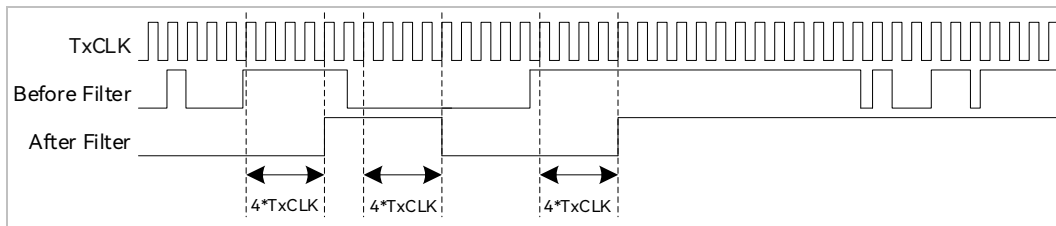
The filtering circuit does not filter out or remove input noise less than 2/3/4/5/6/7/8 clock cycles. The filtering period is selected by setting TIMx_CR0[TxINM]. The relationship between the number of clock cycles and TIMx_CR0[TxINM] is shown in Table 16-3.

Table 16-3 Mapping between Clock Cycles and TIMx_CR0[TxINM]

TIMx_CR0[TxINM]	Clock Cycle	TIMx_CR0[TxINM]	Clock Cycle
000	0	100	5
001	2	101	6
010	3	110	7
011	4	111	8

The filtered signal delays by the corresponding clock cycles compared with the signal before filtering. TIMx_CR0[TxCES] determines the active edge to count. The timing diagram of filter module with 4 clock cycles is shown in Figure 16-4.

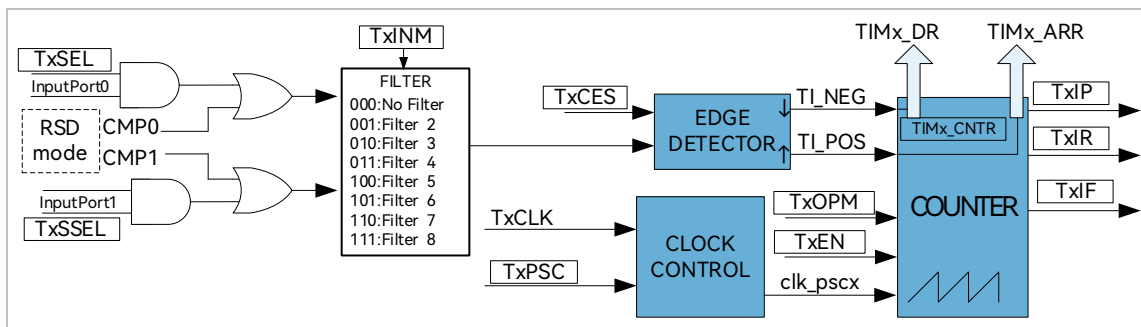
Figure 16-4 Timing Diagram of Filter Module



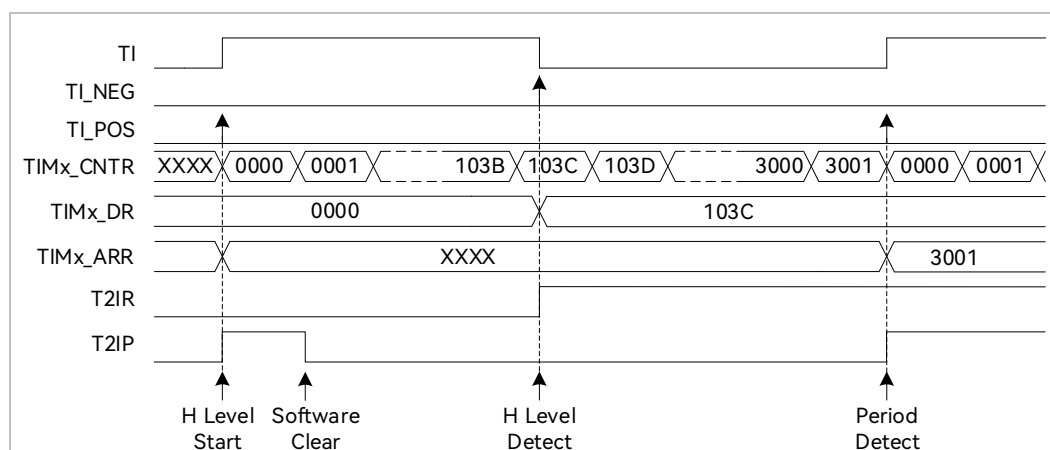
The edge detection module detects filtered input signals and records rising edge and falling edge for input capture mode or input counting modes.

16.2.3 Input Capture Mode

Figure 16-5 Schematic Diagram of Input Capture Mode



The input capture mode detects duty cycle and period of the PWM signal. When $TIMx\_CR0[TxCES] = 0$, the time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). When $TIM\_CR0[TxCES] = 1$, the time between two adjacent falling edges forms one cycle, and the time from falling edge to rising edge forms the pulse width (LOW). When the predefined edge arrives, the count value $TIMx\_CNTR$ is stored in $TIMx\_DR$ and $TIMx\_ARR$ respectively to calculate the period and duty cycle of PWM waveform.

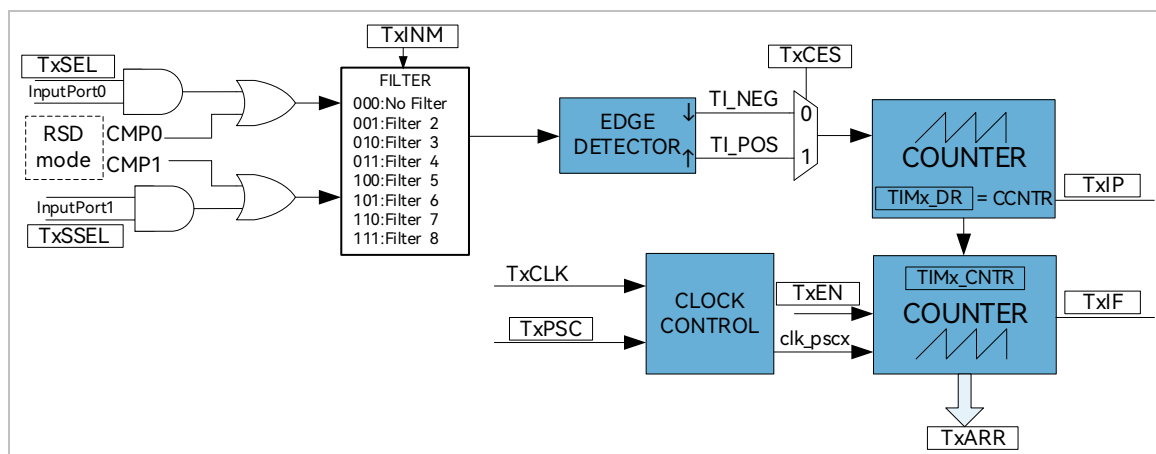
Figure 16-6 Timing Diagram of Input Capture Mode ($TIMx\_CR0[TxCES] = 0$)

For example, when $TIMx\_CR1[TxOCM] = 0$, $TIMx\_CR1[TxEN]$ is set to “1” to enable the basic counter. When the first rising edge of the input (falling edge is invalid) is detected, $TIMx\_CNTR$ is cleared and restarts. When falling edge of the input is detected, the value of $TIMx\_CNTR$ is stored in $TIMx\_DR$, while the interrupt flag $TIMx\_SR[TxIR]$ is set to “1”, and $TIMx\_CNTR$ continues to count. When the second rising edge of input is detected, the value of $TIMx\_CNTR$ is stored in $TIMx\_ARR$. Meanwhile, the interrupt flag $TIMx\_SR[TxIP]$ is set to “1”, and $TIMx\_CNTR$ is cleared to “0” and restarts.

An overflow event occurs if the Timer2/5/6 does not detect the second rising edge of the input and $TIMx\_CNTR$ reaches 0xFFFF. In this case, the interrupt flag $TIMx\_SR[TxIF]$ is set to “1”, and $TIMx\_CNTR$ is cleared to “0” and restarts. At this point, $TIMx\_ARR$ value is 0xFFFF, and the $TIMx\_DR$ value is determined by the input level and $TIMx\_CR1[TxOCM]$ XOR.

16.2.4 Input Counter Mode

Figure 16-7 Schematic Diagram of Input Counter Mode

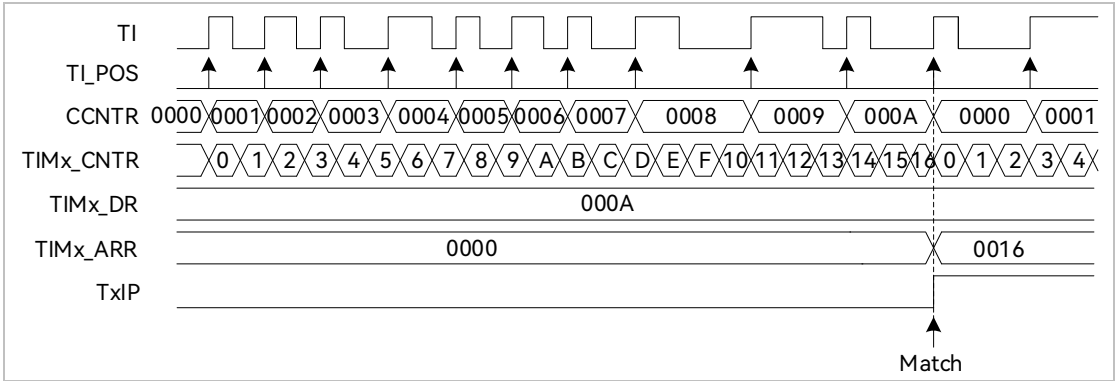


In input counter mode, $TIMx\_DR$ includes preload register and shadow register. When the software writes $TIMx\_DR$ register, the data is saved in the preload register first, and then sent to the shadow register in case of compare match event ($TIMx\_SR[TxIP] = 1$), overflow event ($TIMx\_SR[TxIF] = 1$) or special counter disable ($TIMx\_CR1[TxEN] = 0$).

The input counter mode is used to detect the time to input the set PWM wave. When the number of input PWM counted by the special counter CCNTR reaches the set value ($TIMx\_DR$), $TIMx\_CNTR$ is stored in $TIMx\_ARR$. When $TIMx\_CR0[TxCES]$ is set to “1”, the rising edge of the input PWM signal serves as the active counting edge of the special counter; when $TIMx\_CR0[TxCES]$ is set to “0”, the falling edge of the

input signal as the active edge.

Figure 16-8 Timing Diagram of Input Counter Mode

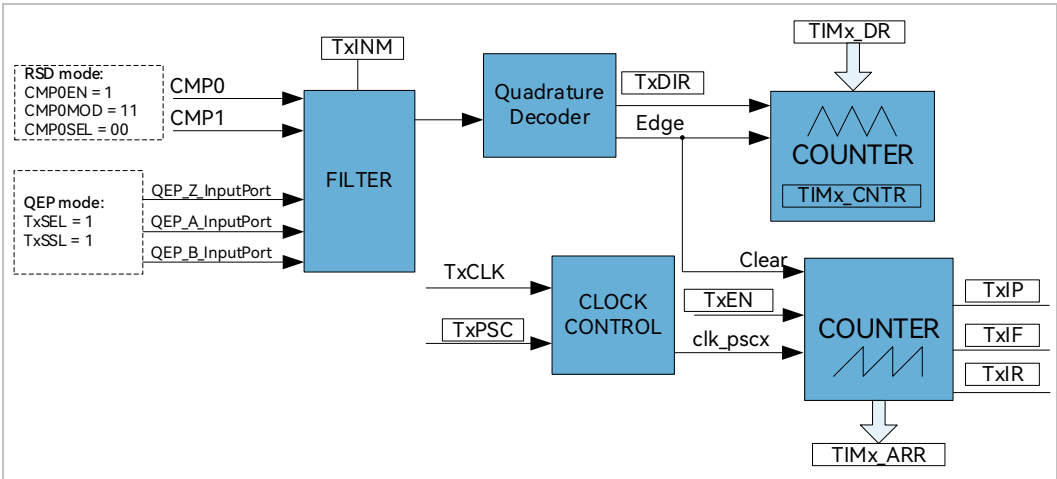


The basic counter is enabled when TIMx_CR1[TxEN] is set to “1”. If the first active edge of the input signal is detected, TIMx_CNTR is cleared to “0” and restarts. Whenever active edge of the input signal arrives, one is added to the count value of the special counter CCNTR. When the count value reaches TIMx_DR, TIMx_CNTR is stored in TIMx_ARR. When TIMx_SR[TxIP] is set to “1”, TIMx_CNTR and CCNTR are cleared to “0” and restart.

When the number of input PWM does not reach the set value and TIMx_CNTR reaches 0xFFFF, an overflow event generates, and the interrupt flag TIMx_SR[TxIF] is set to “1”. TIMx_CNTR is cleared to “0” with CCNTR uncleared. TIMx_CNTR starts counting from 0, and CCNTR continues counting with the previous value.

16.2.5 QEP Input Mode & RSD Mode

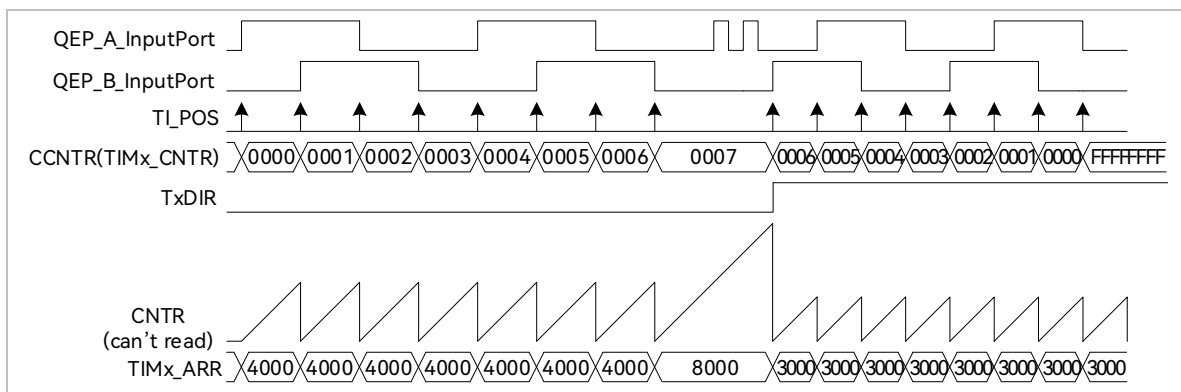
Figure 16-9 Schematic Diagram of QEP Input Mode & RSD Mode



QEP input Mode & RSD mode obtains relative position, direction and speed of the motor by detecting

orthogonal signals on two channels. The port A and port B (QEP input mode) or CMP0, CMP1 (RSD mode) are the input signal sources, which are sent to the quadrature decoding module from the filtering module to obtain active edge and direction (TIMx_CR1[TxDIR]).

Figure 16-10 Timing Diagram of QEP Input & RSD Mode



The special counter is an up/down counter, and the signal source is the active edge from orthogonal decoding module. If TIMx_CR1[TxDIR] = 0, the direction is positive, and the special counter counts upward. When the active edge arrives, the counter increases by one. If TIMx_CR1[TxDIR] = 1, the direction is reverse and the special counter counts down. When the active edge arrives, the counter decreases by one. In QEP Input Mode, after configuring the code value held in TIMx_DR, the count-up counter is cleared to “0” and restarts when it reaches TIMx_DR, and the count-down counter is reloaded with TIMx_DR when it decrements up to 0. The mechanical zero signal (“Z signal”) of QEP encoder is input and generates the interrupt event flag TIMx_SR[TxIR]. The input pins of Timer2/5/6 for mechanical zero signal are shown as below.

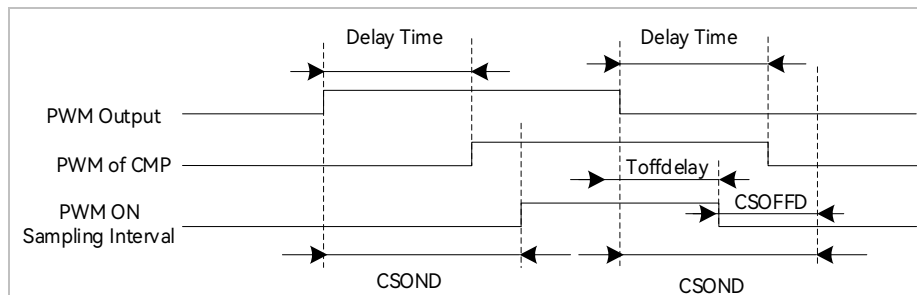
Table 16-4 Input Pins of Timer2/5/6 for Mechanical Zero Signal

Input Pins of Timer for Mechanical Zero Signal	
TIMER2_QEP_Z_InputPort	PA12
TIMER5_QEP_Z_InputPort	PA15
TIMER6_QEP_Z_InputPort	PD3

The basic counter is an up-counter used to record the time of two active counting edges. The clock source frequency can be divided. When the counting edge arrives, the value of the basic counter is stored in TIMx_ARR and cleared to “0”, and TIMx_SR[TxIP] interrupt flag bit is set to “1”. When the basic counter counts to 0xFFFF, the count overflows and the interrupt flag TIMx_SR[TxIF] is generated.

16.2.5.1 RSD Comparator Sampling

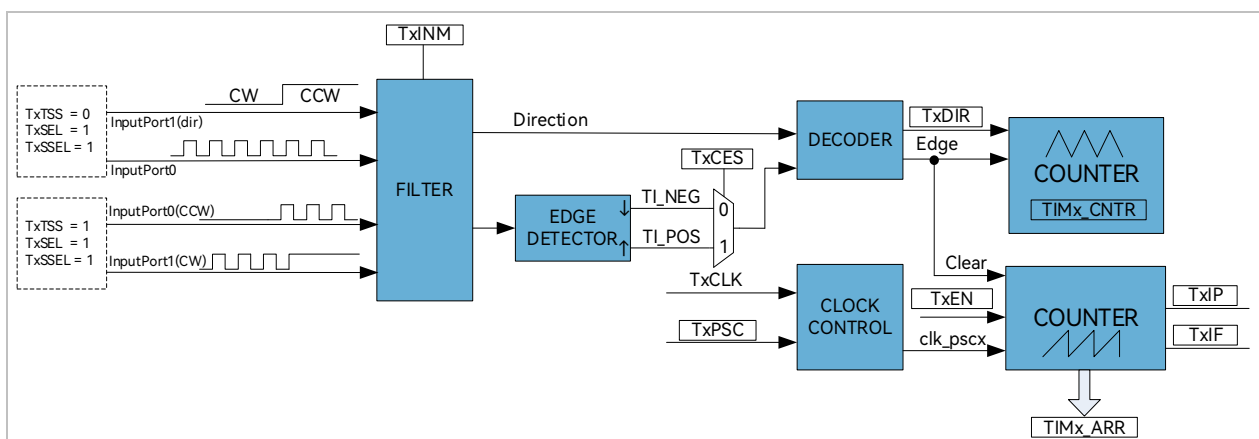
Figure 16-11 PWM ON Sampling Mode



The Start of Sampling (“SoS”) time delay and End of Sampling (“EoS”) time advance must be set in order to sample correct BEMF comparison signals in RSD Sampling mode. See section 33.1.9 for details.

16.2.6 Step Mode

Figure 16-12 Schematic Diagram of Step Mode



In step mode, relative position, direction and speed of the step motor are obtained by detecting inputs of the two channels. The direction input ports and pulse input ports are shown as below.

Table 16-5 Direction Input Pins and Pulse Input Pins of Timer 2/5/6

Timer	Direction Input Pin	Pulse Input Pin
Timer2	PA11	PA10
Timer5	PA14	PA13
	PA5	PA4

Setting TIMx_CR0[TxCES] to select the rising edge or falling edge as the active edge. The input signals are sent to decoding module from the filtering module to obtain the active edge and direction TIMx_CR1[TxDIR].



Note:

TIMx_CR1[TxDIR] changes only when direction input changes and active edge of pulse input arrives. External interrupt shall be applied if an interrupt is required when direction input changes.

Figure 16-13 Timing Diagram of Step Mode

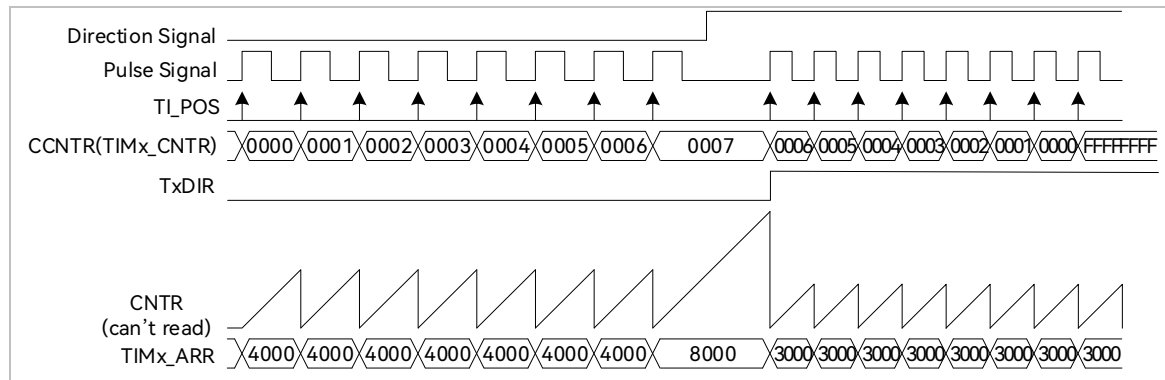
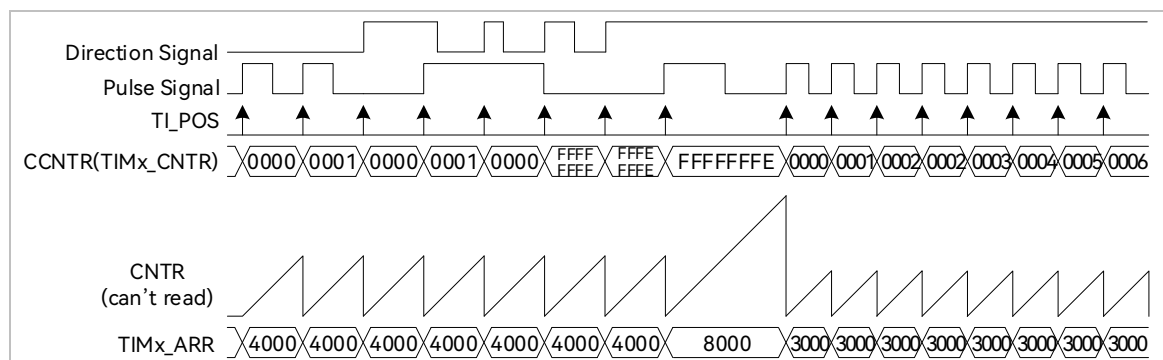


Figure 16-14 Timing Diagram of Positive + Negative Pulse Input State in Step Mode

(Raising Edge Selected as Active Edge)

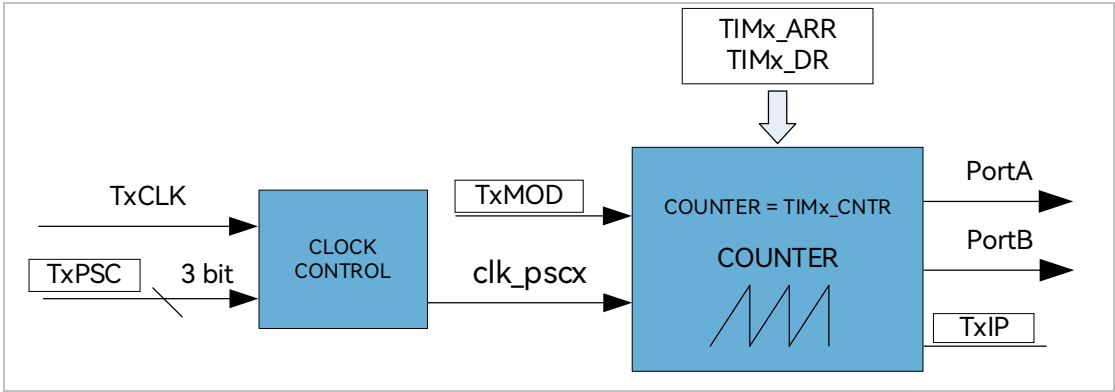


The special counter is an up/down counter, and the signal source is active edge of the encoding module. When the input signal = 0 and TIMx_CR1[TxDIR] = 0, the direction is forward. If active edge arrives, the special counter CCNTR increases by 1. When the input signal = 1 and TIMx_CR1[TxDIR] = 1, the direction is reverse. If active edge arrives, CCNTR decreases by 1. If count value of the special counter reaches 0xFFFFFFFF from 0, it is automatically cleared to "0". If it decreases from 0xFFFFFFFF to 0, it is automatically set to 0xFFFFFFFF. TIMx_CNTR is read to obtain the value of special counter.

The basic counter is an up counter, which uses the output of prescaler as the clock source to record the time between two active counting edges. When active counting edge arrives, the value of basic counter is stored in TIMx_ARR and then cleared to "0", and the interrupt flag bit TIMx_SR[TxIP] is set to "1". When basic counter counts to 0xFFFF, the count overflows and the interrupt flag (TIMx_SR[TxIF]) is set to "1".

16.2.7 QEP Output Mode

Figure 16-15 Schematic Diagram of QEP Output Mode



When TIMx_CR0[MOD] = 100, Timer2/5/6 operates in QEP output mode and generates orthogonal A and B signals with phase difference at 90°.

In QEP output mode, the value held by TIMx_ARR refers to the number of counts in one interrupt cycle and that held by TIMx_DR refers to the step value of signal A and B. The output frequency of QEP is determined by TIMx_DR and interrupt frequency. TIMx_CNTR indicates count value held in the basic counter. The basic counter counts with the step set by TIMx_DR, and generates an active edge of AB signals when it reaches the value set by TIMx_ARR. In this case, the interrupt event flag bit TIMx_SR[TxIP] is set to “1”, and the counter is cleared to “0” and restarts.

16.3 Timer2/5/6 Registers

16.3.1 TIMx_CR0 (CSR: 0x210/0x240/0x250) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																					TxINM			TxPSC			TxCES	TxDIRIN	TxMOD		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:11]	RSV	Reserved
[10:8]	TxINM	Input Signal Filtering Pulse Width Selection Input signals are filtered as noise if pulse width is less than the defined value. If the system clock runs at 48MHz(20.834ns):

		000: Input signals are not filtered 001: Input signals are filtered on every 2 clock cycles 010: Input signals are filtered on every 3 clock cycles 011: Input signals are filtered on every 4 clock cycles 100: Input signals are filtered on every 5 clock cycles 101: Input signals are filtered on every 6 clock cycles 110: Input signals are filtered on every 7 clock cycles 111: Input signals are filtered on every 8 clock cycles
[7:5]	TxPSC	Counter Clock Source Frequency Selection This bit is configured to divide the system clock as the clock source for basic counter. The clock source frequency is: 000: 48MHz 001: 24MHz 010: 12MHz 011: 6MHz 100: 3MHz 101: 1.5MHz 110: 750kHz 111: 375kHz
[4]	TxCES	Output Mode: No effect Input Capture Mode: Counting Edge Selection 0: The time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). 1: The time between two adjacent falling edges forms one cycle, and the time from falling edge to raising edge forms the pulse width (LOW). Input Counter Mode: Active Edge Selection 0: Falling Edge Count 1: Raising Edge Count QEP Input Mode & RSD Mode: Enable Pulse Counter Cleared upon Z Signal Interrupt EXTI1 0: Disable 1: Enable Step Mode: Active Edge Selection 0: Falling Edge Count 1: Raising Edge Count
[3]	TxDIRIN	Polarity Selection of Direction Input Signal in Step Mode 0: Forward direction is input when low level is applied, and reverse direction is input when high level is applied. 1: Reverse direction is input when low level is applied, and forward direction is input when high level is applied.
[2:0]	TxMOD	Mode Selection 000: Input Capture Mode 001: Output Mode

010: Input Counter Mode
 011: QEP Input Mode & RSD Mode or Step Mode
 100: QEP Output Mode

16.3.2 TIMx_CR1 (CSR: 0x211/0x241/0x251) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0									
RSV																							Tx_CNTR_CLR_EN		TxOPM		TxQEP_IN_CNTR_CLR		TxZ_EDGE_SEL		TxSS		RSV		TxOCM		Tx_DIR_R		TxEN	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	0	0	0									

Bit	Name	Description
[31:9]	RSV	Reserved
[8]	Tx_CNTR_CLR_EN	QEP Output Mode: TIMx_CNTR is updated with TIMx_DR 0: TIMx_CNTR is updated with TIMx_DR upon each master clock cycle 1: TIMx_CNTR is updated with TIMx_DR upon Driver1 carrier interrupt
[7]	TxOPM	Single Mode
[6]	TxQEP_IN_CNTR_CLR	QEP Input Mode: This bit decides whether TIMx_CNTR is cleared to “0” when active edge of Z input signal is detected. 0: TIMx_CNTR is not cleared to “0” 1: TIMx_CNTR is cleared to “0”
[5]	TxZ_EDGE_SEL	QEP Input Mode: Active Edge Selection of Z signal 0: Z signal is valid on the rising edge. 1: Z signal is valid on the falling edge. QEP Output Mode: Polarity Selection of Z signal 0: Active high 1: Active low
[4]	TxSS	Dual Pulse Enable in Step Mode 0: Disable 1: Enable
[3]	RSV	Reserved
[2]	TxOCM	Output Mode: Output Mode Selection 0: “0” is output when TIMx_CNTR < TIMx_DR, and “1” is output when TIMx_CNTR ≥ TIMx_DR

		1: “1” is output when TIMx_CNTR < TIMx_DR, and “0” is output when TIMx_CNTR ≥ TIMx_DR Input Counter Mode: No effect Input Capture Mode: TIMx_DR indicates the input level to be selected when TIMx_CNTR becomes overflowed. 0: TIMx_DR is reset to “0” by hardware for low level input upon an overflow interrupt and is set to “0xFFFF” for high level input upon an overflow interrupt. 1: TIMx_DR is reset to “0” by hardware for high level input upon an overflow interrupt and is set to “0xFFFF” for low level output upon an overflow interrupt. QEP Input Mode & RSD Mode and Step Mode Selection 0: QEP Input Mode & RSD Mode 1: Step Mode
[1]	Tx_DIR_R	QEP&RSD Mode: Indicator of Motor Rotation Direction Rotation direction of the motor is determined according to the phase relationship of the two input signals. Step Mode: Indicator of Motor Rotation Direction Rotation direction of the motor is determined according to the direction signal. 0: Forward 1: Backward
[0]	TxEN	Timer Enable 0: Disable 1: Enable

16.3.3 TIMx_IER (CSR: 0x212/0x242/0x252) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																											TxIRE	TxIPE	TxIFE		
																											rW	rW	rW		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	

Bit	Name	Description
[31:3]	RSV	Reserved
[2]	TxIRE	Output Mode: Match Interrupt Enable Input Capture Mode: Pulse Width Detection Interrupt Enable

		Input Counter Mode: No effect RSD Mode: Direction Change Interrupt Enable QEP Input Mode: QEP Encoder Z Signal Interrupt Enable Step Mode: Direction Change Interrupt Enable 0: Disable 1: Enable
[1]	TxIPE	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Enable Input Counter Mode: PWM Input Counter Match Interrupt Enable QEP Output Mode: A and B Signal Interrupt Enable 0: Disable 1: Enable
[0]	TxIFE	Output Mode: Basic Counter Overflow Interrupt Enable Input Capture Mode: Basic Counter Overflow Interrupt Enable Input Counter Mode: Basic Counter Overflow Interrupt Enable 0: Disable 1: Enable

16.3.4 TIMx_SR (CSR: 0x213/0x243/0x253) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																													TxIR	TxIP	TxF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

Bit	Name	Description
[31:3]	RSV	Reserved
[2]	TxIR	Output Mode: Match Interrupt Flag Input Capture Mode: Pulse Width Detection Interrupt Flag Input Counter Mode: No effect QEP Input Mode: QEP Encoder Z Signal Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to "0" 1: No effect

[1]	TxIP	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Flag Input Counter Mode: PWM Input Counter Match Interrupt Flag QEP Input Mode & RSD Mode or Step Mode: Input Active Edge Detection Interrupt Flag QEP Output Mode: A and B Signal Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	TxIF	Output Mode: Basic Counter Overflow Interrupt Flag, which is set to “1” when TIMx_CNTR matches TIMx_ARR. Input Capture Mode: Basic Counter Overflow Interrupt Flag, which is set to “1” when the counter does not detect an input PWM cycle but TIMx_CNTR reaches 0xFFFF. Input Counter Mode: Special Counter Overflow Interrupt Flag, which is set to “1” when the number of input PWM has not reached TIMx_DR but TIMx_CNTR already reaches 0xFFFF. QEP Input Mode & RSD Mode or Step Mode: Basic Counter Overflow Interrupt Flag, which is set to “1” when the counter reaches 0xFFFF. And then the counter is cleared to “0”. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

16.3.5 TIMx_CNTR (CSR: 0x214/0x244/0x254) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMx_CNTR																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	TIMx_CNTR	Output Mode/Input Capture Mode/Input Counter Mode: Count values held in Basic Counter QEP Input Mode & RSD Mode/Step Mode (32 bit): Count values held in the special counter, which is clear to “0” when active edge of the QEP Z input signal is detected and TIMx_CR1[TxQEP_IN_CNTR_CLR] is enabled.

16.3.6 TIMx_DR (CSR: 0x215/0x245/0x255) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMx_DR																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	TIMx_DR	Output Mode: Compare match values (written by software) Input Capture Mode: Count value of the detected input pulse width (written by hardware) Input Counter Mode: The number of the detected PWM (written by software) QEP Input Mode & RSD Mode (32 bit): Maximum count (written by software). The maximum value that TIMx_CNTR can reach. TIMx_CNTR resets to 0 when it counts up above this value, or resets to this maximum value when it counts down below 0. Step Mode: No effect QEP Output Mode: Step value of A and B signal coding (written by software). When TIMx_DR[15] is 0, A signal is led by 90° ahead of B signal, and when TIMx_DR[15] is 1, A signal is lagged by 90° behind B signal. All master clocks load a new TIMx_DR for calculation. If TIMx_CR1[TxQEP_IN_CNTR_CLR] is set to “1”, the new TIMx_DR is applied only when the carrier interrupt is detected.

16.3.7 TIMx_ARR (CSR: 0x216/0x246/0x256) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_ARR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_ARR	Output Mode: PWM cycle (written by software) Input Capture Mode: Count value by basic counter to detect one PWM cycle (written by hardware) Input Counter Mode: Count value by basic counter to input the detected PWM (written by hardware) QEP Input Mode & RSD Mode or Step Mode: Count value by basic counter to detect the input edge as the active edge (written by hardware) QEP output mode: Maximum value of A and B signal coding (written by software)

16.3.8 TIMx_QEP_MNUM (CSR: 0x217/0x247/0x257) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMx_QEP_MNUM																															
r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	TIMx_QEP_MNUM	QEP Input Mode: Value held by TIMx_QEP_CNTR when the carrier interrupt is detected QEP Output Mode: Count value to output the active edge

16.3.9 TIMx_QEP_TNUM (CSR: 0x218/0x248/0x258) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_QEP_TNUM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_QEP_TNUM	QEP Input Mode: Value held by TIMx_CNTR from the previous active edge to carrier interrupt QEP Output Mode: Count value based on the step set by TIMx_DR[15:0]

16.3.10 TIMx_QEP_TS_EMP (CSR: 0x219/0x249/0x259) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_QEP_TS_EMP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_QEP_TS_EMP	QEP Input Mode: Count value of carrier-free interrupt with no active edge between adjacent carrier interrupts

16.3.11 TIMx_QEP_CNTR (CSR: 0x21A/0x24A/0x25A) (x=2/5/6)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMx_QEP_CNTR																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	TIMx_QEP_CNTR	QEP Input Mode: Count value of the timer when an active edge is input QEP Output Mode: Count value of the timer when an active edge is output

16.3.12 TIMx_QEP_ARR (CSR: 0x21B/0x24B/0x25B) (x=2/5/6)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
TIMx_QEP_ARR																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	TIMx_QEP_ARR	QEP Input Mode: Value held by TIMx_CNTR upon the active edge of the Z signal QEP Output Mode: When TIMx_QEP_CNTR = {TIMx_QEP_ARR[29:0]-1, 2'b11}, TIMx_QEP_CNTR is cleared to “0” and a Z pulse is generated. If TIMx_QEP_ARR[29:0] is equal to 0, the Z pulse produces a fixed level and the polarity is set by TIMx_CR1[TxZ_EDGE_SEL].

16.3.13 TIM2_CR2 (CSR: 0x21C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										T2B_EDGE_SEL	T2A_EDGE_SEL	T2_Z_SEL		T2_AB_SEL	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	T2B_EDGE_SEL	QEP B Output Polarity Selection 0: The initial level is low. 1: The initial level is high.
[4]	T2A_EDGE_SEL	QEP A Output Polarity Selection 0: The initial level is low. 1: The initial level is high.
[3:2]	T2_Z_SEL	QEP Z Output Selection 00: Timer2 Output 01: Timer5 Input (unprocessed) 10: Timer6 Input (unprocessed)
[1:0]	T2_AB_SEL	QEP AB Output Selection 00: Timer2 Output 01: Timer5 Input (unprocessed) 10: Timer6 Input (unprocessed)

16.3.14 TIM5_CR2 (CSR: 0x24C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										T5B_EDGE_SEL	T5A_EDGE_SEL	T5_Z_SEL		T5_AB_SEL	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	T5B_EDGE_SEL	QEP B Output Polarity Selection 0: The initial level is low. 1: The initial level is high.
[4]	T5A_EDGE_SEL	QEP A Output Polarity Selection 0: The initial level is low. 1: The initial level is high.
[3:2]	T5_Z_SEL	QEP Z Output Selection 00: Timer5 Output 01: Timer2 Input (unprocessed) 10: Timer6 Input (unprocessed)
[1:0]	T5_AB_SEL	QEP AB Output Selection 00: Timer5 Output 01: Timer2 Input (unprocessed) 10: Timer6 Input (unprocessed)

17 Timer3/4/7/8

17.1 Timer3/4/7/8 Instructions

Timer3/Timer4/Timer7/Timer8 supports output and input modes:

- > Output mode: Generate PWM
- > Input capture mode: Detect the duration of high and low level of input PWM, which can be used to calculate PWM duty cycle

Timer3/Timer4/Timer7/Timer8 has the following features:

- > 3-bit programmable prescaler divides system clock as the clock source for basic counter (clock source of Timer3/Timer8 can be doubled to $2 * \text{TxCLK}$ in input capture mode)
- > 16-bit up-counting basic counter. Counting clock source serves as the output of prescaler
- > Input signal filtering
- > Input signal edge detection
- > Output PWM signal, single compare output
- > Interrupt event

17.1.1 Prescaler

Prescaler divides the system clock frequency and generates counter clock source for Basic Counter. 8 frequency division coefficients of prescaler are available and can be selected by $\text{TIMx\_CR0}[\text{TxPSC}]$. Since this register has no buffer, the clock source frequency is updated immediately after $\text{TIMx\_CR0}[\text{TxPSC}]$ is written. Therefore, the frequency division coefficients shall be configured when Basic Counter is not working. The clock source frequency formula is: $\text{clk\_psc} = \text{TxCLK}/(2^{\text{TxPSC}})$. The clock rate corresponding to different $\text{TIMx\_CR0}[\text{TxPSC}]$ value as shown in Table 17-1.

Table 17-1 Mapping between Clock Rate and $\text{TIMx\_CR0}[\text{TxPSC}]$

$\text{TIMx\_CR0}[\text{TxPSC}]$	Division Factor	$\text{TIMx\_CR0}[\text{TxPSC}]$	Division Factor
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128

**Note:**

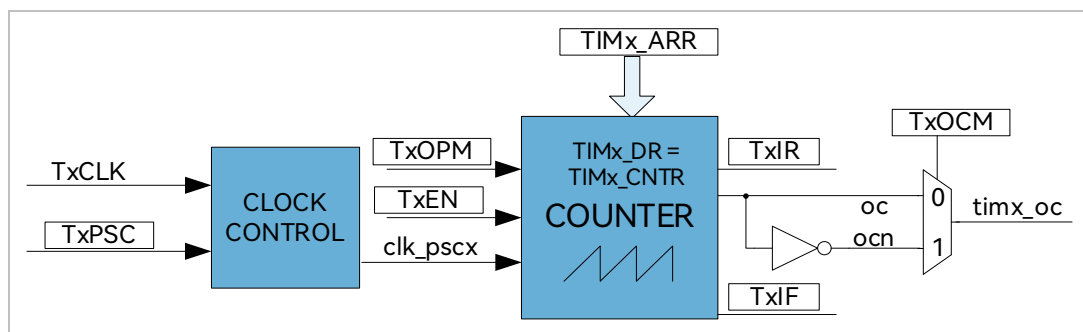
In Input Capture Mode of Timer3/Timer8, the clock rate is $2 * \text{TxCLK}$ when $\text{TIM3\_CR0}[T3PSC] = 111$ and $\text{TIM8\_CR0}[T8PSC] = 111$.

17.1.2 Reading, Writing and Counting of TIMx_CNTR

TIMx_CNTR starts when $\text{TIMx\_CR1}[TxEN] = 1$. The write operation to TIMx_CNTR directly changes the value of the register, so it is required to disable the counter before the write operation.

17.1.3 Output Mode

Figure 17-1 Output Mode Block Diagram



The output mode generate output signals according to $\text{TIMx\_CR0}[TxOCM]$, and the comparison results between TIMx_CNTR and registers TIMx_DR, TIMx_ARR. Meanwhile, corresponding interrupts is generated.

17.1.3.1 High-/Low-level Output Mode

When $\text{TIMx\_CR0}[TxOCM] = 0$ and $\text{TIMx\_DR} > \text{TIMx\_ARR}$, the output signals are always low. When $\text{TIMx\_CR0}[TxOCM] = 1$ and $\text{TIMx\_DR} > \text{TIMx\_ARR}$, the output signals are always high.

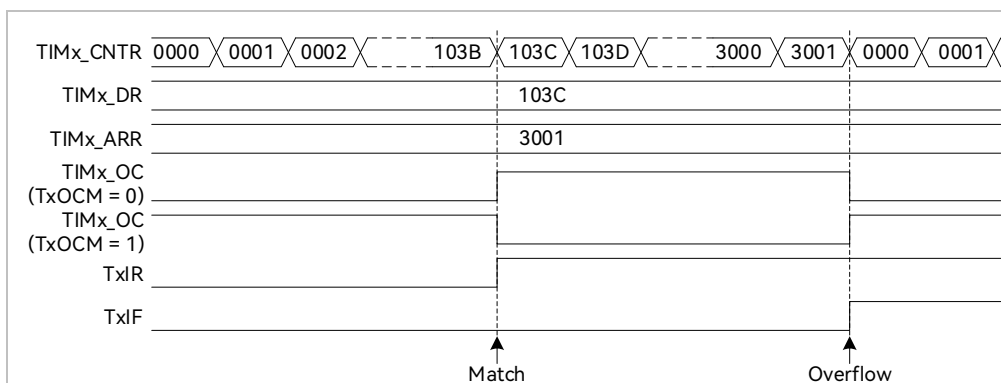
17.1.3.2 PWM Generation

In PWM generation mode, TIMx_ARR determines PWM cycle, and TIMx_DR determines the duty cycle, and $\text{duty cycle} = \text{TIMx\_DR} / \text{TIMx\_ARR} * 100\%$. If $\text{TIMx\_CR0}[TxOCM] = 0$, the low level is output when $\text{TIMx\_CNTR} < \text{TIMx\_DR}$, and the high level is output when $\text{TIMx\_CNTR} \geq \text{TIMx\_DR}$. If $\text{TIMx\_CR0}[TxOCM] = 1$, the high level is output when $\text{TIMx\_CNTR} < \text{TIMx\_DR}$, and low level is output when $\text{TIMx\_CNTR} \geq \text{TIMx\_DR}$. When $\text{TIMx\_CNTR} > \text{TIMx\_ARR}$, the output signal is reversed.

17.1.3.3 Interrupt Events

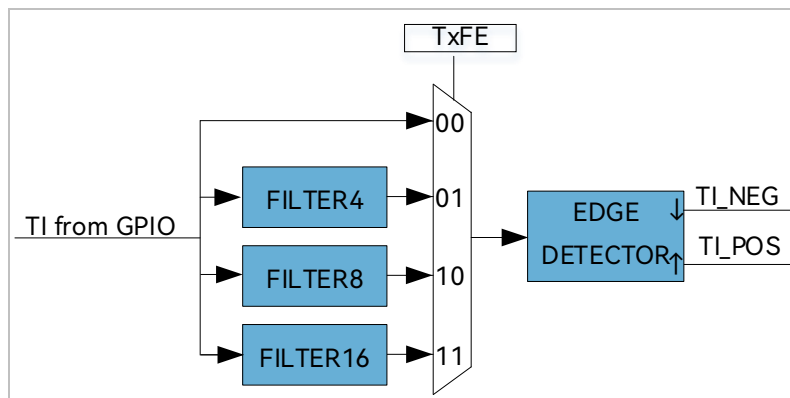
- When $TIMx\_CNTR = TIMx\_DR$, a compare match interrupt is generated. The interrupt flag $TIMx\_SR[TxIR]$ is set to “1”, and the counter continues.
- When $TIMx\_CNTR = TIMx\_ARR$, an overflow event is generated. The interrupt flag $TIMx\_SR[TxIF]$ is set to “1”, and the counter is cleared to “0”. $TIMx\_CR0[TxOPM]$ determines whether the counter recounts. The counter stops when $TIMx\_CR0[TxOPM]=1$, and restarts when $TIMx\_CR0[TxOPM]=0$.

Figure 17-2 Output Waveform of Output Mode



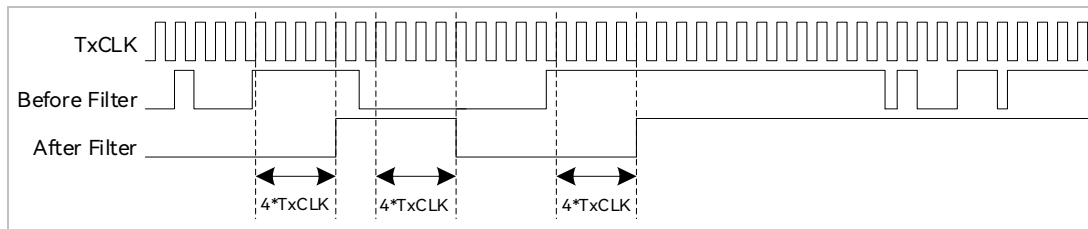
17.1.4 Input Signal Filtering and Edge Detection

Figure 17-3 Block Diagram of Input Signal Filtering and Edge Detection



The input signals of Timer3/4/7/8 come from GPIO pin. $TIMx\_CR0[TxFE]$ is configured to disable the filtering circuit or filter out the input noise below 4/8/16 system clock cycles. The filtered signal is 4/8/16 system clock cycles delayed than the signal before filtering.

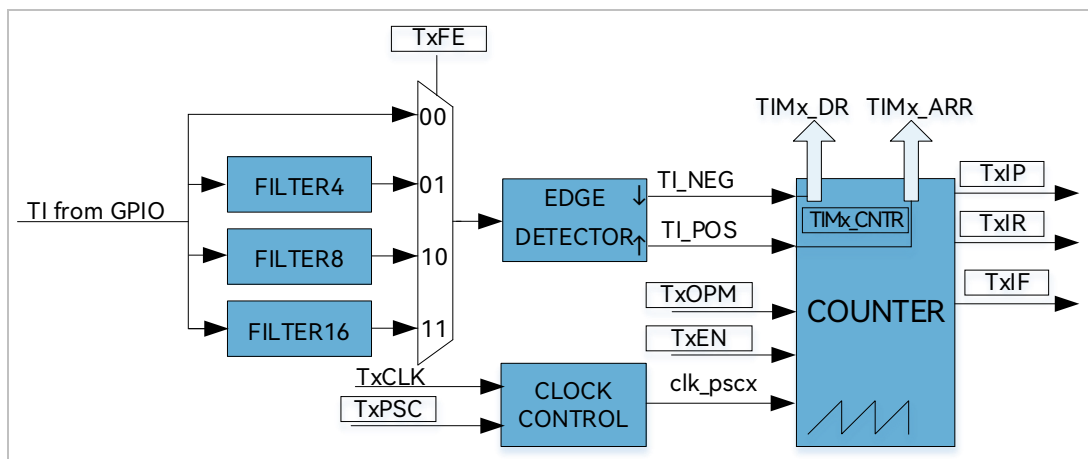
Figure 17-4 Timing Diagram of Filter Module



The edge detection module detects the filtered input signal from filtering module, and records the rising edge and falling edge for input capture mode.

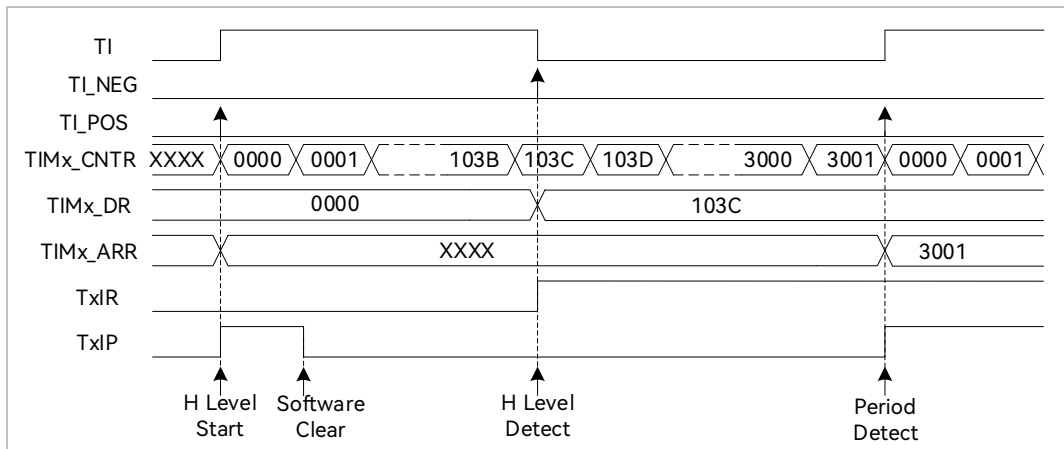
17.1.5 Input Capture Mode

Figure 17-5 Schematic Diagram of Input Capture Mode



The Input Capture Mode detects pulse width and waveform period of the input PWM signals. When $TIMx\_CR0[TxOCM] = 0$, the time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). When $TIMx\_CR0[TxOCM] = 1$, the time between two adjacent falling edges forms one cycle, and the time from falling edge to rising edge forms the pulse width (LOW). The pulse width and the period obtained by $TIMx\_CNTR$ are stored in $TIMx\_DR$ and $TIMx\_ARR$ respectively.

Figure 17-6 Timing Diagram of Input Capture Mode (TIMx_CR0[TxOCM] = 0)



For example, when TIMx_CR0[TxOCM]= 0, TIMx_CR1[TxEN] is set to “1” to enable the basic counter. The counter is cleared to “0” and restarts when the first rising edge is detected. When the falling edge is detected, the value of TIMx_CNTR is stored into TIMx_DR. Meanwhile, the interrupt flag TIMx_CR1[TxIR] is set to “1”, and TIMx_CNTR continues to count. When the second rising edge is detected, the value of TIMx_CNTR is saved into TIMx_ARR. The interrupt flag TIMx_SR[TxIP] is set to “1” and TIMx_CNTR is cleared to “0”. TIMx_CR0[TxOPM] determines whether the counter restarts. If TIMx_CR0[TxOPM] = 1, the counter stops; and if TIMx_CR0[TxOPM] = 0, it restarts.

An overflow event occurs if Timer3/4/7/8 does not detect the second rising edge of the input and TIMx_CNTR reaches 0xFFFF. In this case, the interrupt flag bit TIMx_SR[TxIF] is set to “1”, and TIMx_CNTR is cleared to “0”. TIMx_CR0[TxOPM] determines whether the counter restarts. If TIMx_CR0[TxOCM] = 1, the counter stops counting, and if TIMx_CR0[TxOPM] = 0, it restarts. At this point, TIMx_ARR is 0xFFFF, and TIMx_DR is determined by the input level and TIMx_CR0[TxOCM] XOR.

17.2 Timer3/4/7/8 Registers

17.2.1 TIMx_CR0 (CSR: 0x220/0x230/0x260/0x270) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								TxPSC		TxFE		TxOCM	TxOPM	TxMOD	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:5]	TxPSC	Basic Counter Clock Prescaler Selection It is configured to divide the system clock frequency and generate the clock source for Basic Counter. The prescaled clock rates are configured as follows: 000: TxCLK 001: TxCLK/2 010: TxCLK/4 011: TxCLK/8 100: TxCLK/16 101: TxCLK/32 110: TxCLK/64 111: TxCLK/128  Note: In Input Capture Mode of Timer3/Timer8, the clock rate is 2 * TxCLK when this bit is set to “111”.
[4:3]	TxFE	Input Signal Filtering Pulse Width Selection Input signals are filtered as noise if pulse width is less than the defined value. 00: Input signals are not filtered 01: Input signals are filtered on every 4 clock cycles 10: Input signals are filtered on every 8 clock cycles 11: Input signals are filtered on every 16 clock cycles
[2]	TxOCM	Output Mode: Output Mode Selection 0: “0” is output when TIMx_CNTR < TIMx_DR, and “1” is output when TIMx_CNTR ≥ TIMx_DR 1: “1” is output when TIMx_CNTR < TIMx_DR, and “0” is output when TIMx_CNTR ≥ TIMx_DR Input Capture Mode: TIMx_DR indicates the input level to be selected when the active edge is detected or the counter becomes overflowed. Active Edge Selection 0: The time between two adjacent rising edges forms one cycle, and the time from rising edge to falling edge forms the pulse width (HIGH). 1: The time between two adjacent falling edges forms one cycle, and the time from falling edge to raising edge forms the pulse width (LOW). TIMx_DR indicates the input level to be selected when the counter becomes overflowed.

		0: TIMx_DR is set to “0” by hardware for low level input upon an overflow interrupt and is set to “0xFFFF” by hardware for high level input upon an overflow interrupt. 1: TIMx_DR is set to “0” by hardware for high level input upon an overflow interrupt and is set to “0xFFFF” for low level input upon an overflow interrupt.
[1]	TxOPM	Single Mode Basic counter stops in any of the following events: Output Mode: Basic counter overflow event Input Capture Mode: PWM cycle detection or basic counter overflow event 0: Basic counter does not stop 1: Basic counter stops (TIMx_CR1[TxEN] reset to “0”)
[0]	TxMOD	Working Mode Selection 0: Input Capture Mode 1: Output Mode

17.2.2 TIMx_CR1 (CSR: 0x221/0x231/0x261/0x271) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																															TxEN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

Bit	Name	Description
[31:1]	RSV	Reserved
[0]	TxEN	Basic Counter Enable 0: Disable 1: Enable

17.2.3 TIMx_IER (CSR: 0x222/0x232/0x262/0x272) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV																															TxIRE	TxIPE	TxIFE
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0		

Bit	Name	Description
[31:3]	RSV	Reserved
[2]	TxIRE	Output Mode: Compare Match Interrupt Enable Input Capture Mode: Pulse Width Detection Interrupt Enable 0: Disable 1: Enable
[1]	TxIPE	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Enable 0: Disable 1: Enable
[0]	TxIFE	Output Mode: Basic Counter Overflow Interrupt Input Capture Mode: Basic Counter Overflow Interrupt Enable 0: Disable 1: Enable

17.2.4 TIMx_SR (CSR: 0x223/0x233/0x263/0x273) (x = 3/4/7/8)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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Bit	Name	Description
[31:3]	RSV	Reserved
[2]	TxIR	Output Mode: Match Interrupt Flag Input Capture Mode: Pulse Width Detection Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[1]	TxIP	Output Mode: No effect Input Capture Mode: PWM Cycle Detection Interrupt Flag Read:

		0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to "0" 1: No effect
[0]	TxIF	Output Mode: Basic Counter Overflow Interrupt Flag, which is set to "1" when TIMx_CNTR matches TIMx_ARR. Input Capture Mode: Basic Counter Overflow Interrupt Flag, which is set to "1" when the Counter does not detect an input PWM cycle but TIMx_CNTR reaches 0xFFFF. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to "0" 1: No effect

17.2.5 TIMx_CNTR (CSR: 0x224/0x234/0x264/0x274) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_CNTR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_CNTR	Count values held in Basic Counter

17.2.6 TIMx_DR (CSR: 0x225/0x235/0x265/0x275) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_DR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_DR	Output Mode: Compare match values Input Capture Mode: Count value of the detected input pulse width (written by hardware)

17.2.7 TIMx_ARR (CSR: 0x226/0x236/0x266/0x276) (x = 3/4/7/8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																TIMx_ARR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	TIMx_ARR	Output Mode: Reload value (written by software) Input Capture Mode: Count value of a detected PWM cycle (written by hardware)

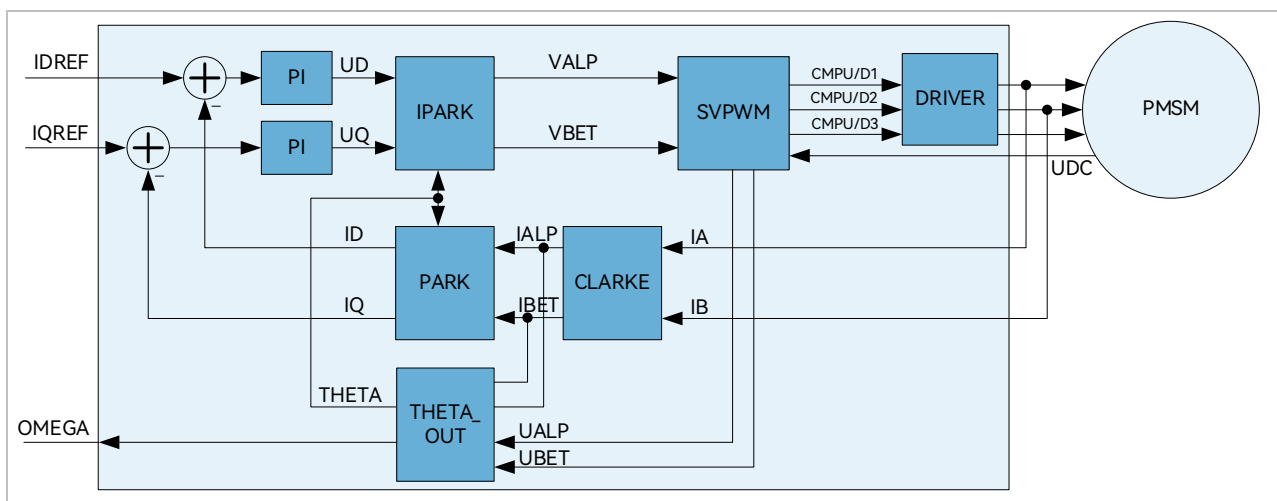
18 ME

18.1 ME Introduction

The ME (motor control engine) module is developed by Fortior, and is used in sensorless and sensed FOC motor drive applications and SVPWM-based motor control applications. The module contains two Driver controllers for independent control of two motors.

The ME module achieves FOC current close-loop control, including coordinate transform, PI control and SVPWM output. Its angle estimator uses the sampled motor current to estimate the rotor position and fulfills sensorless FOC-based motor control. MCU can also process the signals from the position sensor to implement sensed FOC-based control.

Figure 18-1 Block Diagram of ME Module



Moreover, the ME module also supports driver control, current-loop control (FOC), angle output, outer-loop control (FOC), ramping calculation, power calculation, field weakening, terminal voltage monitoring, UQ injection, CORDIC by software, angle fusion, current-loop decoupling, ME interrupt sources management, and high-speed voltage phase compensation.

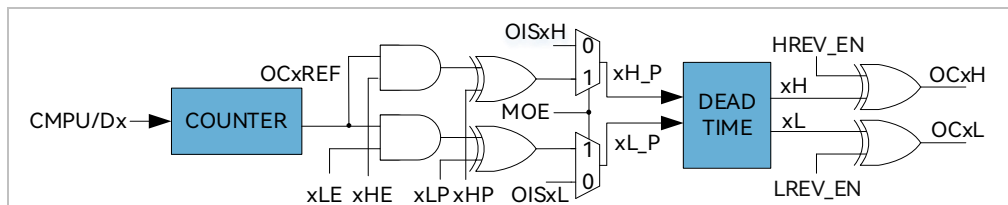
18.2 Driver Controller

18.2.1 FU7512Q1 Driver Controller

FU7512Q1 contains two driver controllers, Driver1 and Driver2. Driver1(2) can output three-phase PWM

signals according to the configurations of Driver1(2). The driver controller is used to generate PWM signals. It outputs 6-channel PWM signals based on the three-phase comparison value to turn on or turn off the high-side and low-side MOSFETs of U/V/W phases for motor control.

Figure 18-2 Block Diagram of FU7512Q1 Driver Controller



18.2.2 FU7564Q1 Driver Controller

FU7564Q1 contains two driver controllers: Driver1 and Driver2. Driver1 is mainly used for 6N pre-driver1 output. Its associated registers are accessed via the internal I²C2. For the register addresses and their functions, see Table 1-6 FU7564Q1/FU7574Q1 6N Pre-driverx Register Address Mapping and sections 18.17.1.1 SLPF_R (0x02) ~ 18.17.1.15 TVDW_R (0x8E). Driver2 is mainly used for PWM2 output.

18.2.2.1 FU7564Q1 6N Pre-driver1

FU7564Q1 6N pre-driver1 has the same functionality as FU7574Q1 6N pre-driverx. For details, see 18.2.4.1 FU7574Q1 6N Pre-driverx.

18.2.2.2 PWM2 Output

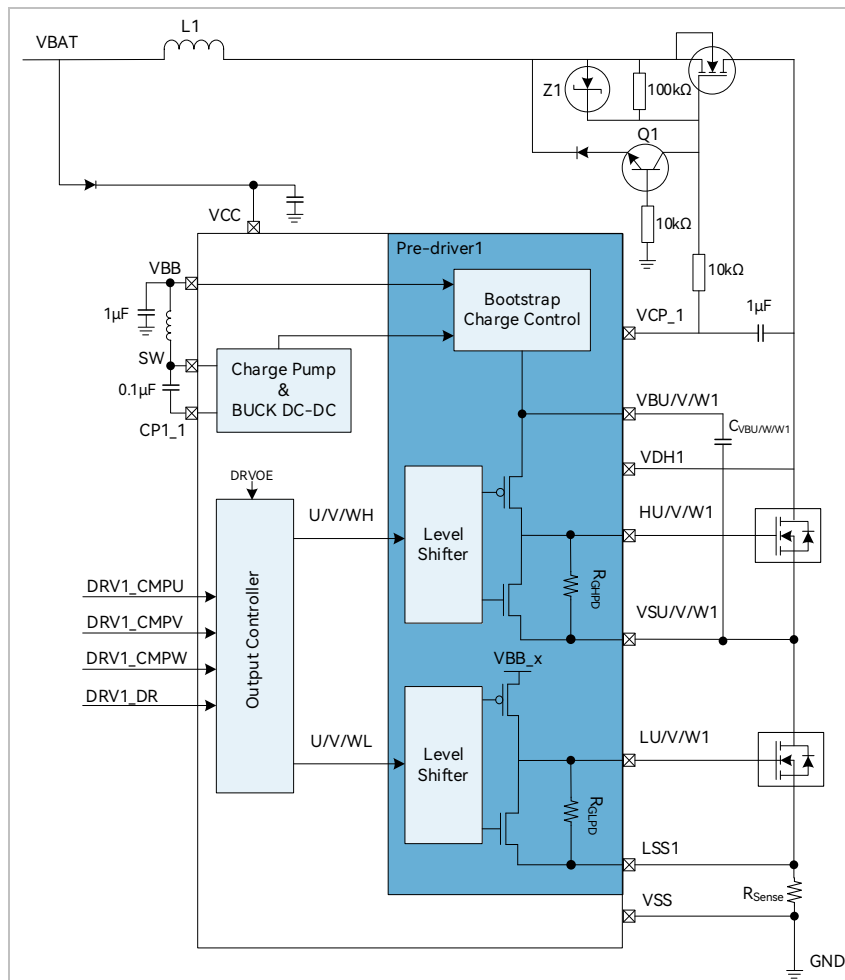
FU7564Q1 Driver2 is used to generate PWM2 signals. It outputs 3-channel PWM2 signals based on the three-phase comparison value to turn on or turn off the high-side and low-side MOSFETs of U/V/W phases for motor control.

18.2.3 FU7565Q1 Driver Controller

FU7565Q1 contains only one driver controller: Driver1. Driver1 is mainly used for 6N pre-driver1 output. Its associated registers are accessed via the I²C2 inside the MCU. For the register addresses and their functions, see 1.5.5.3.2 FU7565Q1 6N Pre-driver1 Register Address Mapping and 18.17.2 FU7565Q1 6N Pre-driver1 Registers.

18.2.3.1 FU7565Q1 6N Pre-driver1

Figure 18-3 Block Diagram of FU7565Q1 6N Pre-driver1



The above figure shows the functional block diagram of the FU7565Q1 6N pre-driver1. DRV1_CMPU/V/W is the three-way comparison value output by FOC module, and DRV1_DR is the comparison value set by the software. The above comparison value outputs three sets of level signals U/V/W to pre-driver1 after passing through the output control module for BLDC motor control.

Configuring DRV1_CR[DRVOE] enables pre-driver1 mode, where the pre-driver1 output is wired to 6 NMOS respectively to drive U/V/W phase.

Table 18-1 Signal Truth Values of FU7565Q1 Built-in Pre-driver1

Input		Output	
UH/VH/WH	UL/VL/WL	HU/HV/HW	LU/LV/LW
L	L	L	L
L	H	L	H

Input		Output	
H	L	H	L
H	H	L	L

Table 18-2 Logic Truth Values of FU7565Q1 Built-in Pre-driver1

Sleep	T _{SD}	V _{CCOVP}	V _{CCUV}	V _{BBOV}	V _{BBOV}	V _{DD5UV}	H_DU/V/W	L_DU/V/W	HU/V/W	LU/V/W	V _{SU/V/W}
1	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	1	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	1	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	1	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	1	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	1	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	1	-	-	Low	Low	HiZ
0	0	0	0	0	0	0	0	0	Low	Low	HiZ
0	0	0	0	0	0	0	0	1	Low	High	Low
0	0	0	0	0	0	0	1	0	High	Low	High
0	0	0	0	0	0	0	1	1	Low	Low	HiZ



Note:

- > 1: Logic 1; Low: MOSFET off
- > 0: Logic 0; High: MOSFET on
- > -: Reserved
- > HiZ: High impedance; both MOSFETs off

Moreover, the 6N pre-driver1 also delivers high transient current to rapidly charge and discharge the gate capacitor of the external MOSFET to reduce dissipation during switching. The capacitor on VBB pin supplies current to charge the low-side driver and the bootstrap capacitor, while the bootstrap capacitor connected between VBU1/VBV1/VBW1 and VSU1/VSV1/VSW1 provide current to power the corresponding high-side drivers.

Other functions of FU7565Q1 6N pre-driver1 are identical to those of FU7574Q1 6N pre-driverx. For details, see 18.2.4.1.1 Bootstrap Power Supply ~ 18.2.4.3 Thermal Shutdown Protection.

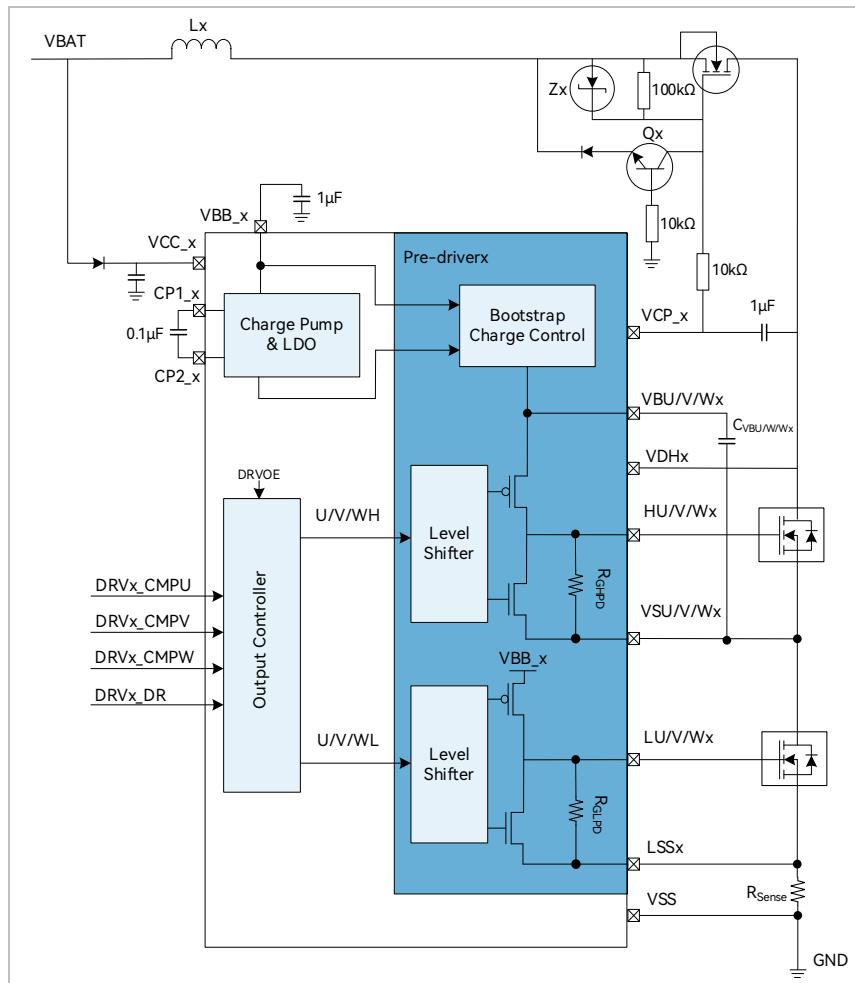
18.2.4 FU7574Q1 Driverx Controller

FU7574Q1 contains two driver controllers: Driver1 and Driver2, which are used for 6N pre-driver1 and 6N pre-driver2 outputs, respectively. 6N pre-driver1 registers are accessed via the I²C2 inside the MCU, while 6N pre-driver2 registers are accessed via the external I²C2. For the register addresses and their functions,

see Table 1-6 FU7564Q1/FU7574Q1 6N Pre-driverx Register Address Mapping and 18.17.1 FU7564Q1/FU7574Q1 6N Pre-driverx Registers.

18.2.4.1 FU7574Q1 6N Pre-driverx

Figure 18-4 Block Diagram of FU7574Q1 6N Pre-driverx



The above figure shows the functional block diagram of the FU7574Q1 6N Pre-driverx. DRVx_CMPU/V/W is the three-way comparison value output by FOC module, DRVx_DR is the comparison value set by the software. The above comparison value outputs three sets of level signals U/V/W to pre-driver after passing through the output control module for BLDC motor control.

Configuring DRVx_CR[DRVOE] enables pre-driverx mode, where the pre-driverx output is wired to 6 NMOS respectively to drive U/V/W phase.

Table 18-3 Signal Truth Values of FU7574Q1 Built-in Pre-driverx

Input		Output	
UH/VH/WH	UL/VL/WL	HU/HV/HW	LU/LV/LW
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

Table 18-4 Logic Truth Values of FU7574Q1 Built-in Pre-driverx

Sleep	T _{SD}	V _{CCOVP}	V _{CCUV}	V _{BBOV}	V _{BBOV}	V _{DD5UV}	H_DU/V/W	L_DU/V/W	HU/V/W	LU/V/W	V _{SU/V/W}
1	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	1	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	1	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	1	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	-	-	-	Low	Low	HiZ
-	-	-	-	1	-	-	-	-	Low	Low	HiZ
-	-	-	-	-	1	-	-	-	Low	Low	HiZ
-	-	-	-	-	-	1	-	-	Low	Low	HiZ
0	0	0	0	0	0	0	0	0	Low	Low	HiZ
0	0	0	0	0	0	0	0	1	Low	High	Low
0	0	0	0	0	0	0	1	0	High	Low	High
0	0	0	0	0	0	0	1	1	Low	Low	HiZ



Note:

- > 1: Logic 1; Low: MOSFET off
- > 0: Logic 0; High: MOSFET on
- > -: Reserved
- > HiZ: High impedance; both MOSFETs off

Moreover, the 6N pre-driverx also delivers high transient current to rapidly charge and discharge the gate capacitor of the external MOSFET to reduce dissipation during switching. The capacitor on VBB_x pin supplies current to recharge the low-side driver and the bootstrap capacitor, while the bootstrap capacitor connected between VBUx/VBVx/VBWx and VSUx/VSVx/VSWx provides current to power the corresponding high-side driver, one per phase.

18.2.4.1.1 Bootstrap Power Supply

When the high-side 6N pre-driverx activates, its reference voltage rises to near the bridge supply voltage. To enable high-side conduction, the bootstrap circuit must generate a voltage that exceeds the bridge supply voltage. This temporary high-side power is supplied by a dedicated bootstrap capacitor for each

high-side channel, connected between the bootstrap supply pin (VBU_x, VBV_x, VBW_x) and the reference pin (VSU_x, VSV_x, VSW_x).

When the reference pin VSU_x/VSV_x/VSW_x is at a low level, the bootstrap capacitor is independently charged to VBB_x voltage. As its output level rises, the voltage at the bootstrap supply pin (VB_x) follows, delivering the gate voltage required for the high-side N-channel MOSFET. The internal charge pump (VCP_x) recharges the bootstrap capacitor when necessary. This ensures sufficient bootstrap capacitor voltage for reliable operation of external MOSFETs across all conditions (duty cycle from 0% to 100%), and simplifies the design in motor control applications especially those with block commutation solutions.

18.2.4.1.2 Bootstrap Charging Management

FU7574Q1 6N pre-driver_x monitors bootstrap capacitor voltages to ensure reliable high-side switch operation. It also integrates an optional bootstrap capacitor charging management system (Boot Manager) that ensures sufficient capacitor charge under all conditions. This feature is critical for systems requiring control processor authorization for MOSFET switching.

When the PWM duty cycle is very high—particularly when the on-time exceeds 2 μs—the bootstrap charging management circuit automatically charges the bootstrap capacitor at regular intervals via the charge pump VCP_x.

Additionally, the bootstrap charging management circuit integrates under-voltage and over-voltage protection for the bootstrap capacitors. See 18.2.4.2.3 Bootstrap Capacitor UVLO and OVP.

18.2.4.1.3 High-side Gate Drive

The HU_x, HV_x, and HW_x pins deliver gate drive signals from the external high-side N-channel MOSFETs. When H_{Dx} = 1 (high), the upper driver section activates, sourcing current from its drain to the MOSFET gate to turn it on. When H_{Dx} = 0 (low), the lower driver section activates, sinking current through its drain to VSU_x/VSV_x/VSW_x pin to turn it off.

The VSU_x, VSV_x, and VSW_x serve as reference pins for the high-side gate driver. These pins connect to the load to sense its voltage, and to the negative terminal of bootstrap capacitors to act as the negative supply reference for the floating high-side drivers. In addition, they provide a return path to discharge high-side MOSFET gate capacitor and connect to the MOSFET bridge with low impedance.

18.2.4.1.4 Low-side Gate Drive

The LUX, LVx, and LWx pins deliver gate drive signals from the external low-side N-channel MOSFETs, and are referenced to LSSx pin. When L_Dx = 1 (high), the upper driver section activates, sourcing current from its drain to the MOSFET gate to turn it on. When L_Dx = 0 (low), the lower driver section activates, sinking current through its drain to LSSx pin to turn it off. LSSx pin provides a return path to discharge low-side MOSFET gate capacitor and connect to the low-side MOSFET source with low impedance.

18.2.4.1.5 MOSFET V_{DS} OVP

FU7574Q1 6N pre-driverx monitors the drain-source voltage (V_{DS}) of each MOSFET and compares it with the corresponding over-voltage thresholds to detect faults on the external MOSFETs.

The over-voltage thresholds are defined for high-side MOSFETs ($V_{DSTHU}/V_{DSTHV}/V_{DSTHW}$) and low-side MOSFETs ($V_{DSTLU}/V_{DSTLV}/V_{DSTLW}$). These thresholds are generated by internal DACs, which are configured via the register variables VTHU_R[5:0], VTHV_R[5:0], VTHW_R[5:0], VTLU_R[5:0], VTLV_R[5:0], and VTLW_R[5:0], respectively. These variables provide the input to two 6-bit DACs with a least significant bit (LSB) of typically 50mV.

Using the U-phase as an example, the over-voltage thresholds generated by the DAC output are defined approximately as follows (same for V and W phases):

$V_{DSTHU} = n * 50\text{mV}$, where n is a positive integer defined by VTHU_R[5:0];

$V_{DSTLU} = n * 50\text{mV}$, where n is a positive integer defined by VTLU_R[5:0].

Table 18-5 V_{DS} Over-voltage Thresholds (U-phase Example)

VTHU_R[5:0]、VTLU_R[5:0]						V_{DSTHU} (mV)	V_{DSTLU} (mV)
[5]	[4]	[3]	[2]	[1]	[0]		
-1600m	+800m	+400m	+200m	+100m	+50m		
0	0	0	0	0	0	1,600	1,600
0	0	0	0	0	1	1,650	1,650
0	0	0	0	1	0	1,700	1,700
0	0	0	0	1	1	1,750	1,750
0	0	0	1	0	0	1,800	1,800
0	0	0	1	0	1	1,850	1,850
0	0	0	1	1	0	1,900	1,900
0	0	0	1	1	1	1,950	1,950
0	0	1	0	0	0	2,000	2,000

VTHU_R[5:0]、VTLU_R[5:0]						V _{DSTHU} (mV)	V _{DSTLU} (mV)
[5]	[4]	[3]	[2]	[1]	[0]		
-1600m	+800m	+400m	+200m	+100m	+50m		
0	0	1	0	0	1	2,050	2,050
0	0	1	0	1	0	2,100	2,100
0	0	1	0	1	1	2,150	2,150
0	0	1	1	0	0	2,200	2,200
0	0	1	1	0	1	2,250	2,250
0	0	1	1	1	0	2,300	2,300
0	0	1	1	1	1	2,350	2,350
0	1	0	0	0	0	2,400	2,400
0	1	0	0	0	1	2,450	2,450
0	1	0	0	1	0	2,500	2,500
0	1	0	0	1	1	2,550	2,550
0	1	0	1	0	0	2,600	2,600
0	1	0	1	0	1	2,650	2,650
0	1	0	1	1	0	2,700	2,700
0	1	0	1	1	1	2,750	2,750
0	1	1	0	0	0	2,800	2,800
0	1	1	0	0	1	2,850	2,850
0	1	1	0	1	0	2,900	2,900
0	1	1	0	1	1	2,950	2,950
0	1	1	1	0	0	3,000	3,000
0	1	1	1	0	1	3,050	3,050
0	1	1	1	1	0	3,100	3,100
0	1	1	1	1	1	3,150	3,150
1	0	0	0	0	0	0	0
1	0	0	0	0	1	50	50
1	0	0	0	1	0	100	100
1	0	0	0	1	1	150	150
1	0	0	1	0	0	200	200
1	0	0	1	0	1	250	250
1	0	0	1	1	0	300	300
1	0	0	1	1	1	350	350
1	0	1	0	0	0	400	400
1	0	1	0	0	1	450	450
1	0	1	0	1	0	500	500
1	0	1	0	1	1	550	550
1	0	1	1	0	0	600	600
1	0	1	1	0	1	650	650
1	0	1	1	1	0	700	700
1	0	1	1	1	1	750	750

VTHU_R[5:0], VTLU_R[5:0]						V _{DSTHU} (mV)	V _{DSTLU} (mV)
[5]	[4]	[3]	[2]	[1]	[0]		
-1600m	+800m	+400m	+200m	+100m	+50m		
1	1	0	0	0	0	800	800
1	1	0	0	0	1	850	850
1	1	0	0	1	0	900	900
1	1	0	0	1	1	950	950
1	1	0	1	0	0	1,000	1,000
1	1	0	1	0	1	1,050	1,050
1	1	0	1	1	0	1,100	1,100
1	1	0	1	1	1	1,150	1,150
1	1	1	0	0	0	1,200	1,200
1	1	1	0	0	1	1,250	1,250
1	1	1	0	1	0	1,300	1,300
1	1	1	0	1	1	1,350	1,350
1	1	1	1	0	0	1,400	1,400
1	1	1	1	0	1	1,450	1,450
1	1	1	1	1	0	1,500	1,500
1	1	1	1	1	1	1,550	1,550

For low-side MOSFETs, the drain-source voltage (V_{DS}) is measured between VSUx/VSVx/VSUx pin and LSSx pin. LSSx pin (instead of GND) functions as the reference to avoid adding any low-side current-sensing voltage to the actual V_{DS} measurement and prevent false OVP detection.

For high-side MOSFETs, V_{DS} is measured between VSUx/VSVx/VSUx pin and VDHx pin. VDHx pin (instead of VCC_x) serves as the reference to avoid adding reverse diode voltage and high-side current-sensing voltage to the actual V_{DS} measurement and prevent false OVP detection.

VDHx pin is a dedicated low-current sensing input to the top of the MOSFET bridge. It shall be independently and directly connected to the common node between the positive power supply and the drain of the high-side MOSFET. With U phase as an example, the input current at VDHx pin is proportional to V_{DS} over-voltage threshold voltage V_{DSTHU} (same for V/W phase), approximately expressed as:

$$I_{VDH} = (1.8 * V_{DSTHU} + 30) * 3$$

where, I_{VDH} denotes the input current (μA) at VDHx pin, and V_{DSTHU} represents the drain-source overvoltage threshold voltage (V) as previously defined. Note that VDHx pin can withstand negative voltages down to -5V. During negative transients, this pin remains directly connected to the high-side node of the three-phase bridge, with such transients clamped by the body diodes of the power MOSFETs. In extreme fault

conditions (such as reverse battery connection), the body diodes can also effectively clamp the negative voltage to protect the circuit.

The output from each V_{DS} overvoltage comparator is filtered by a V_{DS} over-voltage qualifier circuit. This circuit uses a timer to verify the comparator output to determine whether a V_{DS} OVP is valid. The duration of the V_{DS} over-voltage qualifying timer, $t_{VDQU/V/W}$, is determined by the register variable $T_{VDU/V/W\_R}[5:0]$. It is approximately defined as:

Using the U-phase as an example, t_{VDQU} is defined approximately as follows: (same for V and W phases):

$$t_{VDQU} = n * 100 \text{ ns}$$

where n is a positive integer defined by $T_{VDU\_R}[5:0]$.

Table 18-6 Filtering Time (U-phase Example)

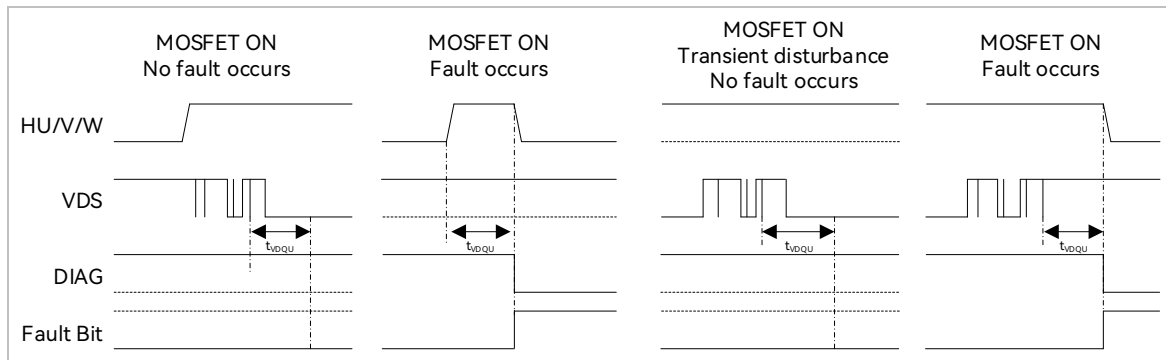
TVDU_R[5:0]						TVDQU (ns)
[5]	[4]	[3]	[2]	[1]	[0]	
-3200ns	+1600ns	+800ns	+400ns	+200ns	+100ns	
0	0	0	0	0	0	3200
0	0	0	0	0	1	3300
0	0	0	0	1	0	3400
0	0	0	0	1	1	3500
0	0	0	1	0	0	3600
0	0	0	1	0	1	3700
0	0	0	1	1	0	3800
0	0	0	1	1	1	3900
0	0	1	0	0	0	4000
0	0	1	0	0	1	4100
0	0	1	0	1	0	4200
0	0	1	0	1	1	4300
0	0	1	1	0	0	4400
0	0	1	1	0	1	4500
0	0	1	1	1	0	4600
0	0	1	1	1	1	4700
0	1	0	0	0	0	4800
0	1	0	0	0	1	4900
0	1	0	0	1	0	5000
0	1	0	0	1	1	5100
0	1	0	1	0	0	5200
0	1	0	1	0	1	5300
0	1	0	1	1	0	5400
0	1	0	1	1	1	5500
0	1	1	0	0	0	5600
0	1	1	0	0	1	5700
0	1	1	0	1	0	5800
0	1	1	0	1	1	5900
0	1	1	1	0	0	6000

TVDU_R[5:0]						TVDQU (ns)
[5]	[4]	[3]	[2]	[1]	[0]	
-3200ns	+1600ns	+800ns	+400ns	+200ns	+100ns	
0	1	1	1	0	1	6100
0	1	1	1	1	0	6200
0	1	1	1	1	1	6300
1	0	0	0	0	0	0
1	0	0	0	0	1	100
1	0	0	0	1	0	200
1	0	0	0	1	1	300
1	0	0	1	0	0	400
1	0	0	1	0	1	500
1	0	0	1	1	0	600
1	0	0	1	1	1	700
1	0	1	0	0	0	800
1	0	1	0	0	1	900
1	0	1	0	1	0	1000
1	0	1	0	1	1	1100
1	0	1	1	0	0	1200
1	0	1	1	0	1	1300
1	0	1	1	1	0	1400
1	0	1	1	1	1	1500
1	1	0	0	0	0	1600
1	1	0	0	0	1	1700
1	1	0	0	1	0	1800
1	1	0	0	1	1	1900
1	1	0	1	0	0	2000
1	1	0	1	0	1	2100
1	1	0	1	1	0	2200
1	1	0	1	1	1	2300
1	1	1	0	0	0	2400
1	1	1	0	0	1	2500
1	1	1	0	1	0	2600
1	1	1	0	1	1	2700
1	1	1	1	0	0	2800
1	1	1	1	0	1	2900
1	1	1	1	1	0	3000
1	1	1	1	1	1	3100

$t_{VDQU/VW}$ the qualifying timer, operates in debounce mode to filter transient VDS over-voltage signals, as shown in Figure 18-6. In this mode, the timer starts each time the comparator output indicates a VDS fault condition when the corresponding MOSFET is active. It resets when the comparator output returns to the normal state. However, if the over-voltage condition persists until the timer expires (set by $t_{VDQU/VW}$), the V_{DS} OVP is considered valid and the corresponding OVP flag bits STAU_R[FAULT_VDSHU], STAU_R[FAULT_VDSLUI] (U phase high-side/low-side), STAV_R[FAULT_VDSHV], STAV_R[FAULT_VDSLVI] (V phase high-side/low-side), STAW_R[FAULT_VDSHW], or STAW_R[FAULT_VDSLWI] (W phase high-

side/low-side) is set to “1” by hardware.

Figure 18-5 $t_{VDQU/V/W}$ Timing Diagram in Debounce Mode



If a valid V_{DS} over-voltage protection is detected, the 6N pre-driverx latches the fault state and disables the associated MOSFET. This state remains latched even after the V_{DS} OVP disappears. A write of “1” to `SLPF_R[VDS_CLR]` clears this protection state.

See 18.17.1.7 `VTHU_R` (0x86) ~ 18.17.1.15 `TVDW_R` (0x8E) for the registers related to MOSFET V_{DS} OVP.



Note:

MOSFET V_{DS} OVP parameters for FU7565Q1 are configured via registers in sections 18.17.2.9 `VTHU_R` (0x87) ~ 18.17.2.17 `TVDW_R` (0x8F).

18.2.4.1.6 6N Pre-driverx Passive Pull-down

Each pre-driverx output includes a discharge circuit to keep external MOSFETs turned off during power-down. This circuit is implemented by a fixed pull-down resistor (950k Ω under low gate-source voltage conditions; 100k Ω for FU7565Q1) that remains inactive during normal operation but provides a discharge path for any charge accumulated on the MOSFET gate even when the power is not connected. In this case, any externally induced charge on the MOSFET gate can be discharged below the turn-on threshold. In some applications, this design eliminates the need for external gate-source resistors.

18.2.4.1.7 Shoot-through Protection

To prevent shoot-through (cross conduction) in any phase of the power MOSFET bridge, a deadtime delay must be implemented between turning off one MOSFET (high-side or low-side) and turning on the other. Shoot through occurs when the high-side and low-side MOSFETs of the same are turned on simultaneously (e.g., during PWM edge transitions).

18.2.4.2 Under-voltage Lockout (UVLO) and Over-voltage Protection (OVP)

FU7574Q1 6N pre-driverx monitors system safety-related parameters, including those related to external active and passive components, power supplies, and interaction with external controllers. It also monitors voltages associated with driving the external power MOSFETs, especially VBB_x, each bootstrap capacitor's voltage, each external power MOSFET V_{DS} , as well as VCC_x overvoltage and undervoltage conditions.

18.2.4.2.1 VBB_x UVLO

The internal power regulator supplies the low-side gate driver and bootstrap charge current. Before enabling any outputs, ensure the VBB_x voltage is above the V_{BBUVF} threshold.

If VBB_x voltage falls below the UVLO threshold voltage V_{BBUVF} , STAV_R[VBBUVP] is set to "1" by hardware, and all pre-driverx outputs are pulled low. In this case, the motor driver is disabled and the motor enters a coasting state. When VBB_x voltage rises above the UVLO release voltage V_{BBUVR} , all pre-driverx outputs are re-enabled, and STAV_R[VBBUVP] is cleared to "0" by hardware.

18.2.4.2.2 VCC_x UVLO and OVP

FU7574Q1 6N pre-driverx monitors VCC_x voltage to determine if it exceeds the normal operating range (e.g., during external voltage transients). If VCC_x voltage rises above the OVP warning threshold voltage V_{CCOVWR} , STAU_R[VCCOVW] is set to "1" by hardware, and all pre-driver outputs continue to operate normally. When VCC_x voltage falls below the OVP warning release voltage V_{CCOVWF} , STAU_R[VCCOVW] is cleared to "0" by hardware.

If VCC_x voltage rises above the OVP threshold voltage V_{CCOVPR} , STAU_R[VCCOVP] is set to "1" by hardware, and all pre-driverx outputs are pulled low. In this case, the motor driver is disabled and the motor enters a coasting state. When VCC_x voltage falls below the OVP release voltage V_{CCOVPF} , all pre-driverx outputs are re-enabled, and STAU_R[VCCOVP] is cleared to "0" by hardware.

If VCC_x voltage falls below the UVLO threshold voltage V_{CCUVF} , STAU_R[VCCUVP] is set to "1" by hardware, and all pre-driverx outputs are pulled low. In this case, the motor driver is disabled and the motor enters a coasting state. When VCC_x voltage rises above the UVLO release voltage V_{CCUVR} all pre-driverx outputs are re-enabled, and STAU_R[VCCUVP] is cleared to "0" by hardware.

18.2.4.2.3 Bootstrap Capacitor UVLO and OVP

FU7574Q1 6N pre-driverx monitors the charging voltage of each bootstrap capacitor to ensure sufficient gate drive voltage for the high-side MOSFETs.

When the bootstrap circuit is active, the bootstrap capacitor voltage must remain above the UVLO threshold voltage V_{BUVF} to ensure reliable high-side MOSFET operation. Otherwise, a bootstrap fault will be indicated and high-side outputs disabled. In this case, $STAx\_R[VBUVx]$ ($x = U/V/W$) is set to "1" by hardware. This UVLO event typically occurs under high PWM duty cycles, where insufficient charging time prevents the bootstrap capacitor from supplying the required gate charge for high-side MOSFET during its on-time.

The bootstrap capacitor voltage must exceed the UVLO release voltage V_{BUVR} to enable the high-side output of the 6N pre-driverx. Once this condition is met, $STAx\_R[VBUVx]$ ($x = U/V/W$) is cleared to "0" by hardware. Otherwise, the 6N pre-driverx initiates a charging cycle by activating the corresponding low-side driver. Under normal conditions, the capacitor charges above V_{BUVR} within microseconds, after which the high-side output is enabled. The bootstrap voltage monitor stays active during high-side operation. If the voltage drops below the UVLO threshold voltage V_{BUVF} , a charging cycle is triggered. Once the bootstrap charging voltage reaches saturation, $STAx\_R[VBSATx]$ ($x = U/V/W$) is set to "1" by hardware.

If the bootstrap capacitor fails to charge sufficiently within $2\mu s$ for any reason, the bootstrap UVLO fault is considered valid. If an UVLO condition is detected while the bootstrap circuit is active and the high-side MOSFET is either on or turning on, the UVLO fault is immediately considered valid.

If the bootstrap capacitor voltage remains above the OVP threshold voltage V_{BOVR} for $2\mu s$, a high-side driver OVP fault is triggered, and 6N pre-driver outputs are disabled. In this case, $STAx\_R[VBOVPx]$ ($x = U/V/W$) is set to "1" by hardware. When the bootstrap capacitor voltage falls below the OVP release voltage V_{BOVF} , the high-side outputs are re-enabled and $STAx\_R[VBOVPx]$ ($x = U/V/W$) is cleared to "0" by hardware.

18.2.4.3 Thermal Shutdown Protection

When the temperature of the 6N pre-driverx exceeds the thermal shutdown (TSD) threshold $165^{\circ}C$, $STAV\_R[TSD]$ is set to "1" by hardware, and the 6N pre-driverx automatically disables all outputs. Proper measures must be implemented to limit power dissipation, preventing chip damage due to overheating and avoiding unpredictable device behaviors. Once the temperature falls below the thermal shutdown

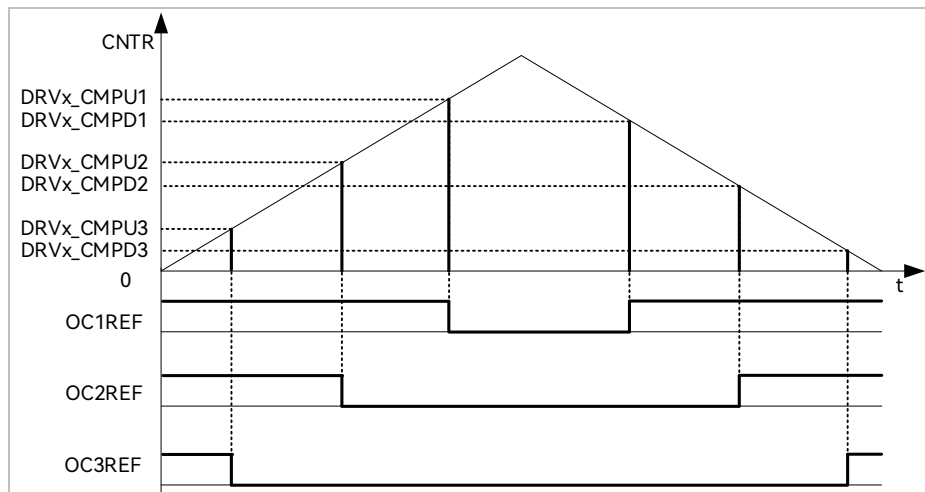
threshold T_{SD} by T_{SDhys} , the 6N pre-driverx resumes normal operation and STAV_R[TSD] is cleared to "0" by hardware.

18.2.5 Count and Compare Module

DRVx_CNTR acts as driver counter. The counter is disabled if the counter enable bit DRVx_CR[DRVEN] is set as "0". When the bit DRVx_CR[DRVEN] is set as "1", it first counts up from 0 to DRVx_ARR and then counts down to 1, and so on. Carrier frequency $f_{carrier} = f_{CLK} / (DRVx\_ARR * 2)$.

The three-phase comparison result OCxREF is generated by six three-phase compare registers, DRVx_CMPU1, DRVx_CMPD1, DRVx_CMPU2, DRVx_CMPD2, DRVx_CMPU3 and DRVx_CMPD3, where DRVx_CMPU1/DRVx_CMPD1 decides OC1REF (A phase), DRVx_CMPU2/DRVx_CMPD2 decides OC2REF (B phase) and DRVx_CMPU3/DRVx_CMPD3 decides OC3REF (C phase). For example, DRVx_CMPU1 is the comparison value on A-phase rising edge, and DRVx_CMPD1 is the comparison value on A-phase falling edge. OC1REF is "1" (high-level signal) if $DRVx\_CMPU1 > DRVx\_CNTR$ or $DRVx\_CMPD1 \geq DRVx\_CNTR$, and "0" (low-level signal) if $DRVx\_CMPU1 \leq DRVx\_CNTR$ or $DRVx\_CMPD1 < DRVx\_CNTR$. Then A-phase PWM duty cycle = $(DRVx\_CMPU1 + DRVx\_CMPD1) / (2 * DRVx\_ARR) * 100\%$. B-phase and C-phase PWM duty cycles are calculated in the same way.

Figure 18-6 Schematic Diagram of Count and Compare Module



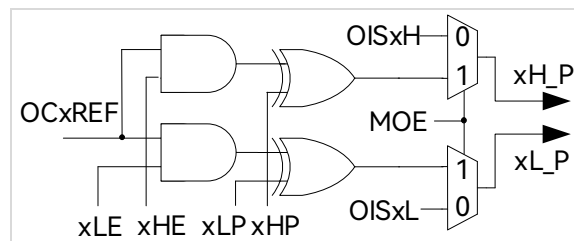
DRVx_DR register is configured to simultaneously update the values held by the six three-phase compare registers. After DRVx_DR register is written, the same value is written to the six three-phase compare registers, generating the three-phase comparison result OCxREF with the same duty cycle. Duty cycle = $DRVx\_DR / DRVx\_ARR * 100\%$.

If DRVx_DR or the three-phase comparison registers are not written, the three-phase comparison registers are updated according to SVPWM calculation results.

18.2.6 Enable and Polarity of Output Signals

The enable and polarity of output three-phase signals are configured by output enable bit DRVx_CM[R][xLE/xHE] and polarity control bit DRVx_CM[R][xLP/xHP] in DRVx_CM[R] register, which are used to implement pre-charging, brake, etc. The logic gates are 1 AND gate and 1 XOR gate.

Figure 18-7 Schematic Diagram of Enable and Polarity of Output Signals



The low level is output when both the output enable bit and polarity control bit are set to “0”, and the high level is output when the output enable bit is set to “0” but the polarity control bit is set to “1”. If both the output enable bit and polarity control bit are set to “1”, the output level is opposite to OCxREF, and if the output enable bit is set to “1” but the polarity control bit is set to “0”, the output level is the same as OCxREF.

The main output enable bit DRVx_OUT[MOE] decides the sources for output signals. When it is set to “1”, the output signals (xH_P/xL_P) are sourced from logic gate signals (the comparison value of the timer). When it is set to “0”, the output signals are sourced from the idle levels set by DRVx_OUT[OISxH/OISxL].

DRVx_DR, DRVx_ARR and DRVx_CM[R] can be configured to implement pre-charging, brake, etc. DRVx_DR and DRVx_ARR control the duty cycle and frequency of PWM. DRVx_CM[R] controls the signal output as a level signal or PWM.

Figure 18-8 Pre-charge Waveform

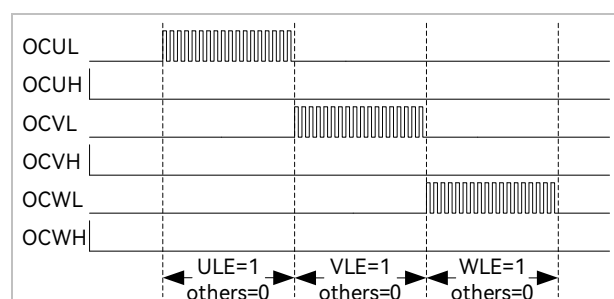
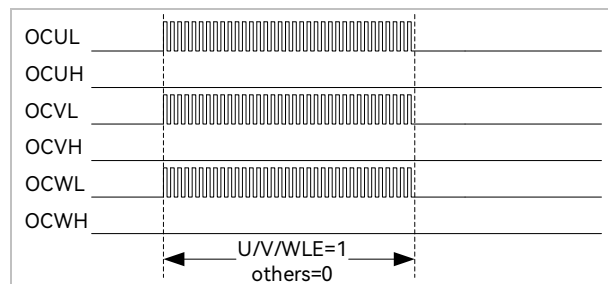


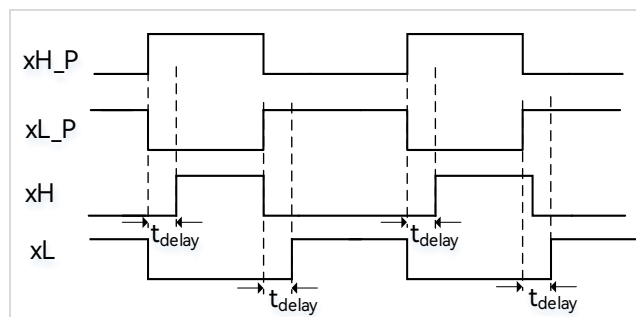
Figure 18-9 Brake Waveform



18.2.7 Deadtime Module

xH_P and xL_P signals are available for deadtime insertion. For complementary outputs, the deadtime insertion is enabled when DRVx_DTR is not "0". Each channel has an 8-bit deadtime generator, and three channels have the same deadtime, which is set by DRVx_DTR. When rising edge signals are detected, output high level of xH and xL is delayed for a period of time set in DRVx_DTR. $\text{Deadtime} = \text{DRVx\_DTR} \times T_{\text{CLK}}$. If the delayed time is greater than the output pulse width, the associated channel pulse width is not delayed.

Figure 18-10 Schematic Diagram of Deadtime Insertion



18.3 FOC Current Loop

18.3.1 Reference Voltage Input

The current loop of FOC module uses the d-axis current reference value NFOCx_IDREF and the q-axis current reference value NFOCx_IQREF as the reference, and uses the d-axis current sampling value NFOCx_ID and the q-axis current sampling value NFOCx_IQ as the feedback.

18.3.2 PI Controllers

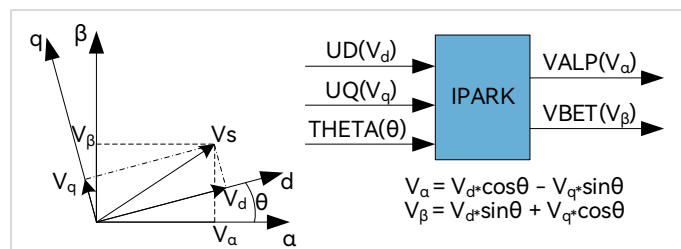
FOC module integrates two PI controllers:

- Flux control: PI controller of d-axis current, with current reference NFOCx_IDREF minus feedback current NFOCx_ID as the input, proportional coefficient NFOCx_DKP and the integral coefficient NFOCx_DKI for adjustment of PI controller performance, and NFOCx_DMAX and NFOCx_DMIN for limiting of the output amplitude to output d-axis voltage NFOCx_DUK, which is compensated by NFOCx_UDCPS to obtain NFOCx_UDFIN.
- Torque control: PI controller of q-axis current, with current reference NFOCx_IQREF minus feedback current NFOCx_IQ as the input, proportional coefficient NFOCx_QKP and the integral coefficient NFOCx_QKI for adjustment of PI controller performance, and NFOCx_QMAX and NFOCx_QMIN for limiting of the output amplitude to output q-axis voltage NFOCx_QUK, which is compensated by NFOCx_UQCPS to obtain NFOCx_UQFIN.

18.3.3 Coordinate Transformation

18.3.3.1 Inverse Park Transformation

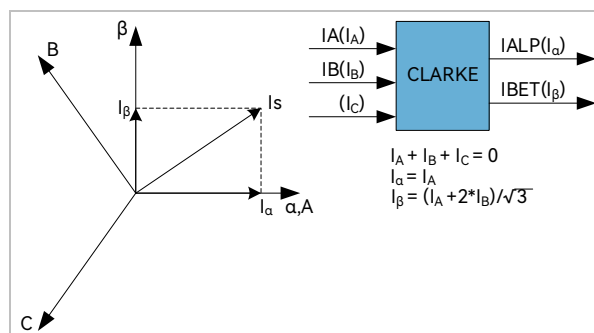
Figure 18-11 Inverse Park Transformation



Inverse Park transformation is used to transform two voltage vectors (NFOCx_UDFIN and NFOCx_UQFIN) from dq-axis coordinate to αβ-axis coordinate to obtain NFOCx_UALORG and NFOCx_UBEORG, and then compensate them by NFOCx_UALCPS and NFOCx_UBECPS to get NFOCx_UALPHA and NFOCx_UBETA respectively.

18.3.3.2 Clarke Transformation

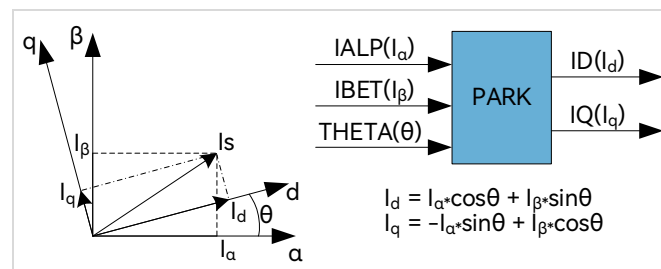
Figure 18-12 Clarke Transform



Clarke transformation is used to transform the sampled current NFOCx_IA (A phase) and NFOCx_IB (B phase) from three-phase stationary A-B-C coordinates to $\alpha\beta$ -axis coordinate to obtain NFOCx_IALPHA and NFOCx_IBETA.

18.3.3.3 Park Transformation

Figure 18-13 Park Transform



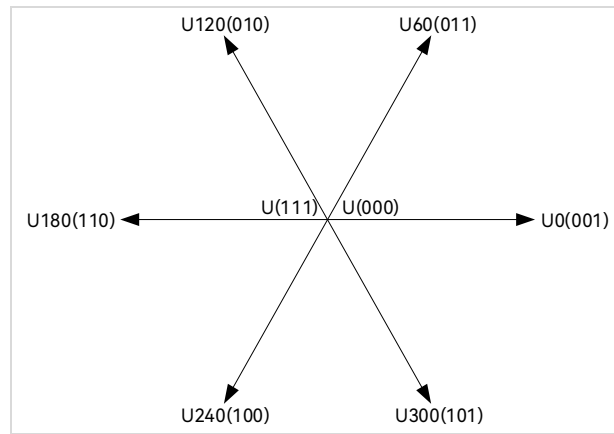
Park transformation is used to transform the current vectors, obtained after Clarke transformation (NFOCx_IALPHA and NFOCx_IBETA), from $\alpha\beta$ -axis coordinate to dq-axis coordinate to get the sampled dq-axis feedback current NFOCx_ID and NFOCx_IQ.

18.3.4 SVPWM

SVPWM algorithm is an important part of FOC. The main idea is to obtain quasi-circular rotating magnetic field by switching the inverter space voltage vectors. This method decreases harmonic components of the phase current, harmonic losses of the motor and torque ripple, and achieves high voltage utilization.

SVPWM generates pulse-width modulation signals for the three-phase motor voltage control, whose process can be reduced to a few simple equations. Since high side and low side of the inverter cannot be turned on simultaneously, there are two states for a phase, i.e., phase connected to bus voltage (represented by 1) or phase connected to ground (represented by 0). Therefore, voltage vector output of THE inverter has a total of $2^3 = 8$ possible states. $X_C X_B X_A$ represents the voltage vectors, where X_C represents the state of C-phase, X_B represents the state of B-phase and X_A represents the state of A-phase. For example, “100” represents the state that C-phase voltage is connected to bus voltage and A, B-phases are connected to ground. When the states of three-phase are all 1 or 0, there is no voltage drop between two phases and the state is called inactive state or zero voltage vector. The other six states which have voltage output are active voltage vectors with an adjacent state rotation offset of 60 degrees.

Figure 18-14 SVPWM Voltage Vector



SVPWM uses the sum of two adjacent vectors to generate any voltage vector located in the voltage vector space. As shown in Figure 18-15, U_{OUT} is the desired vector and it is in the sector between U_{60} and U_0 . Based on the principle of equal impulse, the effect, U_0 applied $2 \cdot T_1$ time and U_{60} applied $2 \cdot T_2$ time, is equivalent to the U_{OUT} . The rest of time (T_0) is applied by zero voltage vector.

Figure 18-15 SVPWM Voltage Vector Synthesis

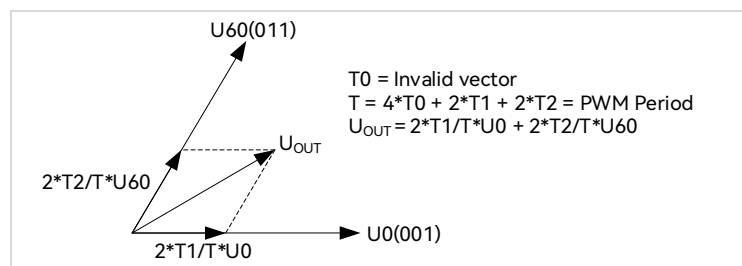


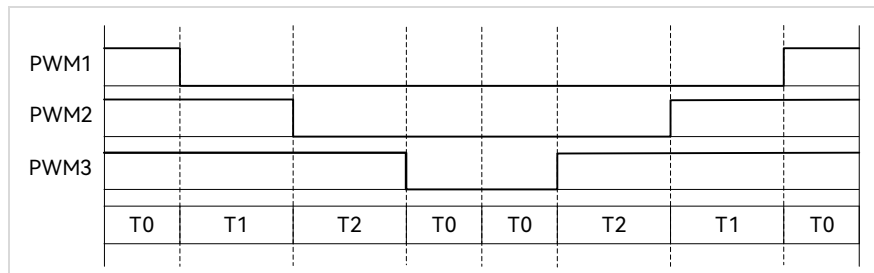
Table 18-7 States of SVPWM Inverter

Phase C	Phase B	Phase A	U_{ALP}	U_{BET}	Vector
0	0	0	0	0	000
0	0	1	$2/3 \cdot U_{DC}$	0	001
0	1	1	$1/3 \cdot U_{DC}$	$1/3 \cdot U_{DC}$	011
0	1	0	$-1/3 \cdot U_{DC}$	$1/3 \cdot U_{DC}$	010
1	1	0	$-2/3 \cdot U_{DC}$	0	110
1	0	0	$-1/3 \cdot U_{DC}$	$-1/3 \cdot U_{DC}$	100
1	0	1	$1/3 \cdot U_{DC}$	$-1/3 \cdot U_{DC}$	101
1	1	1	0	0	111

18.3.4.1 Seven-segment SVPWM

In single-shunt current sampling mode, seven-segment SVPWM is always used. In dual/triple-shunt current sampling mode, $DRVx\_FCR2[NSEG5]$ is set to "0" to select this mode.

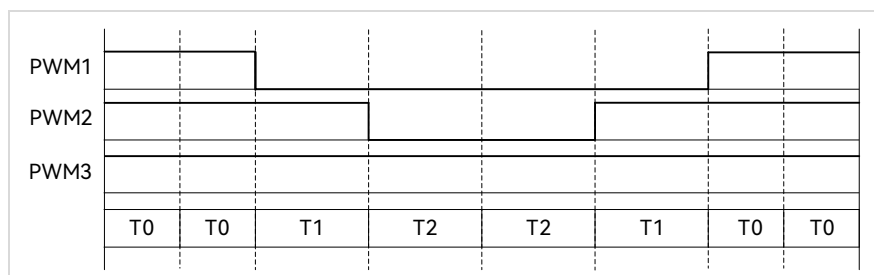
Figure 18-16 Output Level of Seven-segment SVPWM



18.3.4.2 Five-segment SVPWM

Five-segment SVPWM is available in dual/triple-shunt current sampling mode. `DRVx_FCR2[NSEG5]` is set to “1” to activate this mode.

Figure 18-17 Output Level of Five-segment SVPWM



18.3.5 Overmodulation

Overmodulation is available in single/dual/triple-shunt current sampling mode. `DRVx_FCR3[NOVMDL]` is set to “1” to enable the feature. The voltage output, `NFOCx_UD`, `NFOCx_UQ` and related limit amplitudes are multiplied by 1.15 in this mode.

18.3.6 Deadtime Compensation

Deadtime compensation is available in dual/triple-shunt current sampling mode. The compensation value of deadtime is configured by `NFOCx_TDTC`. This mode improves the quality of phase current at low speed.

18.3.7 Current and Voltage Sampling

In FOC mode, bus voltage and phase current are sampled by hardware automatically. Before the FOC module operates, ADC and operational amplifier shall be enabled and the corresponding control registers be configured. No configuration is required for ADC channel and scan mode. Single/dual/triple-shunt current sampling mode is selected by setting `DRVx_FCR0[NCSAMMD]`.

For master motor, in single-shunt current sampling mode, ADC1 channel 4 is the default sampling channel of the bus current (itrip). In dual-shunt current sampling mode, ADC1 channel 0 and channel 1 are the default sampling channels of A-phase current (ia) and B-phase current (ib) respectively. In triple-shunt current sampling mode, ADC1 channel 0, channel 1 and channel 4 are the default sampling channels of ia, ib and C-phase current (ic) respectively. ADC1 channel 2 can be selected for bus voltage sampling.

For slave motor, in single-shunt current sampling mode, ADC2 channel 4 is the default sampling channel of the bus current (itrip). In dual-shunt current sampling mode, ADC2 channel 0 and channel 1 are the default sampling channels of A-phase current (ia) and B-phase current (ib) respectively. In triple-shunt current sampling mode, ADC2 channel 0, channel 1 and channel 4 are the default sampling channels of ia, ib and C-phase current (ic) respectively.



Note:

When the slave motor is inactive and the master motor works in dual-shunt current sampling mode, ADC1 channel 0 and ADC2 channel 13 can be configured to sample the current ia and ib respectively, thereby reducing the total sampling time.

18.3.7.1 Single-shunt Current Sampling Mode

DRVx_FCR0[NCSAMMD] is set to “00000” to select the single-shunt current sampling mode. In this mode, ME module samples itrip (ADC 1 channel 4) twice during driver counter counting-up operation, and samples bus voltage during driver counter counting-down operation and after FOC module completes the calculation.

Since deadtime affects the accuracy of current sampling, ME module samples within T1' and T2', which is the applied time of active voltage vector with deadtime removed. NFOCx_TDLY is the register which advances or delays the current sampling time, and this register shall be configured reasonably to ensure sampling is completed within T1' and T2'. For example, when the clock runs at 48MHz and NFOCx_TDLY = 5, the sampling time is delayed by $5 \cdot T = 104\text{ns}$; NFOCx_TDLY = 0xFFFB(-5), the sampling time is advanced by $5 \cdot T = 104\text{ns}$.

Figure 18-18 Single-shunt Current Sampling Mode

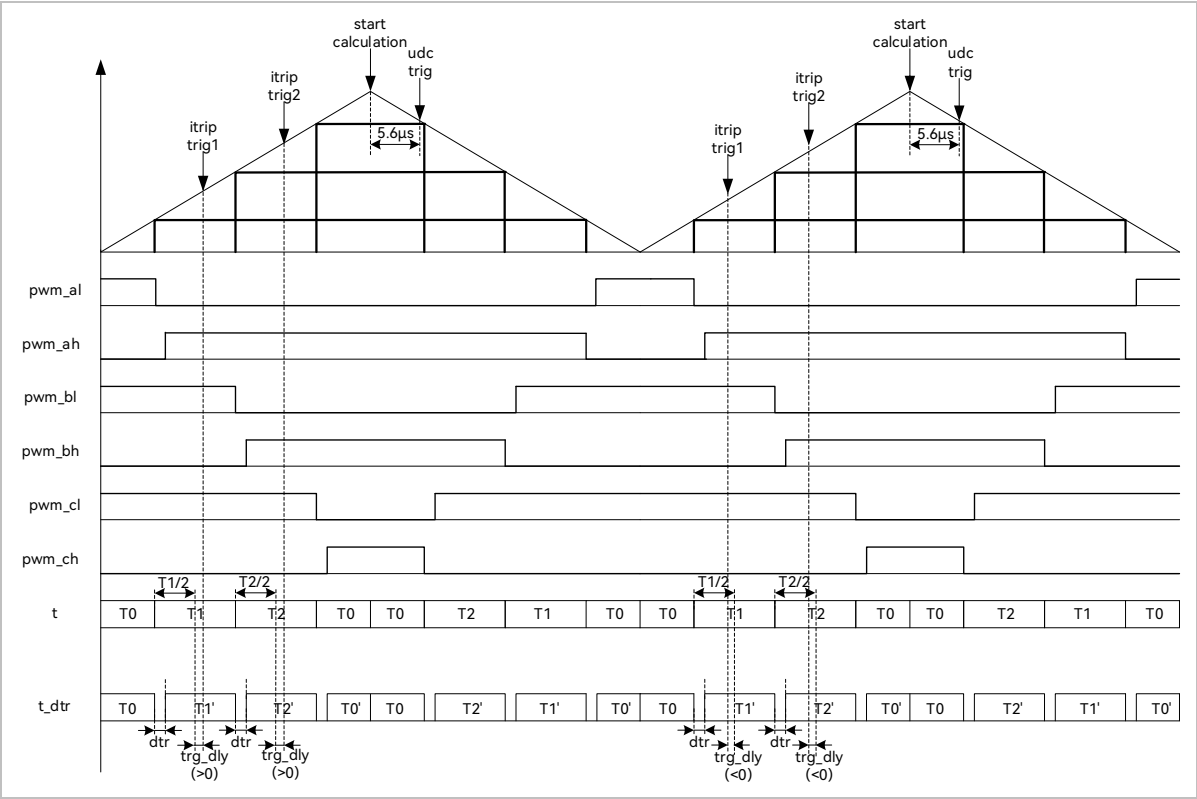
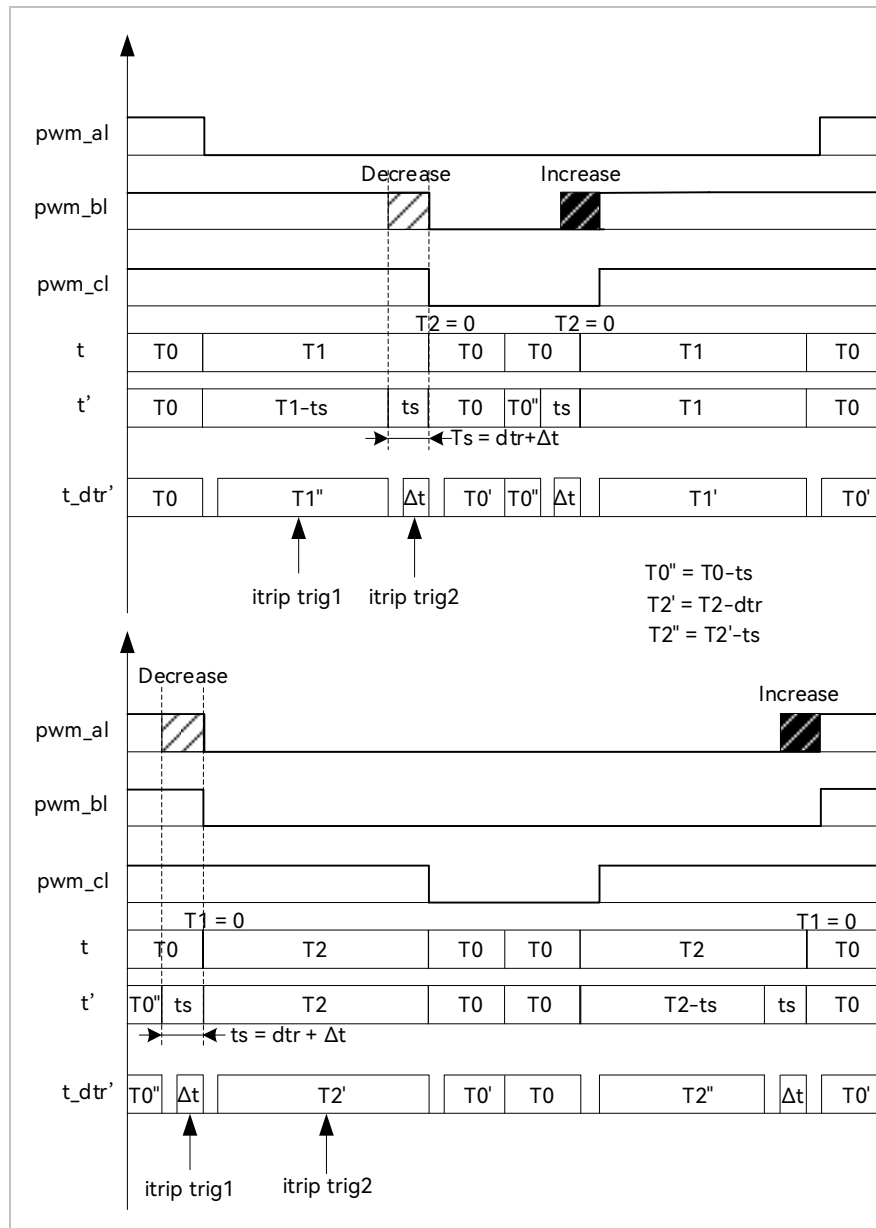


Figure 18-19 Time Compensation for Single-shunt Current Sampling



The time of single-shunt current sampling window may be not enough to sample the current in low modulation index and sector switching area. PWM waveform shall be adjusted to ensure the minimum sampling window required in the case. $NFOCx\_TS$ ($NFOCx\_TS = \text{minimum sampling window} + \text{deadtime}$) is used to configure the compensation value of deadtime, and ME module adjusts the PWM waveform automatically.

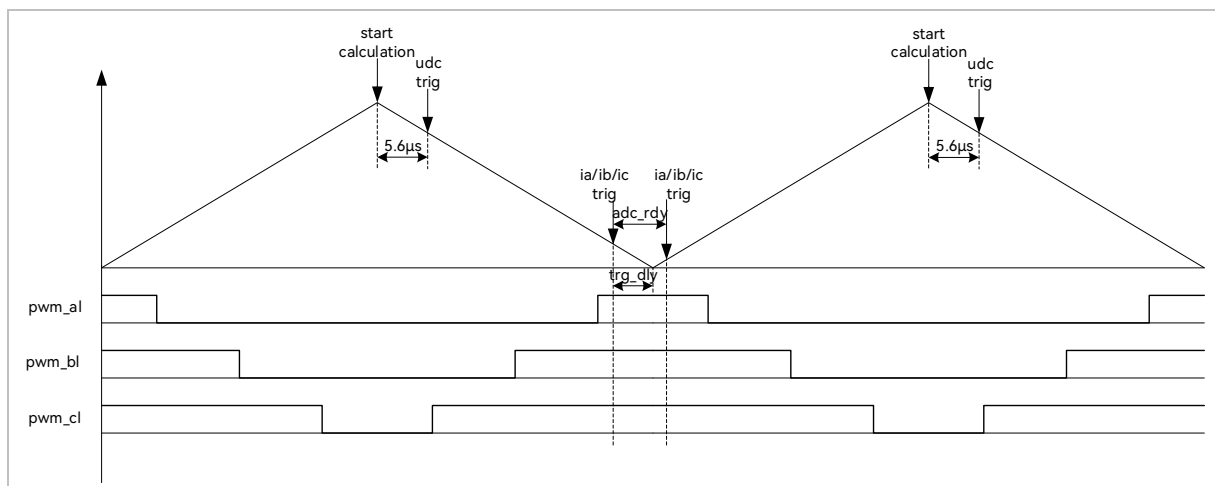
18.3.7.2 Dual/Triple-shunt Current Sampling Mode

$DRVx\_FCR0[NCSAMMD]$ is set to "00001/00010" to select dual/triple-shunt current sampling mode. In

triple-shunt mode, NFOCx_TDLY is used to configure the sampling time of a phase current (ia/ib/ic is determined according to the sector), and other phases are sampled at the end of previous sampling. In dual-shunt mode, NFOCx_TDLY is used to configure the sampling time of ia, and ib is sampled at the end of ia sampling. NFOCx_TDLY shall be configured reasonably to ensure current sampling time is within zero voltage vector (000). For example, when NFOCx_TDLY = 0x32 and FOC counter counts down, ia/ib/ic is sampled at $50 \cdot T = 1.04 \mu\text{s}$ after an underflow event, and then the other phases of ia/ib/ic are sampled.

In this mode, bus voltage is sampled when driver counter is down-counting and FOC module completes the calculation.

Figure 18-20 Dual/Triple-shunt Current Sampling Mode



18.3.7.3 Current Sampling Offset

The current sampling offset voltage shall be added to sample full range of current due to the existence of the positive and negative phase current. When phase current is 0, ADC result is the offset value. ADC result minus this value, 0x4000 default, is the sampling current. Since ADC reference voltage and hardware are nonideal, there is a deviation between the default value and the real value. Therefore, it is necessary to calibrate the offset. The calibration procedure is as follows. When there is no current in three phases, DRVx_FCR2[OFFSET_EN] is set to “1” to enable current sampling offset. MCU starts to sample the corresponding channel several times and averages all the sampled value to obtain NFOCx_IAREF, NFOCx_IBREF, NFOCx_ICREF and NFOCx_ITREF. Providing ADC sampling range on A phase is 0V ~ 5V and the reference value is 2.5V, $\text{NFOCx\_IAREF} = 2.5\text{V}/5\text{V} \cdot 32768 = 16384$ (CRS: 0x4000). After calibration, DRVx_FCR2[OFFSET_EN] is automatically cleared to “0” by hardware.

18.3.7.4 Current Sampling Switching

After FOC calculates $i_a/i_b/i_c$, it automatically updates the NFOCx_CSAM value to DRVx_FCR0[NCSAMMD]. When the FOC calculation enable bit DRVx_FCR0[NCALEN] = 0, NFOCx_CSAM is set equal to DRVx_FCR0[NCSAMMD]. When DRVx_FCR0[NCALEN] = 1, NFOCx_CMRSH is updated to DRVx_FCR0[NCSAMMD] upon overflow/underflow conditions. This mechanism is primarily used for switching current sampling modes. Registers related to current sampling mode include NFOCx_CMRSH and DRVx_ARRSH.

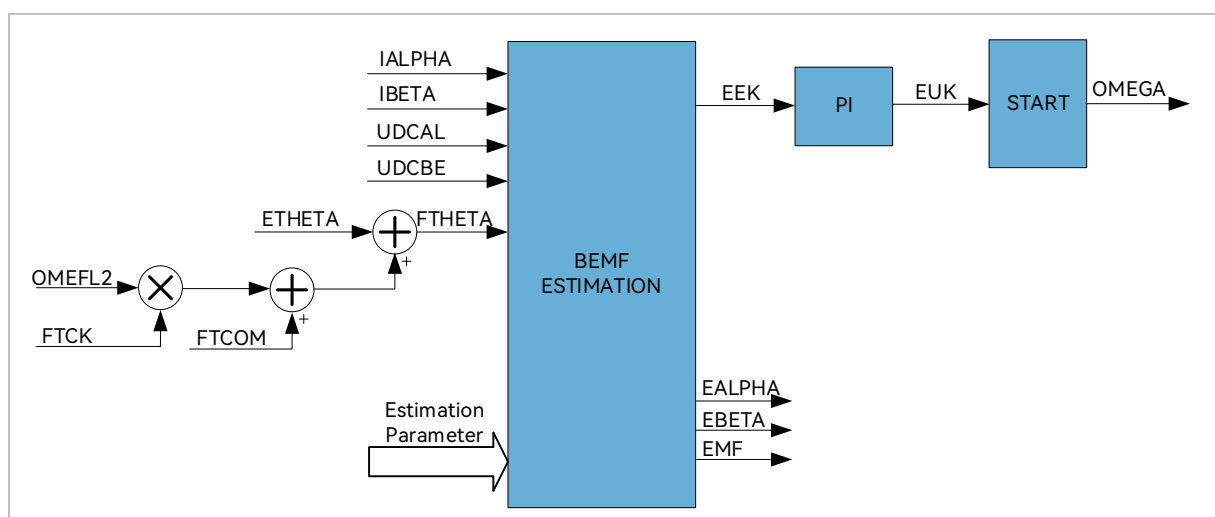
18.4 Angle Output

The angle output module estimates rotor position by sensorless algorithm to fulfill sensorless control of the motor. The motor rotation (angle) can be calculated by integrating motor speed that is obtained by an observer or by HFI-based method.

18.4.1 Speed Observer

The motor speed can be obtained by BEMF estimation module, PI controller and startup module. BEMF estimation module estimates BEMF values NFOCx_EALPHA/NFOCx_EBETA/NFOCx_EMF and angle error NFOCx_EEK. And then PI controller receives NFOCx_EEK and outputs NFOCx_EUK, which is delivered to startup module to define motor speed NFOCx_OMEGA.

Figure 18-21 Schematic Diagram of Speed Observer



18.4.1.1 BEMF Estimation Module

The BEMF estimation module builds the motor model based on selected observer and input motor

parameters, and outputs estimated BEMF values based on the sampled current and voltage. BEMF of the motor varies as both a function of the rotor's position and speed. Sliding mode observer (SMO), flux observer (NFO, CFO and AFO) and adaptive observer (AO) can be selected to estimate BEMF values NFOCx_EALPHA and NFOCx_EBETA.

The ME module uses sliding mode observer (SMO) for BEMF estimation by default. The involved FOC registers include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_KSLIDE, NFOCx_MAXERR and NFOCx_MERRRE.

The adaptive observer (AO) is enabled by setting DRVx_FCR6[EST_MD] = 001. The involved FOC registers include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_EMAX, NFOCx_EMIN, NFOCx_EKP and NFOCx_EKI.

The current model flux observer (CFO) is enabled by setting DRVx_FCR6[EST_MD] = 010. The involved FOC registers include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_KSLIDE, NFOCx_FEK6, NFOCx_FEK7, NFOCx_FEK8, NFOCx_EMAX, NFOCx_EMIN, NFOCx_EKP and NFOCx_EKI.

The nonlinear flux observer (NFO) is enabled by setting DRVx_FCR6[EST_MD] = 011. The involved FOC registers include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_KSLIDE, NFOCx_FEK6, NFOCx_EMAX, NFOCx_EMIN, NFOCx_EKP and NFOCx_EKI.

The adaptive full-order observer (AFO) is enabled by setting DRVx_FCR6[EST_MD] = 100. The involved FOC registers include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_FEK5, NFOCx_AFKDF, NFOCx_AFKAF, NFOCx_AFKP, NFOCx_AFKI, NFOCx_AFMAX, NFOCx_AFMIN, NFOCx_EKP and NFOCx_EKI.

If DRVx_FCR3[DEL_MD] = 00, arctangent (ATAN) is used to calculate the angle error NFOCx_EEK. If DRVx_FCR3[DEL_MD] = 01, sine / cosine is used. If DRVx_FCR3[DEL_MD] = 10, $\Delta\theta$ /EMF based on sine / cosine is used. Then, NFOCx_EEK is sent to the PI controller to obtain the estimated speed NFOCx_EUK.

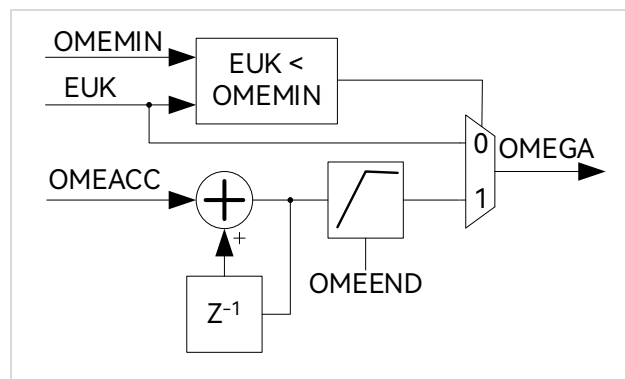
18.4.1.2 Startup Module

The motor may fail to start as the observer module may have a big estimation error when the motor starts due to small output current. In this case, the low speed observer start or Omega startup can be selected to ensure the motor starts smoothly.

The low-speed observer is enabled when $\text{DRVx\_FCR0}[\text{LO\_EN}] = 1$. If $\text{DRVx\_FCR2}[\text{OMELD\_EN}] = 1$, the estimated speed NFOCx_LOME by the low-speed observer is used as NFOCx_OMEGA .

The Omega startup is enabled when $\text{DRVx\_FCR1}[\text{OME\_STA\_EN}] = 1$. As shown in the below figure, different speeds are used as NFOCx_OMEGA by comparing NFOCx_EUK (estimated speed of the observer) and NFOCx_OMEMIN . If $\text{NFOCx\_EUK} < \text{NFOCx\_OMEMIN}$, forced speed of the observer is selected as NFOCx_OMEGA , which starts from 0 and increases by NFOCx_OMEACC in every cycle until it reaches NFOCx_OMEEND . If $\text{NFOCx\_EUK} \geq \text{NFOCx\_OMEMIN}$, NFOCx_EUK is selected as NFOCx_OMEGA .

Figure 18-22 Schematic Diagram of Omega Startup Module



NFOCx_OMEGA is converted to NFOCx_OMEFLT and NFOCx_OMEFL2 after the first-order and second-order low-pass filters.

18.4.2 High-frequency Injection (HFI)

The basic principle of HFI is to superimpose a high frequency voltage signal on the fundamental excitation and apply it to the three-phase winding of the motor, then detect and extract the corresponding high-frequency current generated in the motor, and obtain the rotor position information through a specific algorithm. HFI feature is enabled when $\text{DRVx\_FCR2}[\text{HFI\_CAL\_EN}] = 1$. NFOCx_HUK , or the speed calculated by HFI algorithm, is updated to NFOCx_OMEGA by setting $\text{DRVx\_FCR2}[\text{OMELD\_EN}] = 1$.

18.4.3 Flux Observer

18.4.3.1 Common Flux Observer (CFO)

The common flux observer(CFO) is enabled by configuring $\text{DRVx\_FCR6}[\text{EST\_MD}] = 010$. $\text{DRVx\_FCR6}[\text{ESTU\_SEL}]$ determines Q-format used by the CFO for reading NFOCx_UDCALP and NFOCx_UDCBETA . $\text{DRVx\_FCR6}[\text{ESTID\_SEL}]$ specifies ID source for the CFO calculation. $\text{DRVx\_FCR3}[\text{DEL\_MD}]$ sets the PLL

angle calculation mode. Registers related to the CFO include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_KSLIDE, NFOCx_FEK6, NFOCx_FEK7, NFOCx_FEK8, NFOCx_EMAX, NFOCx_EMIN, NFOCx_EKP and NFOCx_EKI.

18.4.3.2 Nonlinear Flux Observer (NFO)

The nonlinear flux observer (NFO) is enabled by setting DRVx_FCR6[EST_MD] = 011. DRVx_FCR6[ESTU_SEL] determines Q-format used by the NFO for reading NFOCx_UDCALP and NFOCx_UDCBETA. DRVx_FCR6[ESTID_SEL] specifies ID source for the NFO calculation. DRVx_FCR3[DEL_MD] sets the PLL angle calculation mode. Registers related to the NFO include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_KSLIDE, NFOCx_FEK6, NFOCx_EMAX, NFOCx_EMIN, NFOCx_EKP and NFOCx_EKI.

18.4.3.3 Adaptive Flux Observer (AFO)

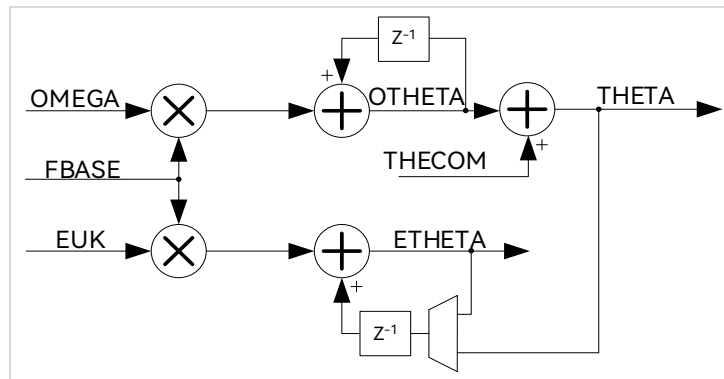
The adaptive flux observer(AFO) is enabled by setting DRVx_FCR6[EST_MD] = 100. DRVx_FCR6[ESTU_SEL] determines Q-format used by the AFO for reading NFOCx_UDCALP and NFOCx_UDCBETA. DRVx_FCR6[ESTID_SEL] specifies ID source for the AFO calculation. DRVx_FCR3[DEL_MD] sets the PLL angle calculation mode. Registers related to the AFO include NFOCx_EK1, NFOCx_EK2, NFOCx_EK3, NFOCx_EK4, NFOCx_FEK5, NFOCx_AFKDF, NFOCx_AFKAF, NFOCx_AFKP, NFOCx_AFKI, NFOCx_AFMAX, NFOCx_AFMIN, NFOCx_EKP and NFOCx_EKI.

18.4.4 Angle Calculation Module

The angle estimation module is used to calculate NFOCx_THETA and NFOCx_ETHERA. NFOCx_THETA is applied in coordinate transformation of the FOC current loop, and NFOCx_ETHERA is converted as NFOCx_FTHETA through feedback compensation, which is sent to BEMF estimation module for speed calculation.

The angle NFOCx_OTHETA is solved based on final speed NFOCx_OMEGA and speed reference NFOCx_FBASE, and it is compensated with NFOCx_THECOM to output the final angle NFOCx_THETA. When HFI feature is enabled, or the low speed observer is enabled, or Omega startup is enabled and DRVx_FCR2[OMESTA_MD] = 1 is configured, the integral of the estimated angle NFOCx_ETHERA is sourced from NFOCx_ETHERA. When Omega startup is enabled but DRVx_FCR2[OMESTA_MD] = 0, the integral of the estimated angle NFOCx_ETHERA is sourced from NFOCx_THETA.

Figure 18–23 Schematic Diagram of Angle Estimation Module



18.5 Outer Loop of FOC

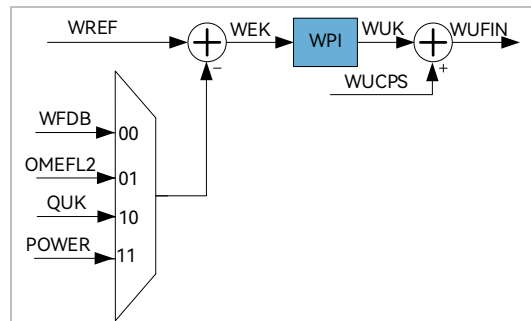
An outer loop calculation is performed once when $DRVx\_PTR[WPI\_TRG] = 1$. An outer loop calculation is automatically performed once in every carrier cycle when $DRVx\_FCR1[WPIAUTO] = 01$. An outer loop calculation is automatically performed once in every SysTick cycle when $DRVx\_FCR1[WPIAUTO] = 10$.

The outer loop of FOC is selected by configuring $DRVx\_FCR1[WPIMD]$.

- > Configuring $DRVx\_FCR1[WPIMD] = 00$ selects the feedback value $NFOCx\_WFDB$ as the manual input to enable software-based closed-loop control.
- > Configuring $DRVx\_FCR1[WPIMD] = 01$ selects outer loop feedback as the motor speed $NFOCx\_OMEFL2$ to enable the speed-current dual closed-loop control.
- > Configuring $DRVx\_FCR1[WPIMD] = 10$ selects outer loop feedback as the q-axis voltage $NFOCx\_QUK$ to enable the voltage-current dual closed-loop control.
- > Configuring $DRVx\_FCR1[WPIMD] = 11$ selects outer loop feedback as the motor power $NFOCx\_POWER$ enable the power-current dual closed-loop control.

The outer loop of FOC uses $NFOCx\_WREF$ as the reference input. The reference input $NFOCx\_WREF$ minus the feedback value generates $NFOCx\_WEK$, which is sent to the PI controller to output $NFOCx\_WUK$. After compensation by $NFOCx\_WUCPS$, $NFOCx\_WUK$ is converted to $NFOCx\_WUFIN$. When $DRVx\_FCR1[WPILDEN] = 1$, $NFOCx\_WUFIN$ is automatically updated to $NFOCx\_IQREF$.

Figure 18-24 Schematic Diagram of Outer Loop of FOC

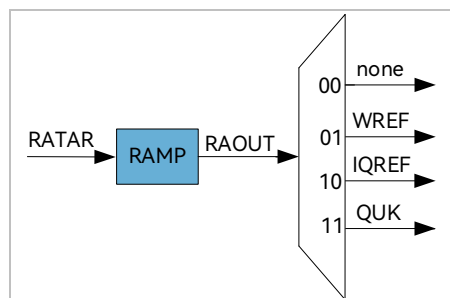


18.6 Ramping Calculation

A ramping calculation is performed once when $\text{DRVx\_PTR}[\text{RAMP\_TRG}] = 1$. A ramping calculation is automatically performed once in every SysTick cycle when $\text{DRVx\_FCR1}[\text{RAMP\_AUTO}] = 1$. If NFOCx_RAOUT fails to reach NFOCx_RATAR , it adds (or subtracts) the step value $\text{NFOCx\_RAIN}/\text{NFOCx\_RADEC}$ as the ramping output, otherwise, NFOCx_RATAR is used as the ramping output.

If $\text{DRVx\_FCR1}[\text{RAMPMD}] = 00$, the ramping output is not updated. If $\text{DRVx\_FCR1}[\text{RAMPMD}] = 01$, the output is updated to NFOCx_WREF register. If $\text{DRVx\_FCR1}[\text{RAMPMD}] = 10$, the output is updated to NFOCx_IQREF register. If $\text{DRVx\_FCR1}[\text{RAMPMD}] = 11$, the output is updated to 16 high-order bits of the data held in NFOCx_QUK register.

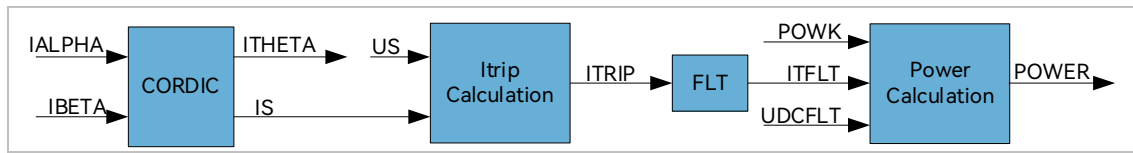
Figure 18-25 Schematic Diagram of Ramping Calculation



18.7 Power Calculation

The ME module calculates motor power based on the sampled current, modulation index of output voltage and filtered bus voltage. If $\text{DRVx\_FCR0}[\text{ITPOWMD}] = 00$, power calculation is not performed. If $\text{DRVx\_FCR0}[\text{ITPOWMD}] = 10$, $\text{NFOCx\_ITRIP} = \text{NFOCx\_US} * \text{NFOCx\_IS}$. If $\text{DRVx\_FCR0}[\text{ITPOWMD}] = 11$, $\text{NFOCx\_ITRIP} = \text{NFOCx\_IS}$, which is used to obtain NFOCx_ITFLT after the low-pass filter and $\text{NFOCx\_POWER} = (\text{NFOCx\_ITFLT} * \text{NFOCx\_POWK2}) * (\text{NFOCx\_UDC} * \text{NFOCx\_POWK1})$.

Figure 18-26 Schematic Diagram of Power Calculation



18.8 Flux Weakening

The flux weakening feature is enabled when $\text{DRVx\_FCR2[FWEAK\_EN]} = 1$. Its calculation mode (MOD0 / MOD1) is selected by $\text{DRVx\_FCR2[FWEAK\_MD]}$. NFOCx_US is obtained from NFOCx_UALPHA and NFOCx_UBETA , and is then filtered to obtain NFOCx_USFLT . $(\text{NFOCx\_FWREF} - \text{NFOCx\_USFLT}) * \text{NFOCx\_UDCFLT}$ is used as the input to PI controller to output NFOCx_FWUK . In MOD0 mode ($\text{DRVx\_FCR2[FWEAK\_MD]} = 0$), $\text{NFOCx\_WUFIN} * \cos(\text{NFOCx\_FWUK})$ is updated to NFOCx_IQREF and $\text{NFOCx\_WUFIN} * \sin(\text{NFOCx\_FWUK})$ is clamped (saturated) and then updated to NFOCx_IDREF . In MOD1 mode ($\text{DRVx\_FCR2[FWEAK\_MD]} = 1$), NFOCx_WUFIN is updated to NFOCx_IQREF , and NFOCx_FWUK is clamped (saturated) and then updated to NFOCx_FWIDR , which is then added to NFOCx_IDREF to serve as the d-axis current reference.



Note:

Generally, the saturation limit NFOCx_IDRLIM varies between the calculation modes MOD0 and MOD1.

18.9 Terminal Voltage

NFOCx_USK and NFOCx_USOMEK are configured based on hardware and motor parameters. $\text{DRVx\_FCR5[UABC\_SEL]}$ is configured to selected the source of NFOCx_UDCALP / NFOCx_UDCBET . When $\text{DRVx\_FCR5[UABC\_SEL]} = 00$, NFOCx_UA/UB/UC are not sampled. The values calculated from NFOCx_UALPHA / NFOCx_BETA and NFOCx_UDC are updated to NFOCx_UDCALP / NFOCx_UDCBET . When $\text{DRVx\_FCR5[UABC\_SEL]} = 01$, NFOCx_UA/UB/UC are sampled. The values calculated from NFOCx_UALPHA / NFOCx_BETA and NFOCx_UDC are updated to NFOCx_UDCALP / NFOCx_UDCBET . When $\text{DRVx\_FCR5[UABC\_SEL]} = 10$, NFOCx_UA/UB/UC are sampled. The values calculated from NFOCx_UA/UB/UC are updated to NFOCx_UDCALP / NFOCx_UDCBET . When $\text{DRVx\_FCR5[UABC\_SEL]} = 11$, NFOCx_UA/UB/UC are sampled. The values calculated from NFOCx_UA/UB/UC are amplitude- and phase-compensated and then updated to NFOCx_UDCALP / NFOCx_UDCBET . When $\text{DRVx\_FCR5[UABC\_SEL]}$ is enabled, $\text{NFOCx\_UA / UB / UC}$ sampling starts at the overflow point.

**Note:**

- > For the master motor, the ADC sampling channels for UA, UB and UC are determined by CMP_CR2[CMP0FS] rather than CMP_CR2[CMP0MOD]. When CMP_CR2[CMP0FS] = 0, UA, UB and UC are sampled via ADC1 channel 6, ADC1 channel 8 and ADC1 channel 9 respectively. When CMP_CR2[CMP0FS] = 1, the corresponding channels are ADC1 channel 6, ADC1 channel 5 and ADC1 channel 7 respectively.
- > For the slave motor, the ADC sampling channels for UA, UB and UC are determined by CMP_CR6[CMP6FS] rather than CMP_CR6[CMP6MOD]. When CMP_CR6[CMP6FS] = 0, UA, UB and UC are sampled via ADC2 channel 6, ADC2 channel 8 and ADC2 channel 9 respectively. When CMP_CR6[CMP6FS] = 1, the corresponding channels are ADC2 channel 6, ADC2 channel 5 and ADC2 channel 7 respectively.

18.10 UQ Injection

When DRVx_FCR2[UQINJ_EN] = 1, UQ injection feature is enabled and NFOCx_UQCPS is automatically updated. The involved FOC registers include NFOCx_UIK0, NFOCx_UIK1, NFOCx_UIK2, NFOCx_UIK3, NFOCx_UIUS0, NFOCx_UIUS1, NFOCx_UIUS2, NFOCx_UIUS3, NFOCx_UITC0, NFOCx_UITC1, NFOCx_UITC2 and NFOCx_UITC3.

18.11 CORDIC by Software

The software can call CORDIC for the calculation when FOC module is idle. Eight CORDIC channels, CORDIC0 ~ CORDIC7, are available in software, which correspond to ME_COR[COR0] ~ ME_COR[COR7] respectively. ME_COR determines the CORDIC channel to be used, and each CORDIC channel can be assigned to enable CORDIC module to complete CORDIC calculation.

CORDIC0, CORDIC1, CORDIC4 and CORDIC5 channels are used to calculate sin and cos, and CORDIC2, CORDIC3, CORDIC6 and CORDIC7 channels to calculate ATAN and square root. CORDIC0 channel has the highest priority and CORDIC7 the lowest.

Calculation formula for sin and cos:

$$XO = XI \cdot \cos(THETA) - YI \cdot \sin(THETA)$$

$$YO = XI \cdot \sin(THETA) + YI \cdot \cos(THETA)$$

Calculation formula for square root and ATAN:

$$US = \sqrt{XI^2 + YI^2}$$

$$UTHETA = \arctan \frac{YI}{XI}$$

18.12 Angle Fusion

Angle fusion enables a smooth switching from the high-frequency injection angle `NFOCx_HTHETA` to the conventionally estimated angle `NFOCx_ATHETA`. Since the fusion logic is based the `NFOCx_HTHETA` loop, it is necessary to set `DRVx_FCR2[OMELD_EN] = 1`.

Two fusion modes, manual fusion and hardware-based fusion, can be selected via `DRVx_FCR5[ANGFU_MAEN]`.

- Configuring `DRVx_FCR5[ANGFU_MAEN] = 1` enables manual fusion mode. In this mode, the angle source is selected through `DRVx_FCR5[ANGFU_MD]`. 00 selects the high-frequency injection (HFI) angle as the source, 01 uses the fused angle, and 1x employs the estimated angle from SMO/AO/FO observers.
- Configuring `DRV1_FCR5[ANGFU_MAEN] = 0` enables hardware-based fusion mode. In this mode, `DRVx_FCR5[ANGFU_MD]` operates as a dynamic register that is automatically updated by hardware based on the comparison between `NFOCx_OMEFL2` and the threshold values (`NFOCx_FUMAX` / `NFOCx_FUMIN`). Specifically, when `NFOCx_OMEFL2 > NFOCx_FUMAX`, the hardware automatically sets `DRVx_FCR5[ANGFU_MD] = 1x`; when `NFOCx_OMEFL2 < NFOCx_FUMIN`, it sets `DRVx_FCR5[ANGFU_MD] = 00`; and in all other cases, it maintains `DRVx_FCR5[ANGFU_MD] = 01`.



Note:

In manual fusion mode, the weight is determined by `NFOCx_FUWEI` (Q15 format): SMO/AO/FO weight = 100% - `NFOCx_FUWEI`. In hardware-based fusion mode, the weight is set by `NFOCx_FUWEI` (Q6 format)

18.13 Current Loop Decoupling

Setting `DRVx_FCR6[CVD_EN] = 1` enables the current loop decoupling to resolve dynamic coupling issues in the currents. The four current loop decoupling modes, complex vector decoupling, negative feedback decoupling, internal model decoupling and internal model plus negative feedback decoupling, are implemented by configuring `NFOCx_CVK1`, `NFOCx_CVK2`, `NFOCx_CVK3`, `NFOCx_CVDK4`, `NFOCx_CVQK4`, `NFOCx_CVDK5` and `NFOCx_CVQK5`. Data format for these parameters is selected via `DRVx_FCR7[CVKO_SEL]`, with 00 for Q14 format, 01 for Q13 format, 10 for Q12 format and 11 for Q11 format.

After the current loop decoupling is enabled, registers related to PI parameters for the current loop must

be configured, including NFOCx_DKP, NFOCx_QKP, NFOCx_DKI, NFOCx_QKI, NFOCx_CVKI2D and NFOCx_CVKI2Q. Data format for these parameters is selected via DRVx_FCR7[CVKP_SEL], DRVx_FCR7[CVKI1_SEL] and DRVx_FCR7[CVKI2_SEL], with 00 for Q14 format, 01 for Q13 format, 10 for Q12 format, or 11 for Q10 format.

The output limits for the current loop's d-axis and q-axis are set by NFOCx_DMAX, NFOCx_DMIN, NFOCx_QMAX and NFOCx_QMIN. Additionally, setting DRVx_FCR6[CVD_SEL] = 1 enables software-calculated inverter output as the anti-windup feedback, with the calculation results to be written into NFOCx_CVQULO and NFOCx_CVDULO.



Note:

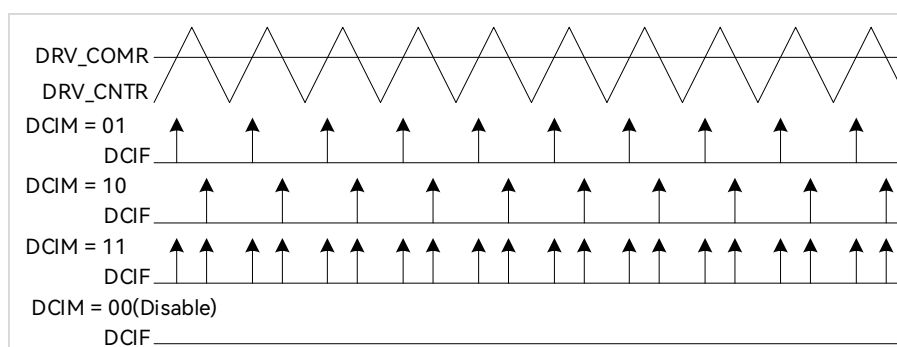
During the first current-loop decoupling PI calculation, NFOCx_UDCLIM serves as the denominator and shall be initialized to a value closed to the UDC.

18.14 ME Interrupt Sources

18.14.1 Driver Compare Match Interrupt

The generation conditions and time for compare match interrupt are configured by DRVx_IER[DCIM] and DRVx_COMR respectively. When the driver counter reaches the value set in DRVx_COMR and the conditions set by DRVx_IER[DCIM] are met, a compare match interrupt is generated and the interrupt flag bit DRVx_IFR[DCIF] is set to “1” by hardware. When DRVx_IER[DCIM] = 00, no interrupt is generated. When DRVx_IER[DCIM] = 01, a compare match interrupt is generated when the counter counts up. When DRVx_IER[DCIM] = 10, a compare match interrupt is generated when the counter counts down. When DRVx_IER[DCIM] = 11, a compare match interrupt is generated when the counter counts up/down.

Figure 18-27 Driver Compare Match Interrupt



DRVx_IER[DCIP] is used to set the number of carrier cycles to generate a compare match interrupt. When DRVx_IER[DCIP] = 0, a compare match interrupt is generated in one carrier cycle. When DRVx_IER[DCIP] = 1, a compare match interrupt is generated in two carrier cycles.

18.14.2 FG Interrupt

FG1 generation is enabled when DRV1_FCR1[FG_OE] = 1. If PH_SEL[T4CT] = 01, FG signal is output from PA0. If PH_SEL[T4CT] = 10, the signal is output from PA2. If PH_SEL[T4CT] = 11, the signal is output from PD3. FG2 generation is enabled when DRV2_FCR1 [FG_OE] = 1. If PH_SEL[T7CT] = 01, the signal is output from PA1. If PH_SEL[T7CT] = 10, the signal is output from PA3. If PH_SEL[T7CT] = 11, the signal is output from PD0.

The output FG signal corresponds to MSB of the FG counter FGTHETA. If DRVx_FCR1[FG_CALEN] = 1 or the FG module outputs a different level from that set by DRVx_FCR1[FG_IDLE_LEV], the FG counter FGTHETA calculates an FG result based on the set FG speed reference NFOCx_FGBASE and motor speed NFOCx_OMEFL2:

$$FGTHETA = FGTHETA + NFOCx_FGBASE * NFOCx_OMEFL2$$

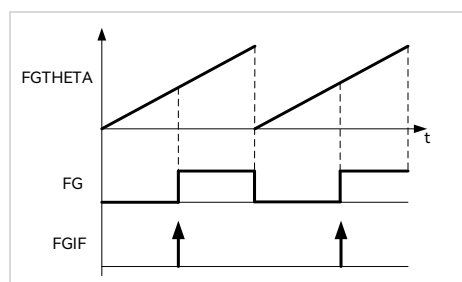
Calculation formula of NFOCx_FGBASE:

$$NFOCx_FGBASE = BASE\_FREQ * 32768 * 64 / 750000 * x$$

Where the last variable x represents the number of FG (Frequency Generator) signal pulses expected to be output within one electrical cycle and BASE_FREQ is the electrical frequency (in Hz) corresponding to the maximum motor speed.

The clock runs at 750KHz when DRVx_FCR1[FG_MD] = 0, and runs at 48MHz when DRVx_FCR1[FG_MD] = 1. During one full FGTHETA cycle, FG module outputs low-and-high levels.

Figure 18-28 FG Interrupt



FG Interrupt is enabled when $DRVx\_IER[FGIE]$ is set to “1”. An FG interrupt is generated on the rising edge of FG signal, and the interrupt flag bit $DRVx\_IFR[FGIF]$ is set to “1” by hardware.

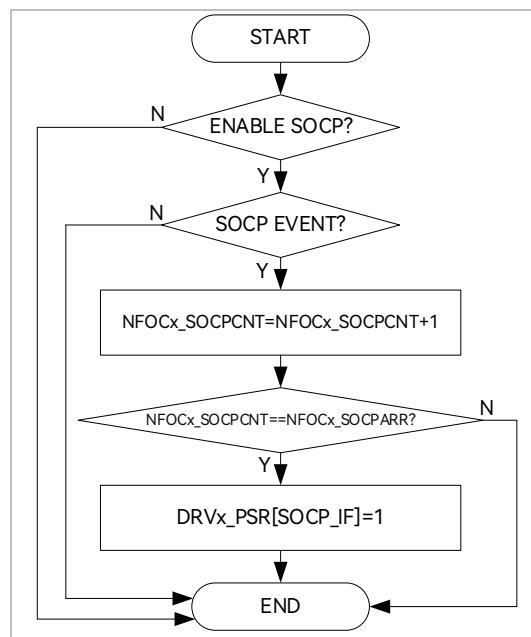
18.14.3 Motor Protection Interrupts

18.14.3.1 Software Over-current Protection (OCP)

An OCP calculation is performed once by software when $DRVx\_PTR[SOCP\_TRG] = 1$. An OCP calculation is automatically performed once by software in every carrier cycle when $DRVx\_PER[SOCP\_AUTO] = 1$. The OCP threshold is set by $NFOCx\_SOCP$, and a software OCP event occurs if $NFOCx\_ITRIP > NFOCx\_SOCP$.

The target count value for software OCP is configured by $NFOCx\_SOCPARR$. When a software OCP event occurs, $NFOCx\_SOCPCNT$ is increased by 1. When $NFOCx\_SOCPCNT$ reaches $NFOCx\_SOCPARR$, the software OCP interrupt flag bit $DRVx\_PSR[SOCP\_IF]$ is set to “1”.

Figure 18-29 Flow Chart of Software Overcurrent Protection



18.14.3.2 Over-voltage Protection (OVP) / Under-voltage Lockout (UVLO)

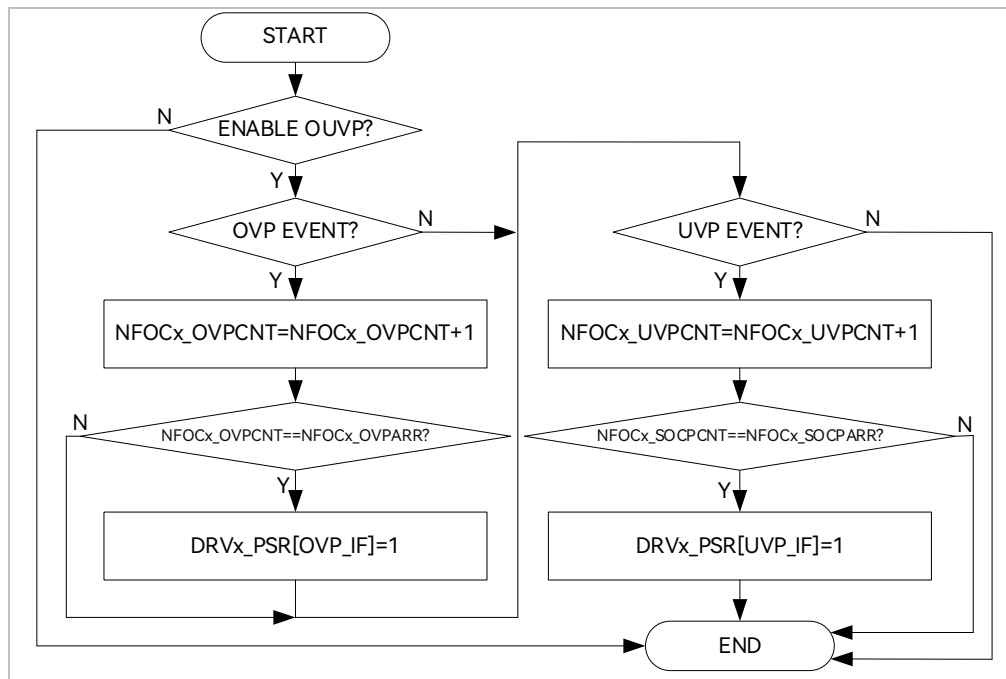
An OVP/UVLO calculation is performed once when $DRVx\_PTR[OUVP\_TRG] = 1$. An OVP/UVLO calculation is automatically performed once in every carrier cycle when $DRVx\_PER[OUVP\_AUTO] = 01$. An OVP/UVLO calculation is automatically performed once in every SysTick cycle when $DRVx\_PER[OUVP\_AUTO] = 10$. The OVP threshold is configured by $NFOCx\_OVP$, and an OVP event occurs when $NFOCx\_UDCFLT >$

NFOCx_OVP. The UVLO threshold is configured by NFOCx_UVP, and a UVLO event occurs when $NFOCx\_UDCFLT < NFOCx\_UVP$.

The target count value for OVP is configured by NFOCx_OVPARR. When an OVP event occurs, NFOCx_OVPCNT is increased by 1. When NFOCx_OVPCNT reaches NFOCx_OVPARR, the OVP interrupt flag bit DRVx_PSR[OVP_IF] is set to “1”.

The target count value for UVLO is configured by NFOCx_UVPARR. When a UVLO event occurs, NFOCx_UVPCNT is increased by 1. When NFOCx_UVPCNT reaches NFOCx_UVPARR, the UVLO interrupt flag bit DRVx_PSR[UVP_IF] is set to “1”.

Figure 18-30 Flow Chart of OVP/UVLO



18.14.3.3 Motor Lock Protection (MLP)

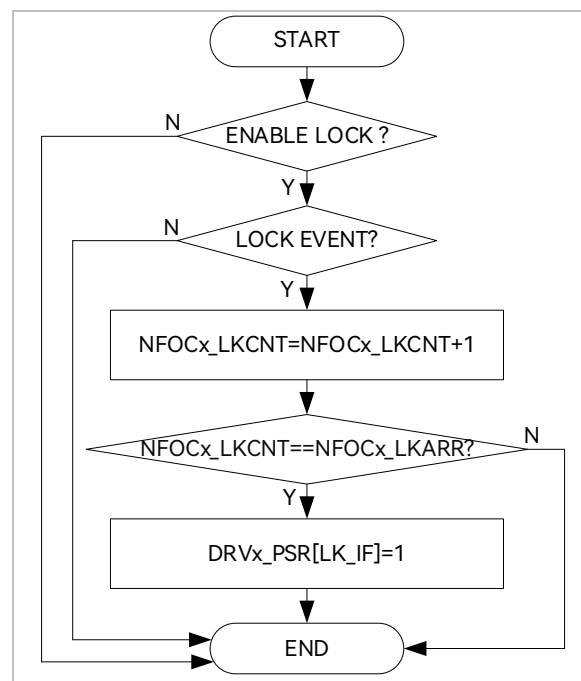
A MLP calculation is performed once when $DRVx\_PTR[LOCK\_TRG] = 1$. A MLP calculation is automatically performed once in every SysTick cycle when $DRVx\_PER[LOCK\_AUTO] = 1$. A MLP event occurs if any one of the following occurs.

- Configure $DRVx\_PER[LOCK0] = 1$ and set NFOCx_LKSMIN. If $NFOCx\_OMEFL2 < NFOCx\_LKSMIN$, a MLP event occurs.

- Configure $\text{DRVx\_PER}[\text{LOCK1}] = 1$ and set NFOCx_LKSMAX . If $\text{NFOCx\_OMEFL2} > \text{NFOCx\_LKSMAX}$, a MLP event occurs.
- Configure $\text{DRVx\_PER}[\text{LOCK2}] = 1$ and set NFOCx_LOCKK (the ratio of motor speed and BEMF). If $\text{NFOCx\_LOCKK} * \text{NFOCx\_EMF} < \text{NFOCx\_OMEFL2}$, a MLP event occurs.

The target count value for MLP is configured by NFOCx_LKARR . When a MLP event occurs, NFOCx_LKCNT is increased by 1. When NFOCx_LKCNT reaches NFOCx_LKARR , the MLP interrupt flag bit $\text{DRVx\_PSR}[\text{LK\_IF}]$ is set to “1”.

Figure 18-31 Flow Chart of MLP

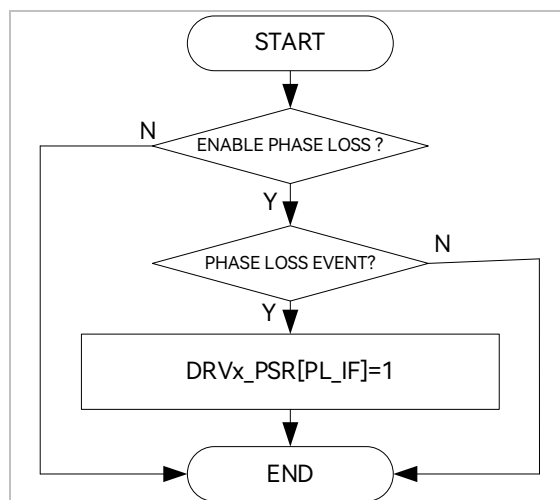


18.14.3.4 Phase Loss Protection

A phase loss protection calculation is performed once when $\text{DRVx\_PTR}[\text{PL\_TRG}] = 1$. A phase loss protection calculation is automatically performed once in every electrical cycle when $\text{DRVx\_PER}[\text{PL\_AUTO}] = 1$. A phase loss event occurs if the maximum current of any phase (NFOCx_IAMAX , NFOCx_IBMAX or NFOCx_ICMAX) is greater than the phase loss protection current NFOCx_NCURR and the product of this maximum current and NFOCx_PLK (multiple of phase loss protection current) is greater than the maximum current of any other two phases.

When a phase loss event occurs, the phase loss protection interrupt flag bit $\text{DRVx\_PSR}[\text{PL\_IF}]$ is set to “1”.

Figure 18-32 Flow Chart of Phase Loss Protection



18.15 High-speed Voltage Phase Compensation

A one-carrier-cycle delay exists between current sampling and driver update. Additionally, when implementing SVPWM logic digitally, an inevitable additional time delay is introduced. The half-sampling delay by the zero-order hold (ZOH) serve as a good approximation for the SVPWM delay. Thus, the total delay amounts to 1.5 carrier cycles. When the motor operates at high speeds, the angular error caused by this 1.5-cycle delay significantly impacts motor performance and therefore requires compensation. Since NFOCx_ETHETA already leads NFOCx_ATHETA by one carrier cycle before compensation, only a 0.5-cycle compensation is required to be applied via NFOCx_FTCK.

18.16 ME Registers

The ME registers are organized into the following 24 groups to facilitate understanding, configurations, as well as precise motor control and protection.

18.16.1 Driver Counter Registers

18.16.1.1 DRVx_IER (CSR: 0x542/0x582) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										CAIE	THIE	FGIE	DCIP	DCIM	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	CAIE	Abnormal FOC Calculation Interrupt After this bit is enabled, a FOC calculation is considered abnormal if it is completed during the counter counting-up operation (mainly for HFI and single-shunt current sampling mode). 0: Disable 1: Enable
[4]	THIE	TH Interrupt Enable After this bit is enabled, a TH interrupt is generated when the electrical angle switches from 0x7FFF to 0x8000. 0: Disable 1: Enable
[3]	FGIE	FG Interrupt Enable After this bit is enabled, an FG interrupt is generated in each rotation cycle (electrical cycle) in FOC or square-wave mode. 0: Disable 1: Enable
[2]	DCIP	Number of Carrier Cycles to Generate a Driver Match Interrupt 0: 1 interrupt in 1 carrier cycle 1: 1 interrupt in 2 carrier cycles
[1:0]	DCIM	Driver Match Interrupt Mode Selection The system decides whether to generate an interrupt according to DRVx_IER[DCIM] when driver counter value is equal to DRVx_COMR. 00: No interrupt is generated. 01: An interrupt is generated when the counter counts up. 10: An interrupt is generated when the counter counts down. 11: An interrupt is generated when the counter counts up/down.

18.16.1.2 DRVx_IFR (CSR: 0x543/0x583) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										CAIF	THIF	FGIF	RSV		DCIF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r0	r0	r0	-	-	r0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	CAIF	Abnormal FOC Calculation Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[4]	THIF	TH Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[3]	FGIF	FG Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[2:1]	RSV	Reserved
[0]	DCIF	Driver Match Interrupt Flag When driver counter reaches DRVx_COMR, the system decides whether to generate an interrupt according to DRVx_IER[DCIM]. This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending

18.16.1.3 DRVx_CNTR (CSR: 0x55A/0x59A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CNTR																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CNTR	Counter Value Driver duty cycle = $\text{DRVx\_CNTR} / \text{DRVx\_ARR} * 100\%$ Range [0,16383]  Note: DRVx_CNTR register can be written only when DRVx_CR[DRVEN] = 1.

18.16.1.4 DRVx_ARR (CSR: 0x550/0x590) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_ARR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	~	~	~	~	~	~	~	~	~	~	~	~	~	~
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_ARR	Counter reload value, which determines PWM frequency (center-aligned) The driver counter counts up from 0 to DRVx_ARR, at which point an overflow event occurs. It then counts back down to 1, and repeats this sequence continuously. Calculation formula: $f_{carrier} = f_{CLK} / (\text{DRVx\_ARR} * 2)$ For example, if the clock runs at 48MHz and DRVx_ARR = 1200, then $f_{carrier} = 48M / (1200 * 2) = 20KHz$ Range [0,16383]

18.16.1.5 DRVx_COMR (CSR: 0x552/0x592) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_COMR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	~	~	~	~	~	~	~	~	~	~	~	~	~	~
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_COMR	DRV Counter Compare Match Value A DRV counter compare match interrupt is generated when the count value is equal to DRVx_COMR and the conditions set in DRVx_IER[DCIM] are met. Duty cycle at the match point = $\text{DRVx\_COMR} / \text{DRVx\_ARR} \times 100\%$ Range [0,16383]

18.16.1.6 DRVx_DR (CSR: 0x551/0x591) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		DRVx_DR													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_DR	Three-phase PWM Duty Cycle Setting The data written to this register is updated to DRVx_CMPU1, DRVx_CMPD1, DRVx_CMPU2, DRVx_CMPD2, DRVx_CMPU3 and DRVx_CMPD3. This register can only be written. Duty cycle = $\text{DRVx\_DR} / \text{DRVx\_ARR} \times 100\%$ Range [0,16383]  Note: When this register is used as a comparison source, the PWM outputs are referenced to the high-side signals. The low-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.7 DRVx_COMUR (CSR: 0x55D/0x59D) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_COMUR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	DRVx_COMUR	Compare Match Interrupt Corresponding DRVx_DR Value During Counter Up-counting

18.16.1.8 DRVx_COMDR (CSR: 0x55E/0x59E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_COMDR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	DRVx_COMDR	Compare Match Interrupt Corresponding DRVx_DR Value During Counter Down-counting

18.16.1.9 DRVx_CMPU1 (CSR: 0x554/0x594) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CMPU1																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CMPU1	Comparison Value of DRVx_CNTR on Rising Edge of Phase A High level is output when DRVx_CMPU1 > DRVx_CNTR; Low level is output when DRVx_CMPU1 ≤ DRVx_CNTR.  Note:

When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.10 DRVx_CMPD1 (CSR: 0x555/0x595) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CMPD1																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CMPD1	Comparison Value of DRVx_CNTR on Falling Edge of Phase A High level is output when $DRVx\_CMPD1 \geq DRVx\_CNTR$; Low level is output when $DRVx\_CMPD1 < DRVx\_CNTR$.  Note: When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.11 DRVx_CMPU2 (CSR: 0x556/0x596) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CMPU2																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CMPU2	Comparison Value of DRVx_CNTR on Rising Edge of Phase B

		High level is output when $DRVx\_CMPU2 > DRVx\_CNTR$; Low level is output when $DRVx\_CMPU2 \leq DRVx\_CNTR$.  Note: When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.12 $DRVx\_CMPD2$ (CSR: 0x557/0x597) ($x = 1/2$)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CMPD2																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	$DRVx\_CMPD2$	Comparison Value of $DRVx\_CNTR$ on Falling Edge of Phase B High level is output when $DRVx\_CMPD2 \geq DRVx\_CNTR$; Low level is output when $DRVx\_CMPD2 < DRVx\_CNTR$.  Note: When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.13 $DRVx\_CMPU3$ (CSR: 0x558/0x598) ($x=1/2$)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RSV																		DRVx_CMPU3																	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w	w	w	w	w	w					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CMPU3	Comparison Value of DRVx_CNTR on Rising Edge of Phase C High level is output when $\text{DRVx\_CMPU3} > \text{DRVx\_CNTR}$; Low level is output when $\text{DRVx\_CMPU3} \leq \text{DRVx\_CNTR}$.  Note: When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.1.14 DRVx_CMPD3 (CSR: 0x559/0x599) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		DRVx_CMPD3													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:14]	RSV	Reserved
[13:0]	DRVx_CMPD3	Comparison Value of DRVx_CNTR on Falling Edge of Phase C High level is output when $\text{DRVx\_CMPD3} \geq \text{DRVx\_CNTR}$; Low level is output when $\text{DRVx\_CMPD3} < \text{DRVx\_CNTR}$.  Note: When this register is used as a comparison source, the PWM outputs are referenced to the low-side signals. The high-side outputs are generated as complementary signals with inserted deadtime.

18.16.2 FOC Control and Status Registers

18.16.2.1 ME_CR (CSR: 0x500)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
RSV																		UDC_DIS		RSV										DRVSYN_EN		RSV		INTCD		TRIG_MD		UDC2_MAEN		RSV	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	-	-	-	-	-	-	-	rw	-	-	rw	rw	rw	-									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	-	0	-	0	0	0	-										

Bit	Name	Description
[31:14]	RSV	Reserved
[13]	UDC_DIS	Sampling Bus Voltage Disable When this bit is enabled, the hardware does not automatically sample the bus voltage. In this case, you can use software to sample the bus voltage, and then write the data to the FOC register. 0: Disable 1: Enable
[12:6]	RSV	Reserved
[5]	DRVSYN_EN	Dual Motors Synchronization Enable When this bit is enabled, the data written to DRV1-related registers is simultaneously updated to DRV2-related registers. Reading DRV1-related registers obtains the value held by the respective register only. 0: Disable 1: Enable Example: When this bit is set to “1” and DRV1_CR[DRVEN] is set to “1”, the hardware automatically sets DRV2_CR[DRVEN] = 1, enabling DRV1_CNTR and DRV2_CNTR to start counting simultaneously.  Note: This synchronization feature ensures that the counters DRV1_CNTR and DRV2_CNTR start simultaneously.
[4]	RSV	Reserved
[3]	INTCD	When this bit is enabled, EXT11 (associated registers shall be properly configured) updates DRVx_CNTR to half of the DRVx_ARR during counting-up operation for EtherCAT synchronization

		0: Disable 1: Enable  Note: EXTI1 generates an interrupt and the interrupt priority can be lower if necessary.
[2]	TRIG_MD	Master Motor ADC2 Enable in Dual-shunt Current Sampling Mode When this bit is enabled, ADC2 channel 13 is used to sample B-phase current (ib) when the master motor works in dual-shunt current sampling mode. A write of “1” is not allowed when both master and slave motors work. 0: Disable 1: Enable  Note: > When this mode is enabled, startup calibration requires the following sequence: first, configure ME_CR[TRIG_MD] and select dual-shunt current sampling mode, and set CK_CR[DRV2CKEN] = 1. Next, set DRV1_FCR2[OFFSET_EN] and DRV2_FCR2[OFFSET_EN] = 1. After this, manually write the NFOC2_IBREF value to NFOC1_IBREF, and finally set CK_CR[DRV2CKEN] = 0. > When the motor reverses, first configure ME_CR[TRIG_MD] and dual-shunt current sampling mode, and set CK_CR[DRV2CKEN] = 1. Then enable DRV1_CR[DDIR] and DRV2_CR[DDIR]. Next, set DRV1_FCR2[OFFSET_EN] and DRV2_FCR2[OFFSET_EN] = 1. After offset calibration, the software swaps NFOC1_IAREF and NFOC1_IBREF. Finally, set CK_CR[DRV2CKEN] = 0.
[1]	UDC2_MAEN	Bus Voltage of Slave Motor Enable When this bit is enabled, FOC module uses bus voltage of slave motor for the calculation. In this case, the bus voltage shall be updated by software. 0: Disable 1: Enable
[0]	RSV	Reserved

18.16.2.2 DRVx_CR (CSR: 0x540/0x580) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRV CNTR DIR	DRV LDM D		RSV			DRV UDM D		DRV UDR N	OCP_MOE MD	MOE MD		DRV MD	DDR	DRV EN	DRV OE
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	-	-	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	DRV CNTR DIR	DRVx_CNTR Counting Direction 0: Up-counting mode 1: Down-counting mode
[14:13]	DRV LDM D	Update Mode for DRVx_ARR and DRVx_CMR 00: Disable 01: DRVx_ARR is updated when CMPx is refreshed. 10: When CMPx is refreshed, both DRVx_ARR and DRVx_CMR are updated, but only once. After this update, this bit is cleared to "0". 11: Both DRVx_ARR and DRVx_CMR are updated when CMPx is refreshed.
[12:10]	RSV	Reserved
[9:8]	DRV UDM D	Update Mode for DRVx_CMPUx/Dx, DRVx_ARR, DRVx_CMR and DRVx_TRG1/2 00: Overflow, underflow or upon FOC computation completion in triangle-wave mode 01: Overflow or underflow 10: Underflow (DRVx_CR[DRVUDRN] = 1) 11: Overflow (DRVx_CR[DRVUDRN] = 1)
[7]	DRV UDR N	Update Mode for DRVx_CMPUx/DRVx_CMPDx in Triangle-wave Mode 0: DRVx_CMPDx is updated on underflow, while DRVx_CMPUx on overflow 1: DRVx_CMPDx and DRVx_CMPUx are updated on underflow or overflow.
[6]	OCP_MOE MD	Over-current Protection Interrupt MOE Enable MOE is cleared to "0" by hardware upon CMP4 over-current protection event. 0: Disable 1: Enable
[5:4]	MOE MD	MOE Cleared and Enabled by Hardware MOE is cleared to "0" and enabled by hardware upon CMP3 over-current protection event.

		00: MOE is not automatically cleared to “0”. 01: MOE is automatically cleared to “0”. 10: MOE is automatically cleared to “0” and enabled (for square-wave control) by hardware upon Driver counter overflow/underflow events or after 5.3μs (the clock runs at 48MHz). 11: MOE is automatically cleared to “0” and enabled (for square-wave control) upon Driver counter overflow/underflow events or after 2.6μs (the clock runs at 48MHz).
[3]	DRVMD	DRVx_CNTR Count Mode 0: Triangular Wave Mode 1: Sawtooth Wave Mode
[2]	DDIR	Output Direction 0: Forward 1: Reverse  Note: In sensorless FOC mode, setting this bit changes motor rotation. In sensor-based FOC mode, it is also required to modify the angle by the software.
[1]	DRVEN	Counter Enable 0: Disable 1: Enable
[0]	DRVOE	Driver Output Enable 0: Disable 1: Enable

18.16.2.3 DRVx_OUT (CSR: 0x541/0x581) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																HREV_EN	LREV_EN	RSV						MOE	RSV	OISWL	OISWH	OISVL	OISVH	OISUL	OISUH
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	-	-	-	-	-	-	rw	-	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	-	-	-	-	-	0	-	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	HREV_EN	High-side Pre-driver Reverse Transfer 0: Disable 1: Enable

[14]	LREV_EN	Low-side Pre-driver Reverse Transfer 0: Disable 1: Enable
[13:8]	RSV	Reserved
[7]	MOE	Main Output Enable This bit selects the sources for three-phase high-side and low-side output signals. It can be set to “1” and “0” by software. When bus overcurrent protection occurs, it is automatically cleared to “0” by hardware to turn off the output. 0: Disable, with output sourced from the idle level set by DRVx_OUT[OISUH]/DRVx_OUT[OISVH]/DRVx_OUT[OISWH]/DRVx_OUT[OISUL]/DRVx_OUT[OISVL]/DRVx_OUT[OISWL]. 1: Enable, with output sourced from the comparison value of the counter.
[6]	RSV	Reserved
[5]	OISWL	W-phase Low-side Output Idle Level See descriptions on OISUH bit
[4]	OISWH	W-phase High-side Output Idle Level See descriptions on OISUH bit
[3]	OISVL	V-phase Low-side Output Idle Level See descriptions on OISUH bit
[2]	OISVH	V-phase High-side Output Idle Level See descriptions on OISUH bit
[1]	OISUL	U-phase Low-side Output Idle Level See descriptions on OISUH bit
[0]	OISUH	U-phase High-side Output Idle Level This bit sets idle level for U-phase high-side output. When DRVx_OUT[MOE] = 0, it outputs idle level to disable MOS. 0: Low Level 1: High Level

18.16.2.4 DRVx_CMR (CSR: 0x547/0x587) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				WHP	WLP	VHP	VLP	UHP	ULP	WHE	WLE	VHE	VLE	UHE	ULE
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11]	WHP	W-phase High-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[10]	WLP	W-phase Low-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[9]	VHP	V-phase High-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[8]	VLP	V-phase Low-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[7]	UHP	U-phase High-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[6]	ULP	U-phase Low-side Polarity Control 0: Normal output 1: Inverted Complementary Output
[5]	WHE	W-phase High-side Output Enable 0: Disable 1: Enable
[4]	WLE	W-phase Low-side Output Enable 0: Disable 1: Enable
[3]	VHE	V-phase High-side Output Enable 0: Disable 1: Enable
[2]	VLE	V-phase Low-side Output Enable 0: Disable 1: Enable
[1]	UHE	U-phase High-side Output Enable 0: Disable 1: Enable
[0]	ULE	U-phase Low-side Output Enable 0: Disable 1: Enable

18.16.2.5 NFOCx_CMRSH (0x30000276/ 0x30010276) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CMRSH															
																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CMRSH	DRVx_CMR Shadow Register

18.16.2.6 DRVx_FCR0 (CSR: 0x548/0x588) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RSV																FDIS_MD			UALBE_SEL		LO_EN		ITPOWMD		RSV		NVQDIS		NVDDIS		NCSAMMD				NCALEN	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	RW	RW				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0	0				

Bit	Name	Description
[31:16]	RSV	Reserved
[15:13]	FDIS_MD	FOC Calculation Mode Selection, which is used to skip some calculation steps to save time for some special applications. 001: It skips BEMF estimation and starts calculations from NFOCx_ZALPHA and NFOCx_ZBETA. It can be used for MR sensor. 010: It skips BEMF estimation and starts calculations from NFOCx_EALPHA and NFOCx_EBETA. 011: It skips the observer to NFOCx_EALPHA/NFOCx_EBETA, and starts from speed calculation. NFOCx_OEMGA is written in the software. 100: It skips the angle calculation, and starts from current loop calculation. NFOCx_THETA is written in the software. It can be used for servo applications.

		101: It calculates only estimated current for SMO. NFOCx_ZALPHA and NFOCx_ZBETA are written in the software to start the calculation. 110: It calculates only the current and voltage (ia/ib/ic and UA/UB/UC), and skips all others. 111: It skips BEMF and speed estimation, and starts calculation from the HFI/LO/OMEGA startup.
[12]	UALBE_SEL	Calculation Source for NFOCx_UDCALP/NFOCx_UDCBET This bit selects NFOCx_UALORG or NFOCx_UALPHA for * NFOCx_UDC calculation to obtain NFOCx_UDCALP that is sent to the observer for NFOCx_US and NFOCx_UTHETA calculation. It can be set as “1” when deadtime compensation is applied to NFOCx_UALPHA and NFOCx_UBETA. 0: NFOCx_UALPHA 1: NFOCx_UALORG
[11]	LO_EN	Low-speed Observer Enable 0: Disable 1: Enable
[10:9]	ITPOWMD	Power Calculation Selection 00: NFOCx_ITRIP, NFOCx_POWER and NFOCx_IS are not calculated. 01: NFOCx_POWER is calculated only, and ADC sampling is configured to obtain NFOCx_ITRIP. 10: NFOCx_ITRIP = NFOCx_US*NFOCx_IS and NFOCx_POWER is calculated. NFOCx_IS is gained by NFOCx_IALPHA and NFOCx_IBETA. 11: NFOCx_ITRIP = NFOCx_US*NFOCx_IS and NFOCx_POWER is calculated. NFOCx_IS is gained by NFOCx_IDFLT and NFOCx_IQFLT
[8]	RSV	Reserved
[7]	NVQDIS	q-axis PI Controller Disable 0: Disable 1: Enable
[6]	NVDDIS	d-axis PI Controller Disable 0: Disable 1: Enable
[5:1]	NCSAMMD	Current Sampling Mode Selection 00000: Single-shunt current sampling mode 00001: Dual-shunt current sampling mode 00010: Triple-shunt current sampling mode 00011: Advanced single-shunt current sampling mode 00100: Single-shunt current sampling ignore mode 00110: Advanced triple-shunt current sampling mode, where dynamic sampling is performed

		00111: Advanced single-shunt current sampling mode 2 01000: Single-shunt dynamic pre- and post-switching current sampling mode 01001: Dual-shunt dual-ADC sampling mode 01010: Advanced single-shunt current sampling mode 3, where U/V/W are windowed and sampled in turn 01011: Advanced single-shunt current sampling mode 4, where sampling is performed at fixed carrier points, specifically measuring i_b and i_c. This mode is specially designed for high-frequency injection (HFI) applications 01100: Advanced single-shunt current sampling mode 5, where dynamic sampling is performed at fixed carrier points. This mode is specifically designed for high-frequency injection (HFI) applications 10001: Triple-shunt manual current sampling mode – similar to standard triple-shunt current sampling mode, but in this mode, DRVx_FCR7 [CBA_MTSAM] must be configured by software to determine the sampling channel.  Note: Please contact us for more details on advanced single-shunt current sampling mode, single-shunt current sampling ignore mode, advanced single-shunt current sampling mode 2, single-shunt dynamic pre- and post-switching current sampling mode, dual-shunt dual-ADC current sampling mode, advanced single-shunt current sampling mode 3, advanced single-shunt current sampling mode 4, and advanced single-shunt current sampling mode 5.
[0]	NCALEN	FOC Calculation Enable After this bit is enabled, FOC calculation and current sampling are performed in every carrier cycle, and the duty cycle is updated to the associated three-phase compare register. 0: Disable 1: Enable

18.16.2.7 DRVx_FCR1 (CSR: 0x549/0x589) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
RSV																WPIAUTO		WPILDEN		FG_MD		WPIMD		RAMP_AUTO		RAMPMD		OME_STA_EN		CT_SEL		ANGMAMD		OME_ABS_EN		FG_IDLE_LEVEL		FG_CALEN		FG_OE	

		0: Disable 1: Enable
[5]	CT_SEL	Time Selection for FOC Calculation 0: Overflow Point of the Driver Counter 1: After Current Sampling (Underflow Point of the Driver Counter in Single-shunt Current Sampling Mode)
[4]	ANGMAMD	Angle Source Manual Mode When this bit is enabled, NFOCx_THETA is not sourced from NFOCx_OTHETA. 0: Disable 1: Enable
[3]	OME_ABS_EN	Estimated Angle Reverse When this bit is enabled, the estimated angle can be reversed. 0: Disable 1: Enable
[2]	FG_IDLE_LEVEL	FG Initial Level Selection 0: Low Level 1: High Level
[1]	FG_CALEN	FG Calculation Enable FG signal is generated when DRVx_FCR1[FG_OE] = 1 and this bit is set to "1". 0: Disable 1: Enable
[0]	FG_OE	FG Generation 0: Disable 1: Enable

18.16.2.8 DRVx_FCR2 (CSR: 0x54A/0x58A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																HFI_ST	OFFSET_EN	FWEAK_MD	FWEAK_EN	RSV	HFI_ST1	OMESTA_MD	NSEG5	UQINJ_EN	RSV			OMELD_EN	HFI_CAL_EN	HFI_TOG_EN	IDQ_MD
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	-	RW	RW	RW	RW	-	-	-	RW	RW	RW	RW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	-	0	0	0	0	-	-	-	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	HFI_ST	UD State in HFI mode

		0: Positive 1: Negative
[14]	OFFSET_EN	OFFSET Calibration After this bit is enabled, the module calibrates the currents ia, ib, and ic/itrip in turn. After calibration, this bit is automatically cleared to “0”. This bit is set to “1” by software, and cleared to “0” by hardware. 0: Disable 1: Enable
[13]	FWEAK_MD	Field-Weakening Mode Selection 0: Mode 0 1: Mode 1
[12]	FWEAK_EN	Flux Weakening Enable 0: Disable 1: Enable
[11]	RSV	Reserved
[10]	HFI_ST1	High-frequency Current Inversion Flag 0: The high-frequency current is not inverted 1: The high-frequency current is inverted
[9]	OMESTA_MD	OMEGA Startup Switching Mode 0: Integral of NFOCx_ETHERTA is sourced from NFOCx_THETA 1: Integral of NFOCx_ETHERTA is sourced from NFOCx_ETHERTA
[8]	NSEG5	5-segment SVPWM Enable 0: Disable 1: Enable
[7]	UQINJ_EN	UQ Injection Enable. After this bit is enabled, NFOCx_UQCPS is automatically updated.
[6:4]	RSV	Reserved
[3]	OMELD_EN	Speed Selection 0: Estimated speed by the observer, which can be used for the subsequent angle calculation 1: Speed calculated by HFI or LO  Note: When this bit is set to “1”, the speed is calculated by HFI or LO but it cannot be used for the subsequent angle calculation.
[2]	HFI_CAL_EN	HFI Enable

		After this bit is enabled, ATAN and PI calculations are performed automatically. 0: Disable 1: Enable
[1]	HFI_TOG_EN	Reverse Voltage in HFI Mode 0: Disable 1: Enable
[0]	IDQ_MD	ID and IQ Mode Selection When this bit is enabled, NFOCx_ID is the average value of the calculated ID and NFOCx_ID0, and NFOCx_IQ is the average value of the calculated IQ and NFOCx_IQ0. 0: Disable 1: Enable

18.16.2.9 DRVx_FCR3 (CSR: 0x54B/0x58B) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV																NOVMDL	DEL_MD		RSV													DLY_EN	SAMPM_EN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	-	-	-	-	-	-	-	-	-	-	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	-	-	-	-	-	-	-	-	0	0	

Bit	Name	Description
[31:15]	RSV	Reserved
[14]	NOVMDL	Overmodulation Enable 0: Disable 1: Enable
[13:12]	DEL_MD	PLL Angle Calculation Mode 00: ATAN 01: sincos 10: Δtheta/EMF after sincos 11: Reserved
[11:2]	RSV	Reserved
[1]	DLY_EN	FOC Calculation Delay Enable It is usually used for high carrier applications and works with DRVx_FCR1[CT_SEL] = 1. 0: Disable 1: Enable

[0]	SAMPM_EN	Manual Sampling Point Enable 0: Disable 1: Enable

18.16.2.10 DRVx_FCR4 (CSR: 0x54C/0x58C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		WPI_CAL	RSV	CUR_SAM_EN	RSV										UDQ_LPF_EN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	-	rW	-	-	-	-	-	-	-	-	-	-	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	-	-	-	-	-	-	-	-	-	-	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13]	WPI_CAL	Outer Loop Calculation Flag 0: Outer loop calculation disabled 1: Outer loop calculation enabled  Note: This bit is read only
[12]	RSV	Reserved
[11]	CUR_SAM_EN	Force Current Sampling Enable When this bit is enabled, current sampling is performed even when DRVx_FCR0[NCALEN] is disabled. 0: Disable 1: Enable
[10:1]	RSV	Reserved
[0]	UDQ_LPF_EN	UD/UQ Low-pass Filter Enable 0: Disable 1: Enable

18.16.2.11 DRVx_FCR5 (CSR: 0x54D/0x58D) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
RSV																			ANGFU_MD		DTC_EN		RSV		ENCODER_STA_CYCLE		UABC_SEL		ANGFU_MAEN		ANGFU_EN		IDQ_FB_SEL		IDQ_LPF_EN		LUTEN_N	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	0	0	0	0	0	0	0	0	0							

Bit	Name	Description
[31:13]	RSV	Reserved
[12:11]	ANGFU_MD	Angle Fusion Source Selection 00: HFI angle 01: Fused angle 1x: SMO/AO/FO angle
[10]	DTC_EN	Deadtime Compensation Enable 0: Disable 1: Enable
[9]	RSV	Reserved
[8:7]	ENCODER_STA_CYCLE	Encoder Auto-Trigger Calculation Cycle Selection 00: Every carrier interrupt 01: Every 2 carrier interrupts 10: Every 4 carrier interrupts 11: Every 8 carrier interrupts
[6:5]	UABC_SEL	Sampling & Sampling Source Selection 00: Sampling is disabled. UDCALPHA / BETA are updated with the calculated voltage from UALPHA / BETA. 01: Sampling is enabled. UDCALPHA / BETA are updated with the calculated voltage from UALPHA / BETA. 10: Sampling is enabled. UDCALPHA / BETA are updated with the sampled voltage (without speed compensation). 11: Sampling is enabled. UDCALPHA / BETA are updated with the sampled voltage (with speed compensation).
[4]	ANGFU_MAEN	Angle Fusion Manual Enable 0: Disable 1: Enable
[3]	ANGFU_EN	Angle Fusion Enable 0: Disable

		1: Enable
[2]	IDQ_FB_SEL	d/q-Axis Current Loop Feedback Value Selection (setting DRVx_FCR5[IDQ_LPF_EN] = 1) 0 : NFOCx_ID / NFOCx_IQ 1 : NFOCx_IDFLT / NFOCx_IQFLT (setting DRVx_FCR5[IDQ_LPF_EN] = 1)
[1]	IDQ_LPF_EN	ID/IQ Low-pass Filter Enable 0: Disable 1: Enable
[0]	LUTEN_N	Sine/Cosine Calculation Method Selection 0: LUT (Lookup Table) 1: CORDIC

18.16.2.12 DRVx_FCR6 (CSR: 0x54E/0x58E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																					CVD_SEL	CVD_EN	ESTU_SEL		ESTID_SEL	MFP_MD	EST_MD				
																					rw	rw	rw	rw	rw	rw	rw	rw			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:11]	RSV	Reserved
[10]	CVD_SEL	Complex Vector QUK_ERR and DUK_ERR Selection 0: QUK_ERR = QUK_FIN - QUK_LIMIT, DUK_ERR = DUK_FIN - DUK_LIMIT 1: QUK_ERR = QUK_FIN - NFOCx_CVQULO, DUK_ERR = DUK_FIN - NFOCx_CVDULO  Note: > QUK_ERR: q-axis voltage output difference of the decoupling controller > QUK_FIN: q-axis voltage output of the decoupling controller before limiting > QUK_LIMIT: q-axis voltage output of the decoupling controller after limiting > DUK_ERR: d-axis voltage output difference of the decoupling controller > DUK_FIN: d-axis voltage output of the decoupling controller before limiting > DUK_LIMIT: d-axis voltage output of the decoupling controller after limiting > NFOCx_CVQULO and NFOCx_CVDULO are static registers and require software updates
[9]	CVD_EN	Current Loop Decoupling Enable 0: Disable

		1: Enable
[8:6]	ESTU_SEL	Q-format for Observer (NFO, AFO and CFO) Reading NFOCx_UDCALP / NFOCx_UDCBET 000: Q15 001: Q14 010: Q13 011: Q12 100: Q11 Others: Q10  Note: It has no effect on NFOCx_UDCALP
[5:4]	ESTID_SEL	ID Source of NFO, AFO, CFO and ID 00: NFOCx_ID 01: NFOCx_IDREF 1x: NFOCx_IDFLT
[3]	MFP_MD	SMO Mode 0: NFOCx_ZALPHA / NFOCx_ZBETA + NFOCx_EALPHA / NFOCx_EBETA 1: NFOCx_ZALPHA / NFOCx_ZBETA + 0 AO: High-speed mode (may affect the low-speed performance) NFO/CFO: Filtering enable
[2:0]	EST_MD	Observer Selection 000: SMO 001: AO 010: CFO 011: NFO 100: AFO

18.16.2.13 DRVx_FCR7 (CSR: 0x54F/0x58F) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CVKP_SEL	CVKP_SEL	CVK11_SEL	CVK11_SEL	CVK12_SEL	CVK12_SEL	CVKO_SEL	CVKO_SEL	RSV					CBA_MTSAM		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	-	-	-	-	-	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	-	-	-	-	-	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	CVKP_SEL	Q-format of Decoupling Controller Coefficient KP 00: Q14 01: Q13 10: Q12 11: Q10
[13:12]	CVKI1_SEL	Q-format of Decoupling Controller Coefficient KI1 00: Q14 01: Q13 10: Q12 11: Q10
[11:10]	CVKI2_SEL	Q-format of Decoupling Controller Coefficient KI2 00: Q14 01: Q13 10: Q12 11: Q10
[9:8]	CVKO_SEL	Q-format for Other Decoupling Controller Coefficients 00: Q14 01: Q13 10: Q12 11: Q11
[7:3]	RSV	Reserved
[2:0]	CBA_MTSAM	Current Sampling in Triple-shunt Manual Current Sampling Mode 001: ib is sampled first, then ia 010: ia is sampled first, then ic 011: ia is sampled first, then ib 100: ic is sampled first, then ib 101: ib is sampled first, then ic 110: ic is sampled first, then ia 000/111: Reserved  Note: CBA_MTSAM takes effect immediately without buffering. Therefore, it cannot be updated between the sampling and calculation of ia/ib/ic

18.16.2.14 DRVx_DTR (CSR: 0x553/0x593) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								DRVx_DTR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	DRVx_DTR	Deadtime Setting $\text{Deadtime} = \text{DRVx\_DTR} \times T_{\text{CLK}}$ For example, if the clock runs at 48MHz and DRVx_DTR = 12, then the deadtime = $12 \times 20.83\text{ns} = 250\text{ns}$  Note: If DRVx_DTR is configured to “0”, deadtime insertion is disabled.

18.16.2.15 DRVx_ARRSH (CSR: 0x55F/0x59F) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_ARRSH															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	DRVx_ARRSH	DRVx_ARR Shadow Register

18.16.3 Time and Sampling Registers

18.16.3.1 NFOCx_TS (0x30000278/0x30010278) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TS	Single-shunt Current Sampling Mode: Minimum window for sampling Dual/triple-shunt Current Sampling Mode: Minimum pulse width for sampling $T_s = \text{sampling window } T_{\text{window}} + \text{deadtime } T_{\text{DT}}$ Range [0,32767] For example, $T_{\text{window}} = 1\mu\text{s}$, $T_{\text{DT}} = 1\mu\text{s}$, $T_s = 2\mu\text{s}$ and carrier cycle = $62.5\mu\text{s}$, then $\text{NFOCx\_TS} = (1 + 1)/62.5 \times 65535 = 2097$ in single-shunt current sampling mode.

18.16.3.2 NFOCx_NTS (0x3000027A/0x3001027A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_NTS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:10]	RSV	Reserved
[9:0]	NFOCx_NTS	Sampling Masking Time in Triple-shunt Current Sampling Mode / Minimum Pulse Width in Advanced Single-shunt Current Sampling Mode In triple-shunt current sampling mode, if the low side is turned on less than NFOCx_NTS, the current of this phase is not sampled and obtained through special process.

		Range [0,1023] For example, the phase current is not sampled if the low side is turned on less than 1 μ s, then NFOCx_NTS = 1000ns/20.8ns = 48

18.16.3.3 NFOCx_TDLY (0x3000027C/0x3001027C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TDLY															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TDLY	Time Configuration for Current Sampling When NFOCx_TDLY = 0, the module samples the current as follows. Single-shunt Current Sampling Mode: Midpoint between deadtime and applied time of active voltage vector Dual/Triple-shunt Current Sampling Mode: Midpoint of vector 000 (Driver counter = 0) Range [-32768,32767] Single-shunt Current Sampling Mode: If NFOCx_TDLY = 5, it delays by 5*T = 104ns to sample the current, and if NFOCx_TDLY = 0xFFFF (complement) or NFOCx_TDLY = -5, it advances by 5*T=104ns. Dual-shunt/Triple-shunt Current Sampling Mode: If NFOCx_TDLY = 5 and driver counter counts down, it samples the current at 5*T = 104ns after an overflow event occurs.

18.16.3.4 NFOCx_TDLYD (0x3000027E/0x3001027E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TDLYD															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TDLYD	Time Configuration for Single-shunt Dynamic Pre- and post-switching Current Sampling Range [-32768,32767]

18.16.3.5 NFOCx_TDTC (0x300001B6/0x300101B6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TDTC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TDTC	Deadtime Compensation in Dual/Triple-shunt Current Sampling Mode Range [0,32767]

18.16.3.6 NFOCx_I1 (0x300001BC/0x300101BC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_I1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_I1	ADC First Sampling Value Range [0,32767]

18.16.3.7 NFOCx_I2 (0x300001BE/0x300101BE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_I2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_I2	ADC Second Sampling Value Range [0,32767]

18.16.3.8 NFOCx_TRG1 (0x30000250/0x30010250) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TRG1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TRG1	DRVx_DR Value Corresponding to Sampling Point NOFCx_I1 Range [0,32767]

18.16.3.9 NFOCx_TRG2 (0x30000252/0x30010252) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_TRG2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_TRG2	DRVx_DR Value Corresponding to Sampling Point NOFCx_I2 Range [0,32767]

18.16.3.10 DRVx_TRG1 (CSR: 0x55B/0x59B) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_TRG1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	DRVx_TRG1	DRVx_DR Value Corresponding to Sampling Point L1

18.16.3.11 DRVx_TRG2 (CSR: 0x55C/0x59C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DRVx_TRG2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	DRVx_TRG2	DRVx_DR Value Corresponding to Sampling Point L2

18.16.3.12 NFOCx_DLYCNT (0x30000396/0x30010396) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DLYCNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DLYCNT	FOC Calculation Delay Time Range [0,32767]

18.16.3.13 NFOCx_ARR (0x30000280/0x30010280) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ARR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ARR	FOC Carrier Frequency It must be the same as DRVx_ARR. Range [0,32767]

18.16.3.14 NFOCx_OSCNT (0x3000037E/0x3001037E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OSCNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OSCNT	Current Offset Calibration Count Value Range [-32768,32767]

18.16.3.15 NFOCx_OSSUM (0x30000380/0x30010380) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_OSSUM																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_OSSUM	Current Offset Calibration Accumulation Value Range [-2147483648,2147483647]

18.16.3.16 NFOCx_CSAM (0x3000038E/ 0x3001038E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CSAM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CSAM	Current Sampling Shadow Register

18.16.4 Voltage Registers

18.16.4.1 NFOCx_UDC (0x30000000/0x30010000) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDC	Sampled Bus Voltage Range [0,32767] For example, the bus voltage is scaled down by 1/6 before feeding into the ADC module, ADC VREF = 5V (namely, the sampling range is 0V ~ 30V) and NFOCx_UDC = 19661(CSR: 0x4CCD), then bus voltage = 19661/32768*5V*6 = 18V.

18.16.4.2 NFOCx_UDCK (0x30000002/0x30010002) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCK	Filter Coefficient for Bus Voltage Sampling. MSB is always 0; Q15 format.

		Range [0,32767]

18.16.4.3 NFOCx_UDCFLT (0x30000004/0x30010004) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NFOCx_UDCFLT

rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_UDCFLT	Filtered Bus Voltage. MSB is always 0; Q31 format. Range [0,2147483647]

18.16.4.4 NFOCx_UDCD (0x30000294/0x30010294) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RSV

NFOCx_UDCD

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCD	d-axis UDC Range [-32768,32767]

18.16.4.5 NFOCx_UDCQ (0x30000296/0x30010296) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RSV

NFOCx_UDCQ

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCQ	q-axis UDC Range [-32768,32767]

18.16.4.6 NFOCx_UALPHA (0x30000220/0x30010220) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UALPHA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UALPHA	α-axis Final Voltage Range [-32768,32767]

18.16.4.7 NFOCx_UBETA (0x30000222/0x30010222) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UBETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UBETA	β-axis Final Voltage Range [-32768,32767]

18.16.4.8 NFOCx_UDCALP (0x300000A4/0x300100A4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCALP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCALP	UDC*UALPHA Range [-32768,32767]

18.16.4.9 NFOCx_UDCBET (0x300000A6/0x300100A6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCBET															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCBET	UDC*UBETA Range [-32768,32767]

18.16.4.10 NFOCx_UALORG (0x30000118/0x30010118) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UALORG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UALORG	α-axis Voltage Range [-32768,32767]

18.16.4.11 NFOCx_UBEORG (0x3000011A/0x3001011A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UBEORG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UBEORG	β-axis Voltage Range [-32768,32767]

18.16.4.12 NFOCx_UALCPS (0x300001DC/0x300101DC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UALCPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UALCPS	Voltage Compensation for NFOCx_UALORG Range [-32768,32767]

18.16.4.13 NFOCx_UBECPS (0x300001DE/0x300101DE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UBECPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UBECPS	Voltage Compensation for NFOCx_UBEORG Range [-32768,32767]

18.16.4.14 NFOCx_OMUNIT (0x3000038C/0x3001038C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OMUNIT															
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMUNIT	Amplification Factor of Overmodulation Range [0,32767]

18.16.5 Terminal Voltage Sampling Registers

18.16.5.1 NFOCx_USOMEK (0x3000025C/0x3001025C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_USOMEK															
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_USOMEK	Terminal Voltage Compensation Coefficient Range [-32768,32767]

18.16.5.2 NFOCx_UA (0x3000025E/0x3001025E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UA	Sampled A-phase Terminal Voltage Range [-32768,32767]

18.16.5.3 NFOCx_UB (0x30000260/0x30010260) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UB															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UB	Sampled B-phase Terminal Voltage Range [-32768,32767]

18.16.5.4 NFOCx_UC (0x30000262/0x30010262) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UC	Sampled C-phase Terminal Voltage Range [-32768,32767]

18.16.5.5 NFOCx_USK (0x30000264/0x30010264) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_USK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_USK	Coefficient of Sampled Terminal Voltage Range [-32768,32767]

18.16.5.6 NFOCx_USOUS (0x30000266/0x30010266) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_USOUS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_USOUS	Amplitude Compensation Coefficient Range [-32768,32767]

18.16.6 Current Registers

18.16.6.1 NFOCx_IA (0x300001C0/0x300101C0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IA	A-phase Current Range [-32768,32767]

18.16.6.2 NFOCx_IB (0x300001C2/0x300101C2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IB															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IB	B-phase Current Range [-32768,32767]

18.16.6.3 NFOCx_IC (0x300001C4/0x300101C4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IC	C-phase Current Range [-32768,32767]

18.16.6.4 NFOCx_IAMAX (0x300001C8/0x300101C8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IAMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IAMAX	Maximum A-phase Current Range [-32768,32767]

18.16.6.5 NFOCx_IBMAX (0x300001CA/0x300101CA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IBMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	nw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IBMAX	Maximum B-phase Current Range [-32768,32767]

18.16.6.6 NFOCx_ICMAX (0x300001C6/0x300101C6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ICMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ICMAX	Maximum C-phase Current Range [-32768,32767]

18.16.6.7 NFOCx_IAREF (0x30000008/0x30010008) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IAREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IAREF	A-phase Current Reference Range [0,32767] For example, if the ADC voltage falls within 0V ~ 5V with a reference value of 2.5V, then NFOCx_IAREF = 2.5V/5V*32768 = 16384 (CSR: 0x4000).

18.16.6.8 NFOCx_IBREF (0x3000000A/0x3001000A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IBREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IBREF	B-phase Current Reference Range [0,32767] For example, if the ADC voltage falls within 0V ~ 5V with a reference value of 2.5V, then NFOCx_IAREF = 2.5V/5V*32768 = 16384 (CSR: 0x4000).

18.16.6.9 NFOCx_ICREF (0x3000000C/0x3001000C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ICREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ICREF	C-phase Current Reference Range [0,32767] For example, if the ADC voltage falls within 0V ~ 5V with a reference value of 2.5V, then NFOCx_IAREF = 2.5V/5V*32768 = 16384 (CSR: 0x4000).

18.16.6.10 NFOCx_IALPHA (0x30000134/0x30010134) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IALPHA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IALPHA	α -axis Current Range [-32768,32767]

18.16.6.11 NFOCx_IBETA (0x30000136/0x30010136) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IBETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IBETA	β -axis Current Range [-32768,32767]

18.16.6.12 NFOCx_ID (0x30000138/0x30010138) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ID															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ID	d-axis Current Range [-32768,32767]

18.16.6.13 NFOCx_IQ (0x3000013A/0x3001013A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IQ															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IQ	q-axis Current Range [-32768,32767]

18.16.6.14 NFOCx_IDFLT (0x3000013C/0x3001013C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_IDFLT																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_IDFLT	ID Filtered Output Range [-2147483648,2147483647]

18.16.6.15 NFOCx IQFLT (0x30000154/0x30010154) (x = 1/2)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

NFOCx_IQFLT

[illegible]

Bit	Name	Description
[31:0]	NFOCx_IQFLT	IQ Filtered Output Range [-2147483648,2147483647]

18.16.6.16 NFOCx IDK (0x30000284/0x30010284) (x = 1/2)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

RSV

NFOC_x IDK[illegible]

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IDK	ID Filter Coefficient Range [-32768,32767]

18.16.6.17 NFOCx_IQK (0x30000286/0x30010286) (x = 1/2)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

RSV

VFOCx_IQK

[illegible]

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IQK	IQ Filter Coefficient Range [-32768,32767]

18.16.6.18 NFOCx_IESTA (0x30000208/0x30010208) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IESTA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IESTA	α -axis Estimated Current Range [-32768,32767]

18.16.6.19 NFOCx_IESTB (0x3000020A/0x3001020A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IESTB															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IESTB	β -axis Estimated Current Range [-32768,32767]

18.16.7 ITRIP and Power Registers

18.16.7.1 NFOCx_IS (0x300003EC/0x300103EC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IS	Amplitude Calculated by NFOCx_IALPHA and NFOCx_IBETA (Square Root) Range [0,32767]

18.16.7.2 NFOCx_ITREF (0x3000000E/0x3001000E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ITREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ITREF	Bus Current Reference Range [0,32767] For example, if the ADC voltage falls within 0V ~ 5V with a reference value of 2.5V, then NFOCx_ITREF = 2.5V/5V*32768 = 16384 (CSR: 0x4000).

18.16.7.3 NFOCx_ITFLT (0x300000D4/0x300100D4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_ITFLT																															
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_ITFLT	Filtered Current NFOCx_ITRIP Range [-2147483648,2147483647]

18.16.7.4 NFOCx_ITRIP (0x300000D8/0x300100D8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ITRIP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ITRIP	Sampled Bus Current for Power Calculation Range [-32768,32767]

18.16.7.5 NFOCx_POWER (0x300000DA/0x300100DA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_POWER															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_POWER	Motor Power Range [-32768,32767]

18.16.7.6 NFOCx_US (0x300000DC/0x300100DC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_US															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_US	Amplitude Calculated by NFOCx_UALPHA and NFOCx_UBETA (Square Root) Range [0,32767]

18.16.7.7 NFOCx_ITK (0x300001D4/0x300101D4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ITK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ITK	Filter Coefficient for itrip Range [-32768,32767]

18.16.7.8 NFOCx_POWK1 (0x300001D6/0x300101D6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_POWK1							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_POWK1	Filter Coefficient 1 for Power Calculation Range [0,255]

18.16.7.9 NFOCx_POWK2 (0x300001D7/0x300101D7) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_POWK2							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_POWK2	Filter Coefficient 2 for Power Calculation Range [0,255]

18.16.8 d-axis Registers

18.16.8.1 NFOCx_DKP (0x30000100/0x30010100) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_DKP													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_DKP	KP Coefficient of PI Controller for d-axis Current Range [0,16383]

18.16.8.2 NFOCx_DKI (0x30000102/0x30010102) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_DKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_DKI	KI Coefficient of PI Controller for d-axis Current Range [0,16383]

18.16.8.3 NFOCx_DMAX (0x30000104/0x30010104) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DMAX	Maximum Output of PI Controller for d-axis Current Range [-32768,32767]

18.16.8.4 NFOCx_DMIN (0x30000106/0x30010106) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DMIN	Minimum Output of PI Controller for d-axis Current Range [-32768,32767]

18.16.8.5 NFOCx_DEK (0x30000108/0x30010108) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DEK	EK of PI Controller for d-axis Current Range [-32768,32767]

18.16.8.6 NFOCx_DEK1 (0x3000010A/0x3001010A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DEK1	EK1 of PI Controller for d-axis Current Range [-32768,32767]

18.16.8.7 NFOCx_DUK (0x3000010C/0x3001010C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_DUK																															
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_DUK	PI Controller Output for d-axis Current Range [-2147483648,2147483647]

18.16.8.8 NFOCx_IDREF (0x300001B8/0x300101B8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IDREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IDREF	d-axis Current Reference Range [-32768,32767]

18.16.8.9 NFOCx_UDCPS (0x300001CC/0x300101CC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCPS	d-axis Voltage Compensation Range [-32768,32767]

18.16.8.10 NFOCx_UDCPS1 (0x300003FC/0x300103FC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCPS1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCPS1	d-axis Voltage Compensation 1 Range [-32768,32767]

18.16.8.11 NFOCx_UDK (0x30000370/0x30010370) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDK	UD Filter Coefficient Range [-32768,32767]

18.16.8.12 NFOCx_UDFLT (0x30000374/0x30010374) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDFLT															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_UDFLT	UD Filtered Output Range [-2147483648,2147483647]

18.16.8.13 NFOCx_UDFIN (0x3000021C/0x3001021C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDFIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDFIN	UD Final Value Range [-32768,32767]

18.16.9 q-axis Registers

18.16.9.1 NFOCx_QKP (0x30000120/0x30010120) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_QKP													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_QKP	KP Coefficient of PI Controller for q-axis Current

		Range [0,16383]

18.16.9.2 NFOCx_QKI (0x30000122/0x30010122) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_QKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_QKI	KI Coefficient of PI Controller for q-axis Current Range [0,16383]

18.16.9.3 NFOCx_QMAX (0x30000124/0x30010124) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QMAX	Maximum Output of PI Controller for q-axis Current Range [-32768,32767]

18.16.9.4 NFOCx_QMIN (0x30000126/0x30010126) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QMIN	Minimum Output of PI Controller for q-axis Current Range [-32768,32767]

18.16.9.5 NFOCx_QEK (0x30000128/0x30010128) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QEK	EK of PI Controller for q-axis Current Range [-32768,32767]

18.16.9.6 NFOCx_QEK1 (0x3000012A/0x3001012A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QEK1	EK1 of PI Controller for q-axis Current Range [-32768,32767]

18.16.9.7 NFOCx_QUK (0x3000012C/0x3001012C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_QUK																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_QUK	PI Controller for q-axis Current Range [-2147483648,2147483647]

18.16.9.8 NFOCx_IQREF (0x300001BA/0x300101BA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IQREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IQREF	q-axis Current Reference Range [-32768,32767]

18.16.9.9 NFOCx_UQCPS (0x300001CE/0x300101CE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UQCPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UQCPS	q-axis Voltage Compensation Range [-32768,32767]

18.16.9.10 NFOCx_UQCPS1 (0x300003FE/0x300103FE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UQCPS1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UQCPS1	q-axis Voltage Compensation 1 Range [-32768,32767]

18.16.9.11 NFOCx_UQK (0x30000372/0x30010372) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UQK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UQK	UQ Filter Coefficient Range [-32768,32767]

18.16.9.12 NFOCx_UQFLT (0x30000378/0x30010378) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																NFOCx_UQFLT															
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_UQFLT	UQ Filter Output Range [-2147483648,2147483647]

18.16.9.13 NFOCx_UQFIN (0x3000021E/0x3001021E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UQFIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UQFIN	UQ Final Value Range [-32768,32767]

18.16.10 Flux-weakening Registers

18.16.10.1 NFOCx_FWKP (0x30000180/0x30010180) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_FWKP													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_FWKP	KP Coefficient of PI Controller for Flux Weakening Range [0,16383]

18.16.10.2 NFOCx_FWKI (0x30000182/0x30010182) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_FWKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_FWKI	KI Coefficient of PI Controller for Flux Weakening Range [0,16383]

18.16.10.3 NFOCx_FWMAX (0x30000184/0x30010184) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWMAX	Maximum Output of PI Controller for Flux Weakening Range [-32768,32767]

18.16.10.4 NFOCx_FWMIN (0x30000186/0x30010186) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWMIN	Minimum Output of PI Controller for Flux Weakening Range [-32768,32767]

18.16.10.5 NFOCx_FWEK (0x30000188/0x30010188) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWEK	EK of PI Controller for Flux Weakening Range [-32768,32767]

18.16.10.6 NFOCx_FWEK1 (0x3000018A/0x3001018A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWEK1	EK1 of PI Controller for Flux Weakening Range [-32768,32767]

18.16.10.7 NFOCx_FWUK (0x3000018C/0x3001018C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																NFOCx_FWUK															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:0]	NFOCx_FWUK	PI Controller Output for Flux Weakening Range [-2147483648,2147483647]

18.16.10.8 NFOCx_KUSF (0x30000192/0x30010192) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_KUSF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_KUSF	US Filtering Coefficient in Flux-weakening Calculation Range [-32768,32767]

18.16.10.9 NFOCx_FWREF (0x30000274/0x30010274) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWREF	Flux-weakening PI Reference Range [-32768,32767]

18.16.10.10 NFOCx_FWIDR (0x3000037C/0x3001037C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FWIDR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FWIDR	Flux-weakening Output in Calculation Mode MOD1 Range [-32768,32767]

18.16.10.11 NFOCx_IDRLIM (0x300003B6/0x300103B6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IDRLIM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IDRLIM	NFOCx_IDREF Amplitude in Flux-weakening Calculation Range [-32768,32767]

18.16.10.12 NFOCx_USFLT (0x300003F0/0x300103F0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_USFLT																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_USFLT	NFOCx_US Filtered Output Range [-2147483648,2147483647]

18.16.11 UQ Injection Registers

18.16.11.1 NFOCx_UIK0 (0x30000238/0x30010238) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIK0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIK0	Frequency Multiplication Coefficient of UQ Compensation Range [-32768,32767]

18.16.11.2 NFOCx_UIK1 (0x3000023A/0x3001023A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIK1	Frequency Multiplication Coefficient of UQ Compensation Range [-32768,32767]

18.16.11.3 NFOCx_UIK2 (0x3000023C/0x3001023C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIK2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIK2	Frequency Multiplication Coefficient of UQ Compensation Range [-32768,32767]

18.16.11.4 NFOCx_UIK3 (0x3000023E/0x3001023E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIK3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIK3	Frequency Multiplication Coefficient of UQ Compensation Range [-32768,32767]

18.16.11.5 NFOCx_UITC0 (0x30000240/0x30010240) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UITC0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UITC0	Phase Angle of UQ Compensation Range [-32768,32767]

18.16.11.6 NFOCx_UIUS0 (0x30000242/0x30010242) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIUS0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIUS0	Amplitude of UQ Compensation Range [-32768,32767]

18.16.11.7 NFOCx_UITC1 (0x30000244/0x30010244) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UITC1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UITC1	Phase Angle of UQ Compensation Range [-32768,32767]

18.16.11.8 NFOCx_UIUS1 (0x30000246/0x30010246) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIUS1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIUS1	Amplitude of UQ Compensation Range [-32768,32767]

18.16.11.9 NFOCx_UITC2 (CSR: 0x30000248/0x30010248) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UITC2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UITC2	Phase Angle of UQ Compensation Range [-32768,32767]

18.16.11.10 NFOCx_UIUS2 (0x3000024A/0x3001024A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIUS2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIUS2	Amplitude of UQ Compensation Range [-32768,32767]

18.16.11.11 NFOCx_UITC3 (0x3000024C/0x3001024C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UITC3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UITC3	Phase Angle of UQ Compensation Range [-32768,32767]

18.16.11.12 NFOCx_UIUS3 (0x3000024E/0x3001024E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UIUS3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UIUS3	Amplitude of UQ Compensation Range [-32768,32767]

18.16.12 HFI Registers

18.16.12.1 NFOCx_HKP (0x300000E0/0x300100E0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_HKP													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_HKP	KP Coefficient of PI Controller for HFI Range [0,16383]

18.16.12.2 NFOCx_HKI (0x300000E2/0x300100E2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_HKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_HKI	KI Coefficient of PI Controller for HFI Range [0,16383]

18.16.12.3 NFOCx_HMAX (0x300000E4/0x300100E4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HMAX	Maximum Output of PI Controller for HFI Range [-32768,32767]

18.16.12.4 NFOCx_HMIN (0x300000E6/0x300100E6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HMIN	Minimum Output of PI Controller for HFI Range [-32768,32767]

18.16.12.5 NFOCx_HEK (0x300000E8/0x300100E8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HEK	EK of PI Controller for HFI Range [-32768,32767]

18.16.12.6 NFOCx_HEK1 (0x300000EA/0x300100EA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HEK1	EK1 of PI Controller for HFI Range [-32768,32767]

18.16.12.7 NFOCx_HUK (0x300000EC/0x300100EC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_HUK																															
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_HUK	PI Controller Output for HFI Range [-2147483648,2147483647]

18.16.12.8 NFOCx_HALPHA (0x300000FC/0x300100FC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HALPHA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HALPHA	α -axis High Frequency Current Envelope Range [-32768,32767]

18.16.12.9 NFOCx_HBETA (0x300000FE/0x300100FE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HBETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HBETA	β -axis High Frequency Current Envelope Range [-32768,32767]

18.16.12.10 NFOCx_HS (0x30000114/0x30010114) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HS	Magnitude Calculation of HALPHA and HBETA (Square Root of Sum of Squares) Range [-32768,32767]

18.16.12.11 NFOCx_ID0 (0x300000F4/0x300100F4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ID0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ID0	d-axis Current by Last FOC Calculation Range [-32768,32767]

18.16.12.12 NFOCx_IQ0 (0x300000F6/0x300100F6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IQ															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IQ0	q-axis Current by Last FOC Calculation Range [-32768,32767]

18.16.12.13 NFOCx_HTCOM (0x3000011E/0x3001011E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HTCOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HTCOM	Angle Compensation for HFI

18.16.13 Observer Registers

18.16.13.1 NFOCx_EKP (0x30000140/0x30010140) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_EKP													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_EKP	KP Coefficient of PI Controller for Observer Range [0,16383]

18.16.13.2 NFOCx_EKI (0x30000142/0x30010142) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_EKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_EKI	KI Coefficient of PI Controller for Observer Range [0,16383]

18.16.13.3 NFOCx_EMAX (0x30000144/0x30010144) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EMAX	Maximum Output of PI Controller for Observer Range [-32768,32767]

18.16.13.4 NFOCx_EMIN (0x30000146/0x30010146) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EMIN	Minimum Output of PI Controller for Observer Range [-32768,32767]

18.16.13.5 NFOCx_EEK (0x30000148/0x30010148) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EEK	EK of PI Controller for Observer Range [-32768,32767]

18.16.13.6 NFOCx_EEK1 (0x3000014A/0x3001014A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EEK1	EK1 of PI Controller for Observer Range [-32768,32767]

18.16.13.7 NFOCx_EUK (0x3000014C/0x3001014C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_EUK																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_EUK	PI Controller Output for Observer Range [-2147483648,2147483647]

18.16.13.8 NFOCx_EK1 (0x300001A8/0x300101A8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EK1	Parameter 1 of Observer Range [-32768,32767]

18.16.13.9 NFOCx_EK2 (0x300001AA/0x300101AA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EK2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EK2	Parameter 2 of Observer Range [-32768,32767]

18.16.13.10 NFOCx_EK3 (0x300001AC/0x300101AC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EK3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EK3	Parameter 3 of Observer Range [-32768,32767]

18.16.13.11 NFOCx_EK4 (0x300001AE/0x300101AE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EK4															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EK4	Parameter 4 of Observer Range [-32768,32767]

18.16.14 SMO Registers

18.16.14.1 NFOCx_KSLIDE (0x300001B0/0x300101B0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_KSLIDE															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_KSLIDE	SMO and Flux Observer Coefficients Range [-32768,32767]

18.16.14.2 NFOCx_MAXERR (0x300001B2/0x300101B2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_MAXERR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_MAXERR	Amplitude Limiting for SMO Range [-32768,32767]

18.16.14.3 NFOCx_MERRRE (0x300001B4/0x300101B4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_MERRRE															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_MERRRE	Reciprocal of Amplitude Limiting for SMO Range [-32768,32767]

18.16.15 Low-speed Observer Registers

18.16.15.1 NFOCx_LK1 (0x300001EC/0x300101EC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK1	Low-speed Observer Coefficient 1 Range [-32768,32767]

18.16.15.2 NFOCx_LK2 (0x300001EE/0x300101EE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK2	Low-speed Observer Coefficient 2 Range [-32768,32767]

18.16.15.3 NFOCx_LK3 (0x300001F0/0x300101F0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK3	Low-speed Observer Coefficient 3 Range [-32768,32767]

18.16.15.4 NFOCx_LK4 (0x300001F2/0x300101F2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK4															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK4	Low-speed Observer Coefficient 4 Range [-32768,32767]

18.16.15.5 NFOCx_LK5 (0x300001F4/0x300101F4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK5															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK5	Low-speed Observer Coefficient 5 Range [-32768,32767]

18.16.15.6 NFOCx_LK6 (0x300001F6/0x300101F6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LK6															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LK6	Low-speed Observer Coefficient 6 Range [-32768,32767]

18.16.15.7 NFOCx_LED (0x300001F8/0x300101F8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LED															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LED	d-axis Low-speed Observer Coefficient Range [-32768,32767]

18.16.15.8 NFOCx_LEQ (0x300001FA/0x300101FA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LEQ															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LEQ	q-axis Low-speed Observer Coefficient Range [-32768,32767]

18.16.15.9 NFOCx_LOME (0x300001FC/0x300101FC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LOME															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LOME	Output Speed of Low-speed Observer Range [-32768,32767]

18.16.16 Flux Observer Registers

18.16.16.1 NFOCx_AFKP (0x300000C0/0x300100C0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFKP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFKP	KP Coefficient of PI Controller for Adaptive Flux Observer (AFO) Range [-32768,32767]

18.16.16.2 NFOCx_AFKI (0x300000C2/0x300100C2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFKI															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFKI	KI Coefficient of PI Controller for AFO Range [-32768,32767]

18.16.16.3 NFOCx_AFMAX (0x300000C4/0x300100C4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFMAX	Maximum Output of PI Controller for AFO Range [-32768,32767]

18.16.16.4 NFOCx_AFMIN (0x300000C6/0x300100C6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFMIN	Minimum Output of PI Controller for AFO Range [-32768,32767]

18.16.16.5 NFOCx_AFEK (0x300000C8/0x300100C8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFEK	EK of PI Controller for AFO Range [-32768,32767]

18.16.16.6 NFOCx_AFEK1 (0x300000CA/0x300100CA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

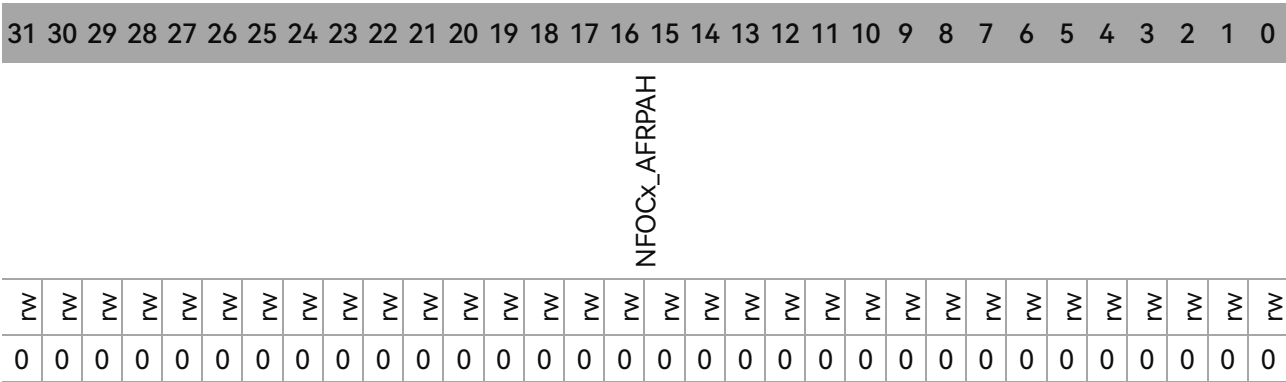
Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFEK1	EK1 of PI Controller for AFO Range [-32768,32767]

18.16.16.7 NFOCx_AFUK (0x300000CC/0x300100CC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_AFUK																															
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

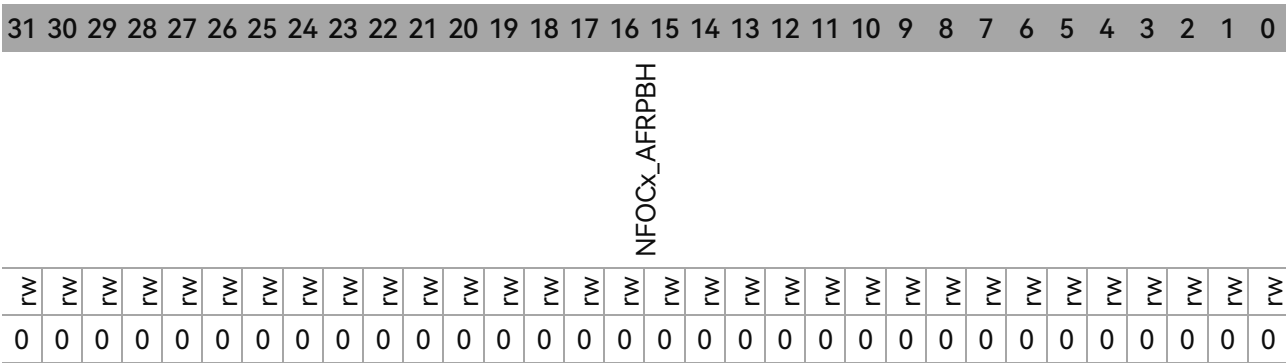
Bit	Name	Description
[31:0]	NFOCx_AFUK	UK of PI Controller for AFO Range [-2147483648,2147483647]]

18.16.16.8 NFOCx_AFRPAH (0x3000015C/0x3001015C) (x = 1/2)



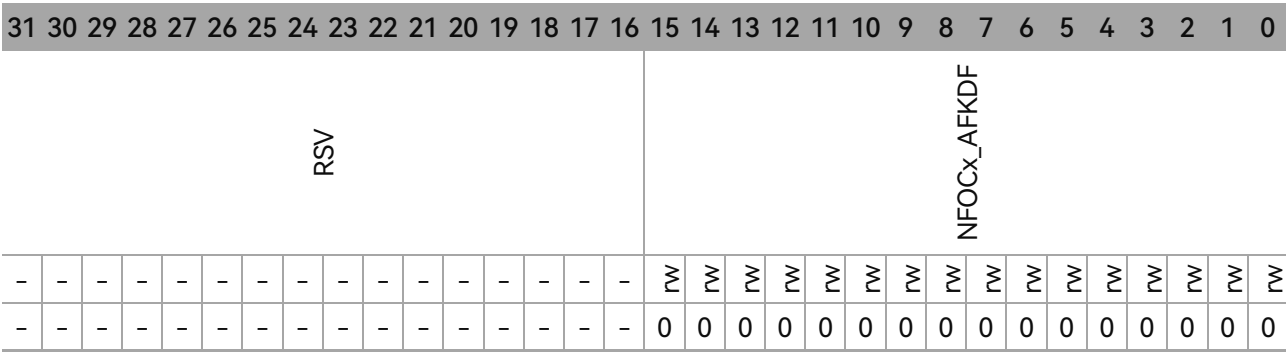
Bit	Name	Description
[31:0]	NFOCx_AFRPAH	Estimated α-axis Flux Linkage of AFO Range [-2147483648,2147483647]

18.16.16.9 NFOCx_AFRPBH (0x30000174/0x30010174) (x = 1/2)



Bit	Name	Description
[31:0]	NFOCx_AFRPBH	Estimated β-axis Flux Linkage of AFO Range [-2147483648,2147483647]

18.16.16.10 NFOCx_AFKDF (0x3000017C/0x3001017C) (x = 1/2)



Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFKDF	AFO Calculation Parameter Range [-32768,32767]

18.16.16.11 NFOCx_AFKAF (0x3000017E/0x3001017E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_AFKAF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_AFKAF	AFO Calculation Parameter Range [-32768,32767]

18.16.16.12 NFOCx_FEK5 (0x300001B0/0x300101B0) (x = 1/2)

NFOCx_FEK5																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_FEK5	AFO Parameter 5 Range [-2147483648,2147483647]

18.16.16.13 NFOCx_FEK6 (0x300001B4/0x300101B4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FEK6															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FEK6	Coefficient 6 of Flux Observer Range [-32768,32767]

18.16.16.14 NFOCx_FEK7 (0x30000BC/0x30010BC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FEK7															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FEK7	Coefficient 7 of Flux Observer Range [-32768,32767]

18.16.16.15 NFOCx_FEK8 (0x300000BE/0x300100BE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FEK8															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FEK8	Coefficient 8 of Flux Observer Range [-32768,32767]

18.16.16.16 NFOCx_AFTHE (0x30000254/0x30010254) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NFOCx_AFTHE

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_AFTHE	AFO Estimated Angle Range [-2147483648,2147483647]

18.16.17 Speed and Angle Registers

18.16.17.1 NFOCx_EALPHA (0x3000015C/0x3001015C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NFOCx_EALPHA

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_EALPHA	Estimated α -axis BEMF by Observer Range [-2147483648,2147483647]

18.16.17.2 NFOCx_EBETA (0x30000174/0x30010174) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0												
NFOCx_EBETA																																											
																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_EBETA	Estimated β-axis BEMF by Observer Range [-2147483648,2147483647]

18.16.17.3 NFOCx_ETHETA (0x30000178/0x30010178) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0											
NFOCx_ETHETA																																										
																⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										

Bit	Name	Description
[31:0]	NFOCx_ETHETA	Estimated Angle by Observer Range [-2147483648,2147483647]

18.16.17.4 NFOCx_ZALORG (0x3000017C/0x3001017C) (x=1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ZALORG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ZALORG	Estimated α -axis BEMF Range [-32768,32767]

18.16.17.5 NFOCx_ZBEORG (0x3000017E/0x3001017E) ($x=1/2$)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ZBEORG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ZBEORG	Estimated β -axis BEMF Range [-32768,32767]

18.16.17.6 NFOCx_EMF (0x300001E0/0x300101E0) ($x = 1/2$)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_EMF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_EMF	Estimated BEMF Amplitude Range [-32768,32767]

18.16.17.7 NFOCx_OMEGA (0x30000204/0x30010204) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OMEGA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMEGA	Final Speed of the Motor Range [-32768,32767]

18.16.17.8 NFOCx_FTCK (0x3000019E/0x3001019E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FTCK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FTCK	Dynamic Compensation Coefficient of Feedback Angle; Q8 format Range [-32768,32767]

18.16.17.9 NFOCx_FGBASE (0x300001D8/0x300101D8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FGBASE															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FGBASE	Speed Reference for FG Calculation Range [-32768,32767]

18.16.17.10 NFOCx_OMEMI2 (0x300001A2/0x300101A2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OMEMI2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMEMI2	Minimum Speed Corresponding to NFOCx_KLPP Range [-32768,32767]

18.16.17.11 NFOCx_THECOM (0x300001A4/0x300101A4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_THECOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_THECOM	Static Compensation for Output Angle Range [-32768,32767]



Note:
If compensation is required for NFOCx_ETHETA, please set NFOCx_FTCOM.

18.16.17.12 NFOCx_FTCOM (0x300001A6/0x300101A6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FTCOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FTCOM	Static Compensation for Feedback Angle Range [-32768,32767]

18.16.17.13 NFOCx_OMEFLT (0x3000020C/0x3001020C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_OMEFLT																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_OMEFLT	First-order Filtered OMEGA Range [-2147483648,2147483647]

18.16.17.14 NFOCx_OMEFL2 (0x30000210/0x30010210) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_OMEFL2																															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_OMEFL2	Second-order Filtered OMEGA Range [-2147483648,2147483647]

18.16.17.15 NFOCx_ZALPHA (0x30000214/0x30010214) (x=1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ZALPHA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ZALPHA	α-axis BEMF before Filtering Range [-32768,32767]

18.16.17.16 NFOCx_ZBETA (0x30000216/0x30010216) (x=1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ZBETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ZBETA	β -axis BEMF before Filtering Range [-32768,32767]

18.16.17.17 NFOCx_KLPF (0x30000218/0x30010218) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_KLPF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_KLPF	LPF Coefficient of the Observer Range [-32768,32767]

18.16.17.18 NFOCx_FTCPS (CSR: 0x30000268/0x30010268) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FTCPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FTCPS	Calculated Dynamic Compensation Angle $NFOCx\_FTCPs = NFOCx\_FTCK * NFOCx\_OMEFL2 * NFOCx\_FBASE$ Range [-32768,32767]

18.16.17.19 NFOCx_FTHETA (0x3000026A/0x3001026A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FTHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FTHETA	Feedback Angle by Observer Range [-32768,32767]

18.16.17.20 NFOCx_ITHETA (0x300003EE/0x300103EE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ITHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ITHETA	Angle Calculated by NFOCx_IALPHA and NFOCx_IBETA (ATAN) Range [-32768,32767]

18.16.17.21 NFOCx_THETA (0x30000158/0x30010158) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_THETA																															
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_THETA	Final Angle Range [-2147483648,2147483647]

18.16.17.22 NFOCx_OTHETA (0x30000258/0x30010258) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OTHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OTHETA	Angle before Compensation by Integral of NFOCx_OMEGA Range [-32768,32767]

18.16.17.23 NFOCx_DELOTHE (0x3000028C/0x3001028C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_DELOTHE																															
⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_DELOTHE	NFOCx_OTHETA Variation Range [-2147483648,2147483647]

18.16.17.24 NFOCx_DELETEHE (0x30000290/0x30010290) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_DELETEHE																															
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_DELETEHE	NFOCx_ETHERA Variation Range [-2147483648,2147483647]

18.16.17.25 NFOCx_UTHETA (0x300000DE/0x300100DE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UTHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UTHETA	Angle Calculated by NFOCx_UALPHA and NFOCx_UBETA (ATAN) Range [-32768,32767]

18.16.17.26 NFOCx_FBASE (0x300001A0/0x300101A0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FBASE															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FBASE	Speed Reference Range [-32768,32767]

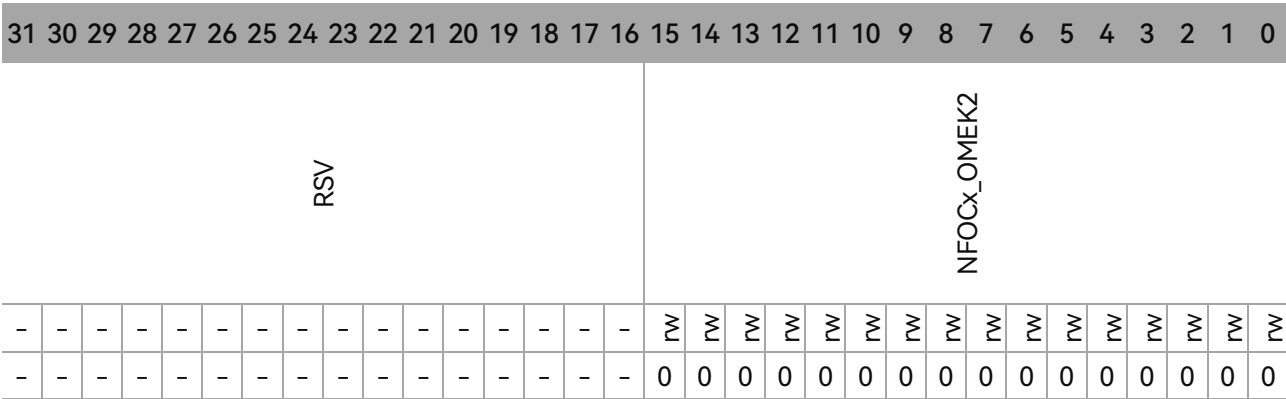
18.16.18 OMEGA Startup Registers

18.16.18.1 NFOCx_OMEGAK (0x30000288/0x30010288) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OMEGAK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

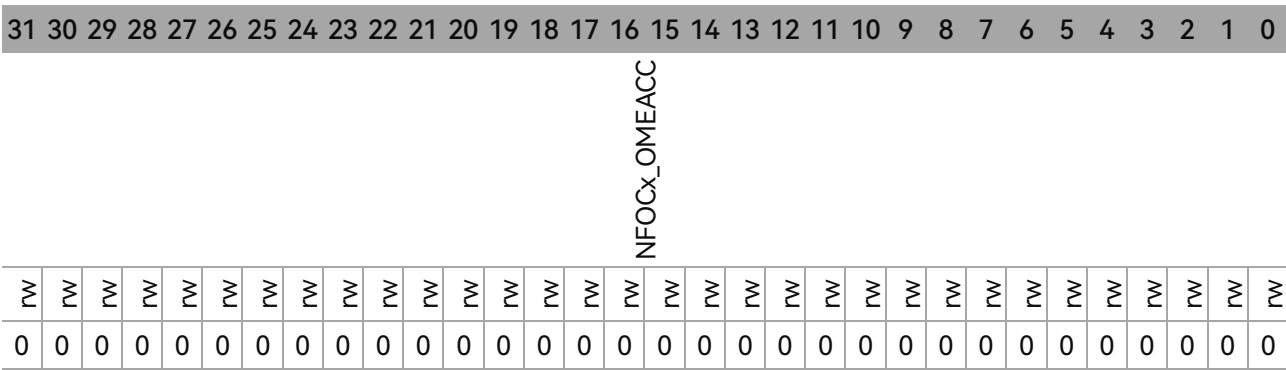
Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMEGAK	First-order Filter Coefficient for OMEGA Range [-32768,32767]

18.16.18.2 NFOCx_OMEK2 (0x3000028A/0x3001028A) (x = 1/2)



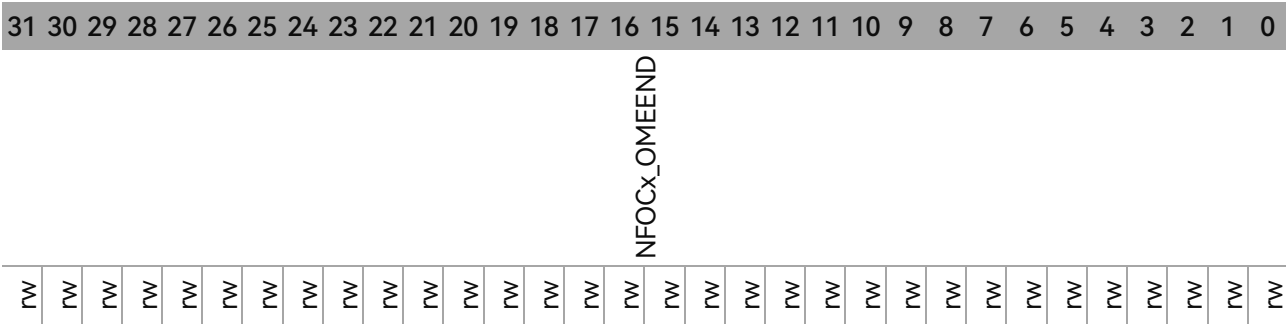
Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMEK2	Second-order Filter Coefficient for OMEGA Range [-32768,32767]

18.16.18.3 NFOCx_OMEACC (0x30000194/0x30010194) (x = 1/2)



Bit	Name	Description
[31:0]	NFOCx_OMEACC	Speed Increment for Omega Startup Range [-2147483648,2147483647]

18.16.18.4 NFOCx_OMEEND (0x30000198/0x30010198) (x = 1/2)



[illegible]

Bit	Name	Description
[31:0]	NFOCx_OMEEND	Maximum Speed for Omega Startup Range [-2147483648,2147483647]

18.16.18.5 NFOCx OMEMIN (0x3000019C/0x3001019C) (x = 1/2)

[illegible]

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OMEMIN	Minimum Speed for Omega Startup Range [-32768,32767]

18.16.19 Outer Loop Registers

18.16.19.1 NFOCx WKP (0x30000160/0x30010160) (x = 1/2)

[illegible]

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4

[13:0]	NFOCx_WKP	KP Coefficient of PI Controller for Outer-loop Control Range [0,16383]

18.16.19.2 NFOCx_WKI (0x30000162/0x30010162) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PI_QSEL		NFOCx_WKI													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:14]	PI_QSEL	PI Parameter Format 00: Q15 01: Q12 10: Q8 11: Q4
[13:0]	NFOCx_WKI	KI Coefficient of PI Controller for Outer-loop Control Range [0,16383]

18.16.19.3 NFOCx_WMAX (0x30000164/0x30010164) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WMAX	Maximum Output of PI Controller for Outer-loop Control Range [-32768,32767]

18.16.19.4 NFOCx_WMIN (0x30000166/0x30010166) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WMIN	Minimum Output of PI Controller for Outer-loop Control Range [-32768,32767]

18.16.19.5 NFOCx_WEK (0x30000168/0x30010168) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WEK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WEK	EK of PI Controller for Outer-loop Control Range [-32768,32767]

18.16.19.6 NFOCx_WEK1 (0x3000016A/0x3001016A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WEK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WEK1	EK1 of PI Controller for Outer-loop Control Range [-32768,32767]

18.16.19.7 NFOCx_WUK (0x3000016C/0x3001016C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFOCx_WUK																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:0]	NFOCx_WUK	PI Controller Output for Outer-loop Control Range [-2147483648,2147483647]

18.16.19.8 NFOCx_WREF (0x300001D0/0x300101D0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WREF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WREF	Outer Loop Reference Value Range [0,32767]

18.16.19.9 NFOCx_WFDB (0x300001D2/0x300101D2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WFDB															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WFDB	Outer Loop Feedback Value Range [-32768,32767]

18.16.19.10 NFOCx_WUCPS (0x3000033C/0x3001033C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WUCPS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WUCPS	Outer-loop Compensation Value Range [0,32767]

18.16.19.11 NFOCx_WUFIN (0x3000033E/0x3001033E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_WUFIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_WUFIN	Outer-loop Final Value Range [0,32767]

18.16.20 Ramping Registers

18.16.20.1 NFOCx_RATAR (0x300001E4/0x300101E4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_RATAR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_RATAR	Target Ramping Output Range [-32768,32767]

18.16.20.2 NFOCx_RAOUT (0x300001E6/0x300101E6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_RAOUT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_RAOUT	Ramping Output Range [-32768,32767]

18.16.20.3 NFOCx_RAINC (0x300001E8/0x300101E8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_RAINC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_RAINC	Upward Step Value Range [-32768,32767]

18.16.20.4 NFOCx_RADEC (0x300001EA/0x300101EA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_RADEC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_RADEC	Downward Step Value Range [-32768,32767]

18.16.21 Motor Protection Registers

18.16.21.1 DRVx_PER (CSR: 0x544/0x584) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																					LOCK2EN	LOCK1EN	LOCK0EN	ODCIF_EN	OSPD_AUTO	OVEL_AUTO	PL_AUTO	LOCK_AUTO	OUPV_AUTO		SOC_P AUTO
																					rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:11]	RSV	Reserved
[10]	LOCK2EN	MLP Detection 2 Enable When this bit is enabled, the motor lock condition is detected when the ratio of motor speed to BEMF exceeds the set threshold. 0: Disable 1: Enable
[9]	LOCK1EN	MLP Detection 1 Enable When this bit is enabled, the motor lock conditions is detected when the motor speed exceeds the maximum threshold.

		0: Disable 1: Enable
[8]	LOCK0EN	MLP Detection 0 Enable When this bit is enabled, the motor lock conditions is detected when the motor speed is lower than the minimum threshold. 0: Disable 1: Enable
[7]	ODCIF_EN	Carrier Interrupt Timeout Protection Enable 0: Disable 1: Enable
[6]	OSPD_AUTO	Over-speed Auto Calculation Enable (Once per carrier cycle) 0: Disable 1: Enable
[5]	OVEL_AUTO	Speed Deviation Auto Calculation Enable (Once per outer-loop cycle) 0: Disable 1: Enable
[4]	PL_AUTO	Phase Loss Auto Calculation Enable (Once per electrical cycle) 0: Disable 1: Enable
[3]	LOCK_AUTO	MLP Auto Calculation Enable (Once per Systick cycle) 0: Disable 1: Enable
[2:1]	OUVP_AUTO	Software OVP/UVLO Auto Calculation Enable 00: Disable 01: Once per carrier cycle 10: Once per Systick cycle 11: No effect
[0]	SOC_P_AUTO	Software OCP Auto Calculation Enable (Once per carrier cycle) 0: Disable 1: Enable

18.16.21.2 DRVx_PTR (CSR: 0x545/0x585) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																						RAMP_TRG	WPI_TRG	OSPD_TRG	OVEL_TRG	RSV		PL_TRG	LOCK_TRG	OUPV_TRG	SOCPTRG
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w1	w1	w1	w1	-	-	w1	w1	w1	w1
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	-	-	0	0	0	0

Bit	Name	Description
[31:10]	RSV	Reserved
[9]	RAMP_TRG	Ramping Calculation Trigger The ramping calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[8]	WPI_TRG	Outer-loop Calculation Trigger An outer-loop calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[7]	OSPD_TRG	Over-speed Protection Calculation Trigger The over-speed protection calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[6]	OVEL_TRG	Speed Deviation Protection Calculation Trigger The over-speed protection calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[5:4]	RSV	Reserved
[3]	PL_TRG	Phase Loss Protection Calculation Trigger A phase loss protection calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[2]	LOCK_TRG	MLP Calculation Trigger A MLP calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[1]	OUPV_TRG	OVP/UVLO Calculation Trigger An OVP/UVLO calculation is performed once after “1” is written. Writing “0” to this bit or reading it has no effect.
[0]	SOCPTRG	OCP Calculation Trigger An OCP calculation is automatically performed once by software after “1” is written. Writing “0” to this bit or reading it has no effect.

18.16.21.3 DRVx_PSR (CSR: 0x546/0x586) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CBA			RSV			RIF	ODCIFIF	OSPDIF	OVELIF	PLIF	LOCKIF	UVPIF	OVPIF	SOCPIF	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:15]	RSV	Reserved
[14:12]	CBA	Sector Selection 000: No effect 001: II Sector 010: VI Sector 011: I Sector 100: IV Sector 101: III Sector 110: V Sector 111: No effect
[11:9]	RSV	Reserved
[8]	RIF	Abnormal Current Reference Flag (No interrupt is generated) This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[7]	ODCIFIF	Carrier Interrupt Timeout Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[6]	OSPDIF	Over-speed Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[5]	OVELIF	Speed Deviation Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[4]	PLIF	Phase Loss Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software.

		0: No Interrupt Pending 1: Interrupt Pending
[3]	LOCKIF	MLP Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[2]	UVPIF	UVLO Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[1]	OVPIF	OVP Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending
[0]	SOCPIF	Software OCP Interrupt Flag This bit is set to “1” by hardware, and cleared to “0” by software. 0: No Interrupt Pending 1: Interrupt Pending

18.16.21.4 NFOCx_IRLOW (0x30000010/0x30010010) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IRLOW															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IRLOW	Minimum Current Reference If the current is lower than this value, an abnormal current reference is reported Range [0,32767]

18.16.21.5 NFOCx_IRUPP (0x30000012/0x30010012) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_IRUPP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_IRUPP	Maximum Current Reference If the current is higher than this value, an abnormal current reference is reported. Range [0,32767]

18.16.21.6 NFOCx_OVP (0x30000014/0x30010014) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_OVP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_OVP	OVP Threshold Range [0,32767]

18.16.21.7 NFOCx_OVPARR (0x30000016/0x30010016) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_OVPARR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_OVPARR	Target Count Value for OVP Range [0,255]

18.16.21.8 NFOCx_OVPCNT (0x30000017/0x30010017) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_OVPCNT							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_OVPCNT	Count Value for OVP Range [0,255]

18.16.21.9 NFOCx_UVP (0x30000018/0x30010018) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UVP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UVP	UVLO Threshold Range [0,32767]

18.16.21.10 NFOCx_UVPARR (0x3000001A/0x3001001A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_UVPARR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_UVPARR	Target Count Value for UVLO Range [0,255]

18.16.21.11 NFOCx_UVPCNT (0x3000001B/0x3001001B) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_UVPCNT							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_UVPCNT	Count Value for UVLO Range [0,255]

18.16.21.12 NFOCx_SOCP (0x3000001C/0x3001001C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_SOCP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_SOCP	Software OCP Threshold Range [0,32767]

18.16.21.13 NFOCx_SOCARR (0x3000001E/0x3001001E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								NFOCx_SOCARR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_SOCARR	Target Count Value for Software OCP Range [0,255]

18.16.21.14 NFOCx_SOCPCNT (0x3000001F/0x3001001F) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																			
RSV																								NFOCx_SOCPCNT																										
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw																		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0																			

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	NFOCx_SOCPCNT	Count value for Software OCP Range [0,255]

18.16.21.15 NFOCx_LKSMIN (0x30000020/0x30010020) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LKSMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LKSMIN	Minimum MLP Speed Corresponding to LOCK0 Range [0,32767]

18.16.21.16 NFOCx_LKSMAX (0x30000022/0x30010022) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LKSMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LKSMAX	Maximum MLP Speed Corresponding to LOCK1 Range [0,32767]

18.16.21.17 NFOCx_LOCKK (0x30000024/0x30010024) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LOCKK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LOCKK	MLP Speed and BEMF Corresponding to LOCK2; Q8 Format Range [0,32767]

18.16.21.18 NFOCx_LKARR (0x30000028/0x30010028) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LKARR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LKARR	Target count value for MLP, which is applicable to three MLP conditions. Range [0,32767]

18.16.21.19 NFOCx_LKCNT (0x3000002A/0x3001002A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_LKCNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_LKCNT	Count value for MLP, which is applicable to three MLP conditions. Range [0,65535]

18.16.21.20 NFOCx_NCURRE (0x3000002C/0x3001002C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_NCURRE															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_NCURRE	Phase Loss Protection Current Range [0,32767]

18.16.21.21 NFOCx_PLK (0x3000002E/0x3001002E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_PLK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	w	r	w	r	w	r	w	r	w	r	w	r	w	r	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_PLK	Multiple of Phase Loss Protection Current; Q8 Format Range [0,32767]

18.16.22 CORDIC Registers

18.16.22.1 ME_COR (CSR: 0x50C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							COR7	COR6	COR5	COR4	COR3	COR2	COR1	COR0	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	COR7	CORDIC7 Called by Software 0: Disable 1: Enable The software calls CORDIC7 to calculate ATAN and square root. The steps are as follows: 1. Write NFOC2_XI3 and NFOC2_YI3 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC2_US3 and NFOC2_THETA3 are read by software to obtain the CORDIC result.

[6]	COR6	CORDIC6 Called by Software 0: Disable 1: Enable The software calls CORDIC6 to calculate ATAN and square root. The steps are as follows: 1. Write NFOC2_XI2 and NFOC2_YI2 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC2_US2 and NFOC2_THETA2 are read by software to obtain the CORDIC result.
[5]	COR5	CORDIC5 Called by Software 0: Disable 1: Enable The software calls CORDIC5 to calculate sin and cos. The steps are as follows: 1. Write NFOC2_XI1, NFOC2_YI1 and NFOC2_THETA1 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC2_XO1 and NFOC2_YO1 are read by software to obtain the CORDIC result.
[4]	COR4	CORDIC4 Called by Software 0: Disable 1: Enable The software calls CORDIC4 to calculate sin and cos. The steps are as follows: 1. Write NFOC2_XI0, NFOC2_YI0 and NFOC2_THETA0 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC2_XO0 and NFOC2_YO0 are read by software to obtain the CORDIC result.
[3]	COR3	CORDIC3 Called by Software 0: Disable 1: Enable The software calls CORDIC3 to calculate ATAN and square root. The steps are as follows: 1. Write NFOC_XI3 and NFOC_YI3 in the software; 2. This bit is set to “1” by software;

		3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC1_US3 and NFOC1_THETA3 are read by software to obtain the CORDIC result.
[2]	COR2	CORDIC2 Called by Software 0: Disable 1: Enable The software calls CORDIC2 to calculate ATAN and square root. The steps are as follows: 1. Write NFOC1_XI2 and NFOC1_YI2 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC1_US2 and NFOC1_THETA2 are read by software to obtain the CORDIC result.
[1]	COR1	CORDIC1 Called by Software 0: Disable 1: Enable The software calls CORDIC1 to calculate sin and cos. The steps are as follows: 1. Write NFOC1_XI1, NFOC1_YI1 and NFOC1_THETA1 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC1_XO1 and NFOC1_YO1 are read by software to obtain the CORDIC result.
[0]	COR0	CORDIC0 Called by Software 0: Disable 1: Enable The software calls CORDIC0 to calculate sin and cos. The steps are as follows: 1. Write NFOC1_XI0, NFOC1_YI0 and NFOC1_THETA0 in the software; 2. This bit is set to “1” by software; 3. After CORDIC calculation, this bit is set to “0” by hardware, and NFOC1_XO0 and NFOC1_YO0 are read by software to obtain the CORDIC result.

18.16.22.2 NFOCx_XI0 (0x30000030/0x30010030) (x=1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XI0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XI0	X-axis input of CORDIC0 (CORDIC4) Range [-32768,32767]

18.16.22.3 NFOCx_YI0 (0x30000032/0x30010032) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YI0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YI0	Y-axis input of CORDIC0 (CORDIC4) Range [-32768,32767]

18.16.22.4 NFOCx_THETA0 (0x30000036/0x30010036) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_THETA0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_THETA0	Angle input of CORDIC0 (CORDIC4) Range [-32768,32767]

18.16.22.5 NFOCx_XO0 (0x30000038/0x30010038) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XO0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XO0	X-axis output of CORDIC0 (CORDIC4) Range [-32768,32767]

18.16.22.6 NFOCx_YO0 (0x3000003A/0x3001003A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YO0															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YO0	Y-axis output of CORDIC0 (CORDIC4) Range [-32768,32767]

18.16.22.7 NFOCx_XI1 (0x3000003C/0x3001003C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XI1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XI1	X-axis input of CORDIC1 (CORDIC5) Range [-32768,32767]

18.16.22.8 NFOCx_YI1 (0x3000003E/0x3001003E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YI1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YI1	Y-axis input of CORDIC1 (CORDIC5) Range [-32768,32767]

18.16.22.9 NFOCx_THETA1 (0x30000042/0x30010042) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_THETA1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_THETA1	Angle input of CORDIC1 (CORDIC5) Range [-32768,32767]

18.16.22.10 NFOCx_XO1 (0x30000044/0x30010044) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XO1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XO1	X-axis output of CORDIC1 (CORDIC5) Range [-32768,32767]

18.16.22.11 NFOCx_YO1 (0x30000046/0x30010046) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YO1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YO1	Y-axis output of CORDIC1 (CORDIC5) Range [-32768,32767]

18.16.22.12 NFOCx_XI2 (0x30000048/0x30010048) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XI2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XI2	X-axis input of CORDIC2 (CORDIC6) Range [-32768,32767]

18.16.22.13 NFOCx_YI2 (0x3000004A/0x3001004A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YI2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YI2	Y-axis input of CORDIC2 (CORDIC6) Range [-32768,32767]

18.16.22.14 NFOCx_US2 (0x3000004C/0x3001004C) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_US2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_US2	Square root output of CORDIC2 (CORDIC6) Range [0,32767]

18.16.22.15 NFOCx_THETA2 (0x3000004E/0x3001004E) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_THETA2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_THETA2	ATAN output of CORDIC2 (CORDIC6) Range [-32768,32767]

18.16.22.16 NFOCx_XI3 (0x30000050/0x30010050) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_XI3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_XI3	X-axis input of CORDIC3 (CORDIC7) Range [-32768,32767]

18.16.22.17 NFOCx_YI3 (0x30000052/0x30010052) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_YI3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_YI3	Y-axis input of CORDIC3 (CORDIC7) Range [-32768,32767]

18.16.22.18 NFOCx_US3 (0x30000054/0x30010054) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_US3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_US3	Square root output of CORDIC3 (CORDIC7) Range [-32768,32767]

18.16.22.19 NFOCx_THETA3 (0x30000056/0x30010056) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_THETA3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_THETA3	ATAN output of CORDIC3 (CORDIC7) Range [-32768,32767]

18.16.23 Angle Fusion Registers

18.16.23.1 NFOCx_HTHETA (0x30000116/0x30010116) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_HTHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_HTHETA	Angle Obtained from Arctangent Calculation of NFOCx_HALPHA and NFOCx_HBETA Range [-32768,32767]

18.16.23.2 NFOCx_ATHETA (0x300001E2/0x300101E2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_ATHETA															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_ATHETA	Angle Obtained from Arctangent Calculation of NFOCx_EALPHA and NFOCx_EBETA Range [-32768,32767]

18.16.23.3 NFOCx_FUWEI (0x3000021A/0x3001021A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FUWEI															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FUWEI	Weighting Coefficient/Value for HFI Angle in Angle Fusion When DRVx_FCR5[ANGFU_MAEN] = 1, NFOCx_FUWEI is the weighting value of HFI angle with Q15 format Range [0,32767]; When DRVx_FCR5[ANGFU_MAEN] = 0, NFOCx_FUWEI is the weighting coefficient of HFI angle with Q16 format Range [0,32767]

18.16.23.4 NFOCx_FUMAX (0x300003E8/0x300103E8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FUMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FUMAX	Maximum Speed Threshold for Angle Fusion

18.16.23.5 NFOCx_FUMIN (0x300003EA/0x300103EA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_FUMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_FUMIN	Minimum Speed Threshold for Angle Fusion

18.16.24 Current Loop Decoupling Registers

18.16.24.1 NFOCx_CVK1 (0x300003CC/0x300103CC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVK1															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVK1	Parameter 1 for Decoupling Controller

18.16.24.2 NFOCx_CVK2 (0x300003E0/0x300103E0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVK2															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVK2	Parameter 2 for Decoupling Controller

18.16.24.3 NFOCx_CVK3 (0x300003CE/0x300103CE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVK3															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVK3	Parameter 3 for Decoupling Controller

18.16.24.4 NFOCx_CVDK4 (0x300003D0/0x300103D0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVDK4															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVDK4	d-axis Parameter 4 for Decoupling Controller

18.16.24.5 NFOCx_CVDK5 (0x30003D4/0x300103D4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVDK5															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVDK5	d-axis Parameter 5 for Decoupling Controller

18.16.24.6 NFOCx_CVQK4 (0x300003D2/0x300103D2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVQK4															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVQK4	q-axis Parameter 4 for Decoupling Controller

18.16.24.7 NFOCx_CVQK5 (0x300003D6/0x300103D6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVQK5															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVQK5	q-axis Parameter 5 for Decoupling Controller

18.16.24.8 NFOCx_CVKI2D (0x30000112/0x30010112) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVKI2D															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVKI2D	KI2 Coefficient of d-axis PI Controller for Decoupling Controller

18.16.24.9 NFOCx_CVKI2Q (0x30000132/0x30010132) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVKI2Q															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVKI2Q	KI2 Coefficient of q-axis PI Controller for Decoupling Controller

18.16.24.10 NFOCx_CVDULO (0x30000302/0x30010302) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVDULO															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVDULO	Output Limit of d-axis Inverter for Decoupling Controller (Software Update)

18.16.24.11 NFOCx_CVQULO (0x3000032A/0x3001032A) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVQULO															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVQULO	Output Limit of q-axis Inverter for Decoupling Controller (Software Update)

18.16.24.12 NFOCx_UDCMAX (0x300003E4/0x300103E4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCMAX	Maximum Amplitude of UDC for Decoupling Controller

18.16.24.13 NFOCx_UDCMIN (0x300003E6/0x300103E6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCMIN	Minimum Amplitude of UDC for Decoupling Controller

18.16.24.14 NFOCx_UDCLIM (0x300003E2/0x300103E2) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_UDCLIM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_UDCLIM	UDC Output of Decoupling Controller

18.16.24.15 NFOCx_CVDUK (0x30000110/0x30010110) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVDUK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVDUK	Complex Vector Decoupling Calculation Parameter

18.16.24.16 NFOCx_CVKI2D (0x30000112/0x30010112) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVKI2D															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVKI2D	Complex Vector Decoupling Calculation Parameter

18.16.24.17 NFOCx_CVQUK (0x30000130/0x30010130) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_CVQUK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_CVQUK	Complex Vector Decoupling Calculation Parameter

18.16.24.18 NFOCx_DCOM (0x300003D8/0x300103D8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DCOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DCOM	Complex Vector Decoupling Calculation Parameter

18.16.24.19 NFOCx_DAS (0x300003DA/0x300103DA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DAS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DAS	Complex Vector Decoupling Calculation Parameter

18.16.24.20 NFOCx_QCOM (0x300003DC/0x300103DC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QCOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QCOM	Complex Vector Decoupling Calculation Parameter

18.16.24.21 NFOCx_QAS (0x300003DE/0x300103DE) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QAS															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QAS	Complex Vector Decoupling Calculation Parameter

18.16.24.22 NFOCx_DUKF (0x300003F4/0x300103F4) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_DUKF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_DUKF	d-axis Output of Decoupling Controller

18.16.24.23 NFOCx_QUKF (0x300003F6/0x300103F6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																NFOCx_QUKF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	NFOCx_QUKF	q-axis Output of Decoupling Controller

18.17 6N Pre-driver Registers (FU7564Q1/FU7565Q1/FU7574Q1)

18.17.1 FU7564Q1/FU7574Q1 6N Pre-driverx Registers

18.17.1.1 SLPF_R (0x02)

7	6	5	4	3	2	1	0
RSV			SLP_FORCE	REBOOT	VDS_CLR	FAULT_CLR	ANA_RDY
-	-	-	rw	w1	w1	w1	r
-	-	-	0	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	SLP_FORCE	See descriptions in section SLPF_R (0x02)SLPF_R (0x02).
[3]	REBOOT	Writing “1” restarts the pre-driverx and resets the associated registers to their defaults
[2]	VDS_CLR	Writing “1” releases the V _{DS} OVP state
[1]	FAULT_CLR	See descriptions in section SLPF_R (0x02)SLPF_R (0x02).
[0]	ANA_RDY	Pre-driverx initialization is completed

18.17.1.2 STAU_R (0x07)

7	6	5	4	3	2	1	0
VCCOVP	VCCOVW	VCCUVP	VBOVPU	VBSATU	VBUVU	FAULT_VDSL	FAULT_VDSHU
r	r	r	r	r	r	r	r
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	VCCOVP	VCC _x OVP Flag 0: VCC _x < V _{CCOVPF} , the chip works normally 1: VCC _x > V _{CCOVPR} , VCC _x OVP is triggered
[6]	VCCOVW	VCC _x OVP Warning Flag 0: VCC _x < V _{CCOVWF} , no VCC _x OVP warning is triggered 1: VCC _x > V _{CCOVWR} , VCC _x OVP warning is triggered
[5]	VCCUVP	VCC _x UVLO Flag 0: VCC _x > V _{CCUVR} , the chip works normally 1: VCC _x < V _{CCUVF} , VCC _x UVLO is triggered

[4]	VBOVPU	U-phase High-side VB-VS OVP Flag 0: $V_{BUx} - V_{SUx} < V_{BOVF}$, the chip works normally 1: $V_{BUx} - V_{SUx} > V_{BOVR}$, the OVP is triggered
[3]	VBSATU	U-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVU	U-phase High-side VB-VS UVLO Flag 0: $V_{BUx} - V_{SUx} > V_{BUVR}$, the chip works normally 1: $V_{BUx} - V_{SUx} < V_{BUVF}$, the UVLO is triggered
[1]	FAULT_VDSL	U-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHU	U-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.1.3 STAV_R (0x08)

7	6	5	4	3	2	1	0
RSV	VBBUVP	TSD	VBOVPV	VBSATV	VBUVV	FAULT_VDSL	FAULT_VDSHU
-	r	r	r	r	r	r	r
-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	VBBUVP	VBB _x UVLO Flag 0: $V_{BBx} > V_{BBUVR}$, the chip works normally 1: $V_{BBx} < V_{BBUVF}$, VBB _x UVLO is triggered
[5]	TSD	6N Pre-driverx Thermal Shutdown Protection Flag 0: No thermal shutdown protection is detected 1: Thermal shutdown protection is detected
[4]	VBOVPV	V-phase High-side VB-VS OVP Flag 0: $V_{BVx} - V_{SVx} < V_{BOVF}$, the chip works normally 1: $V_{BVx} - V_{SVx} > V_{BOVR}$, the OVP is triggered
[3]	VBSATV	V-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVV	V-phase High-side VB-VS UVLO Flag 0: $V_{BVx} - V_{SVx} > V_{BUVR}$, the chip works normally 1: $V_{BVx} - V_{SVx} < V_{BUVF}$, the UVLO is triggered

[1]	FAULT_VDSLW	V-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHW	V-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.1.4 STAW_R (0x09)

7	6	5	4	3	2	1	0
RSV			VBOVPW	VBSATW	VBUVW	FAULT_VDSLW	FAULT_VDSHW
-	-	-	r	r	r	r	r
-	-	-	0	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	VBOVPW	W-phase High-side VB-VS OVP Flag 0: $V_{BWx} - V_{SWx} < V_{BOVF}$, the chip works normally 1: $V_{BWx} - V_{SWx} > V_{BOVR}$, the OVP is triggered
[3]	VBSATW	W-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVW	W-phase High-side VB-VS UVLO Flag 0: $V_{BWx} - V_{SWx} > V_{BUVR}$, the chip works normally 1: $V_{BWx} - V_{SWx} < V_{BUVF}$, the UVLO is triggered
[1]	FAULT_VDSLW	W-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHW	W-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.1.5 I2C_R (0x83)

7	6	5	4	3	2	1	0
CP_DIS	RSV		I2C_PU	RSV			
rw	-	-	rw	-	-	-	-
0	-	-	0	-	-	-	-

Bit	Name	Description
[7]	CP_DIS	Charge Pump Disable 0: Disable 1: Enable

[6:5]	RSV	Reserved
[4]	I2C_PU	I ² C Bus Pull-up Enable 0: Disable 1: Enable
[3:0]	RSV	Reserved

18.17.1.6 DIS_R (0x84)

7	6	5	4	3	2	1	0
VDS_DIS	TSD_DIS	RSV			VBBUVP_DIS	VCCOVP_DIS	VCCUVP_DIS
rw	rw	-	-	-	rw	rw	rw
0	0	-	-	-	0	0	0

Bit	Name	Description
[7]	VDS_DIS	MOSFET VDS OVP Disable 0: Disable 1: Enable
[6]	TSD_DIS	6N Pre-driverx TSD Disable 0: Disable 1: Enable
[5:3]	RSV	Reserved
[2]	VBBUVP_DIS	VBB_x UVLO Disable 0: Disable 1: Enable
[1]	VCCOVP_DIS	VCC_x OVP Disable 0: Disable 1: Enable
[0]	VCCUVP_DIS	VCC_x UVLO Disable 0: Disable 1: Enable

18.17.1.7 VTHU_R (0x86)

7	6	5	4	3	2	1	0
VDD5ON_SEL	LIN_WK_DIS	VTHU					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	VDD5ON_SEL	VDD5_x/Internal Power Supply Switching 0: Internal Power Supply Based on Sleep Status 1: Automatic Switching
[6]	LIN_WK_DIS	LIN Wake-up Disable

		0: Disable 1: Enable
[5:0]	VTHU	U-phase High-side V_{DS} Over-voltage Threshold $V_{DSTHU} = n * 50\text{mV}$ (0V ~ 3.15V and 1.6V by default)

18.17.1.8 VTLU_R (0x87)

7	6	5	4	3	2	1	0
RSV	MON_WK_DIS	VTLU					
-	rw	rw	rw	rw	rw	rw	rw
-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	MON_WK_DIS	MONx Wake-up Disable 0: Disable 1: Enable
[5:0]	VTLU	U-phase Low-side V_{DS} Over-voltage Threshold $V_{DSTLU} = n * 50\text{mV}$ (0V ~ 3.15V and 1.6V by default)

18.17.1.9 TVDU_R (0x88)

7	6	5	4	3	2	1	0
RSV		TVDU					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	TVDU	U-phase V_{DS} OVP Timer Duration $t_{VDQU} = n * 100\text{ns}$ (0 μs ~ 6.3 μs)

18.17.1.10 VTHV_R (0x89)

7	6	5	4	3	2	1	0
RSV		VTHV					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	VTHV	V-phase High-side V_{DS} Over-voltage Threshold $V_{DSTHV} = n * 50\text{mV}$ (0V ~ 3.15V and 1.6V by default)

18.17.1.11 VTLV_R (0x8A)

7	6	5	4	3	2	1	0
RSV		VTLV					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	VTLV	V-phase Low-side V_{DS} Over-voltage Threshold $V_{DSTLV} = n * 50\text{mV}$ (0V ~ 3.15V and 1.6V by default)

18.17.1.12 TVDV_R (0x8B)

7	6	5	4	3	2	1	0
RSV		TVDV					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	TVDV	V-phase V_{DS} OVP Timer Duration $t_{VDQV} = n * 100\text{ns}$ (0 μs ~ 6.3 μs)

18.17.1.13 VTHW_R (0x8C)

7	6	5	4	3	2	1	0
RSV		VTHW					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	VTHW	W-phase High-side V_{DS} Over-voltage Threshold $V_{DSTHW} = n * 50\text{mV}$ (0V ~ 3.15V and 1.6V by default)

18.17.1.14 VTLW_R (0x8D)

7	6	5	4	3	2	1	0
RSV		VTLW					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description

[7:6]	RSV	Reserved
[5:0]	VTBW	W-phase Low-side V_{DS} Over-voltage Threshold $V_{DSTLW} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.1.15 TVDW_R (0x8E)

7	6	5	4	3	2	1	0
FAULTNS_PU	FAULTNS_OE	TVBW					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	FAULTNS_PU	FAULTNxS Pin Pull-up Enable 0: Disable 1: Enable
[6]	FAULTNS_OE	FAULTNxS Pin Output Enable 0: Disable 1: Enable
[5:0]	TVBW	W-phase V_{DS} OVP Timer Duration $t_{VDQW} = n * 100ns$, (0 μs ~ 6.3 μs)

18.17.2 FU7565Q1 6N Pre-driver1 Registers

18.17.2.1 SLPF_R (0x02)

7	6	5	4	3	2	1	0
RSV			SLP_FORCE	REBOOT	VDS_CLR	FAULT_CLR	ANA_RDY
-	-	-	rw	w1	w1	w1	r
-	-	-	0	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	SLP_FORCE	See descriptions in section SLPF_R (0x02).
[3]	REBOOT	Writing “1” restarts the pre-driver1 and resets the associated registers to their defaults
[2]	VDS_CLR	Writing “1” releases the VDS OVP state
[1]	FAULT_CLR	See descriptions in section SLPF_R (0x02).
[0]	ANA_RDY	Pre-driver1 initialization is completed

18.17.2.2 TSD_R (0x06)

7	6	5	4	3	2	1	0
RSV							TSD
-	-	-	-	-	-	-	r
-	-	-	-	-	-	-	0

Bit	Name	Description
[7:1]	RSV	Reserved
[0]	TSD	6N Pre-driver1 TSD Flag 0: No TSD is detected 1: TSD is detected

18.17.2.3 STAU_R (0x07)

7	6	5	4	3	2	1	0
RSV	VCCOVP	VCCUVP	VBOVPU	VBSATU	VBUVU	FAULT_VDSL	FAULT_VDSHU
-	r	r	r	r	r	r	r
-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	VCCOVP	VCC OVP Flag 0: $V_{CC} < V_{CCOVP}$, the chip works normally 1: $V_{CC} > V_{CCOVP}$, VCC OVP is triggered
[5]	VCCUVP	VCC UVLO Flag 0: $V_{CC} > V_{CCUVP}$, the chip works normally 1: $V_{CC} < V_{CCUVP}$, VCC UVLO is triggered
[4]	VBOVPU	U-phase High-side VB-VS OVP Flag 0: $V_{BU1} - V_{SU1} < V_{BOVP}$, the chip works normally 1: $V_{BU1} - V_{SU1} > V_{BOVP}$, OVP is triggered
[3]	VBSATU	U-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVU	U-phase High-side VB-VS UVLO Flag 0: $V_{BU1} - V_{SU1} > V_{BUVP}$, the chip works normally 1: $V_{BU1} - V_{SU1} < V_{BUVP}$, UVLO is triggered
[1]	FAULT_VDSL	U-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHU	U-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.2.4 STAV_R (0x08)

7	6	5	4	3	2	1	0
RSV	VBBUVP	VBBOK	VBOVPV	VBSATV	VBUVV	FAULT_VDSL	FAULT_VDSHV
-	r	r	r	r	r	r	r
-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	VBBUVP	VBB UVLO Flag 0: $V_{BB} > V_{BBUVR}$, the chip works normally 1: $V_{BB} < V_{BBUVR}$, VBB UVLO is triggered
[5]	VBBOK	VBB Power Ready Flag 0: VBB power not ready 1: VBB power ready
[4]	VBOVPV	V-phase High-side VB-VS OVP Flag 0: $V_{BV1} - V_{SV1} < V_{BOVF}$, the chip works normally 1: $V_{BV1} - V_{SV1} > V_{BOVR}$, OVP is triggered
[3]	VBSATV	V-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVV	V-phase High-side VB-VS UVLO Flag 0: $V_{BV1} - V_{SV1} > V_{BUVR}$, the chip works normally 1: $V_{BV1} - V_{SV1} < V_{BUVR}$, UVLO is triggered
[1]	FAULT_VDSL	V-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHV	V-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.2.5 STAW_R (0x09)

7	6	5	4	3	2	1	0
RSV			VBOVPW	VBSATW	VBUVW	FAULT_VDSLW	FAULT_VDSHW
-	-	-	r	r	r	r	r
-	-	-	0	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	VBOVPW	W-phase High-side VB-VS OVP Flag 0: $V_{BW1} - V_{SW1} < V_{BOVF}$, the chip works normally 1: $V_{BW1} - V_{SW1} > V_{BOVR}$, OVP is triggered

[3]	VBSATW	W-phase High-side VB-VS Charging Voltage Status 0: The charging voltage is not saturated 1: The charging voltage is saturated
[2]	VBUVW	W-phase High-side VB-VS UVLO Flag 0: $V_{BW1} - V_{SW1} > V_{BUVR}$, the chip works normally 1: $V_{BW1} - V_{SW1} < V_{BUVF}$, UVLO is triggered
[1]	FAULT_VDSLW	W-phase Low-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected
[0]	FAULT_VDSHW	W-phase High-side V_{DS} OVP Flag 0: No V_{DS} OVP is detected 1: V_{DS} OVP is detected

18.17.2.6 I2C_R (0x84)

7	6	5	4	3	2	1	0
BUCK_DIS	CP_DIS	RSV	I2C_PU	RSV			
rw	rw	-	rw	-	-	-	-
0	0	-	0	-	-	-	-

Bit	Name	Description
[7]	BUCK_DIS	Buck DC-DC Converter Disable 0: Disable 1: Enable
[6]	CP_DIS	Charge Pump Disable 0: Disable 1: Enable
[5]	RSV	Reserved
[4]	I2C_PU	I ² C Bus Pull-Up Enable 0: Disable 1: Enable
[3:0]	RSV	Reserved

18.17.2.7 DIS_R (0x85)

7	6	5	4	3	2	1	0
VDS_DIS	TSD_DIS	RSV			VBBUVP_DIS	VCCOVP_DIS	VCCUVP_DIS
rw	rw	-	-	-	rw	rw	rw
0	0	-	-	-	0	0	0

Bit	Name	Description
[7]	VDS_DIS	MOSFET V_{DS} OVP Disable 0: Disable 1: Enable

[6]	TSD_DIS	6N Pre-driver1 TSD Disable 0: Disable 1: Enable
[5:3]	RSV	Reserved
[2]	VBBUVP_DIS	VBB UVLO Disable 0: Disable 1: Enable
[1]	VCCOVP_DIS	VCC OVP Disable 0: Disable 1: Enable
[0]	VCCUVP_DIS	VCC UVLO Disable 0: Disable 1: Enable

18.17.2.8 LIN_PU_R (0x86)

7	6	5	4	3	2	1	0
RSV			VDD5FEN	FAULTN_PU	RSV		LIN_PU_DIS
-	-	-	rw	rw	-	-	rw
-	-	-	0	0	-	-	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	VDD5FEN	VDD5 Forced Enable 1: Keep VDD5 powered during sleep 0: Power down VDD5 during sleep
[3]	FAULTN_PU	FAULTN1 Pin Pull-Up Enable 0: Disable 1: Enable
[2:1]	RSV	Reserved
[0]	LIN_PU_DIS	LIN Bus Pull-Up Disable 0: Disable 1: Enable

18.17.2.9 VTHU_R (0x87)

7	6	5	4	3	2	1	0
VDD5ON_SEL	LIN_WK_DIS	VTHU					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	VDD5ON_SEL	VDD5/Internal Power Supply Switching 0: Automatic switching 1: Internal power supply based on sleep status

[6]	LIN_WK_DIS	LIN Wake-Up Disable 0: Disable 1: Enable
[5:0]	VTHU	U-phase High-side V_{DS} OVP Threshold $V_{DSTHU} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.10 VTLU_R (0x88)

7	6	5	4	3	2	1	0
MON_PU_DIS	MON_WK_DIS	VTLU					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	MON_PU_DIS	MON1 Internal Pull-Up Disable 0: Disable 1: Enable
[6]	MON_WK_DIS	MON1 Wake-up Disable 0: Disable 1: Enable
[5:0]	VTLU	U-phase Low-side V_{DS} OVP Threshold $V_{DSTLU} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.11 TVDU_R (0x89)

7	6	5	4	3	2	1	0
RSV		TVDU					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	TVDU	U-phase V_{DS} OVP Timer Duration $t_{VDQU} = n * 100ns$ (0 μs ~ 6.3 μs)

18.17.2.12 VTHV_R (0x8A)

7	6	5	4	3	2	1	0
RSV		VTHV					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description

[7:6]	RSV	Reserved
[5:0]	VTHV	V-phase High-side V_{DS} OVP Threshold $V_{DSTHV} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.13 VTLV_R (0x8B)

7	6	5	4	3	2	1	0
OSC2_FSEL		VTLV					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	OSC2_FSEL	Buck DC-DC Converter Clock Frequency Selection 00: 125kHz 01: 250kHz 10: 500kHz 11: 1MHz
[5:0]	VTLV	V-phase Low-side V_{DS} OVP Threshold $V_{DSTLV} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.14 TVDV_R (0x8C)

7	6	5	4	3	2	1	0
RSV		TVDV					
-	-	rw	rw	rw	rw	rw	rw
-	-	0	0	0	0	0	0

Bit	Name	Description
[7:6]	RSV	Reserved
[5:0]	TVDV	V-phase V_{DS} OVP Timer Duration $t_{VDQV} = n * 100ns$ (0 μs ~ 6.3 μs)

18.17.2.15 VTHW_R (0x8D)

7	6	5	4	3	2	1	0
OSC2_SS		VTHW					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7:6]	OSC2_SS	Buck DC-DC converter clock spread spectrum selection 00: Disabled 01: Triangular

		10: Random 11: Hybrid
[5:0]	VTHW	W-phase High-side V_{DS} OVP Threshold $V_{DSTHW} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.16 VTLW_R (0x8E)

7	6	5	4	3	2	1	0
RSV	VCCOVS	VTLW					
-	rw	rw	rw	rw	rw	rw	rw
-	0	0	0	0	0	0	0

Bit	Name	Description
[7]	RSV	Reserved
[6]	VCCOVS	VCC overvoltage/undervoltage level selection 00: 48V 01: 24V
[5:0]	VTLW	W-phase Low-side V_{DS} OVP Threshold $V_{DSTLW} = n * 50mV$ (0V ~ 3.15V and 1.6V by default)

18.17.2.17 TVDW_R (0x8F)

7	6	5	4	3	2	1	0
FAULTNS_PU	FAULTNS_OE	TVDW					
rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	FAULTNS_PU	FAULTN1S Pin Pull-Up Enable 0: Disable 1: Enable
[6]	FAULTNS_OE	FAULTN1S Pin Output Enable 0: Disable 1: Enable
[5:0]	TVDW	W-phase V_{DS} OVP Timer Duration $t_{VDQW} = n * 100ns$, (0 μs ~ 6.3 μs)

19 PFC

19.1 PFC Operating Instructions

19.1.1 PFC Introduction

Power Factor Correction (PFC) improves power efficiency and power density, optimizes voltage control the system and reduces electromagnetic compatibility and electromagnetic interference.



Note:

PFC1 is enabled only when PFC_CR0[PFCEN] is set to “1”. To enable both PFC1 and PFC2, PFC_CR0[IAC2EN] must be also set to “1”.

PFC module has the following features:

- Full-automatic hardware
- ADC automatic sampling
- Over-current protection and cycle-by-cycle current limiting
- Interleaved two-phase boost PFC

Figure 19-1 Structure Diagram of PFC Module

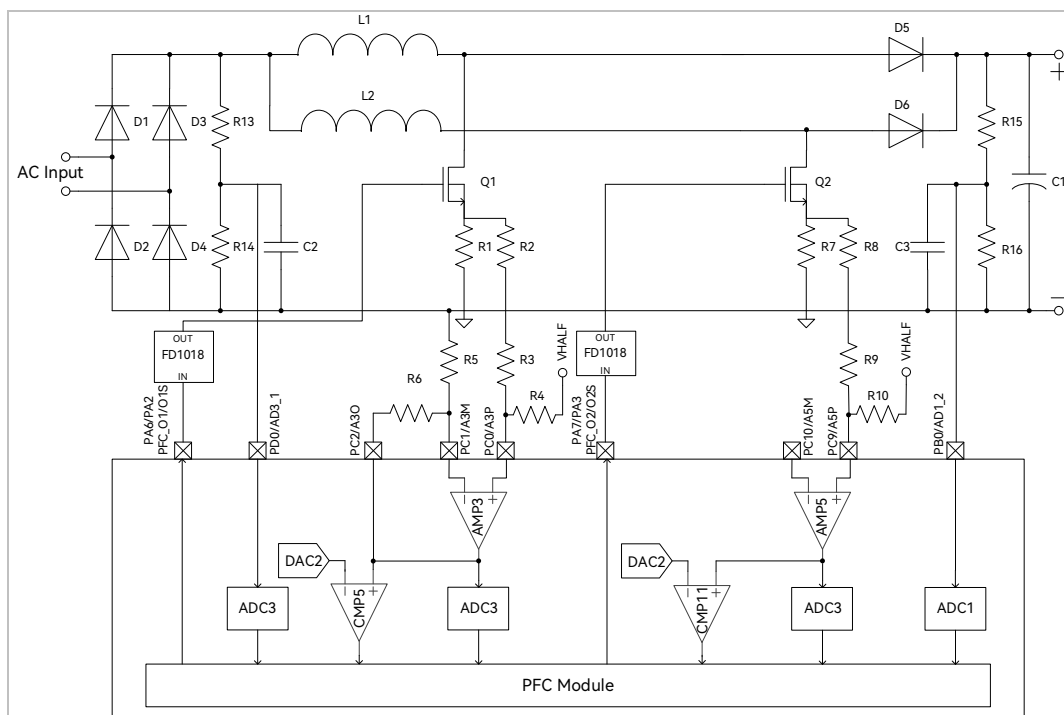
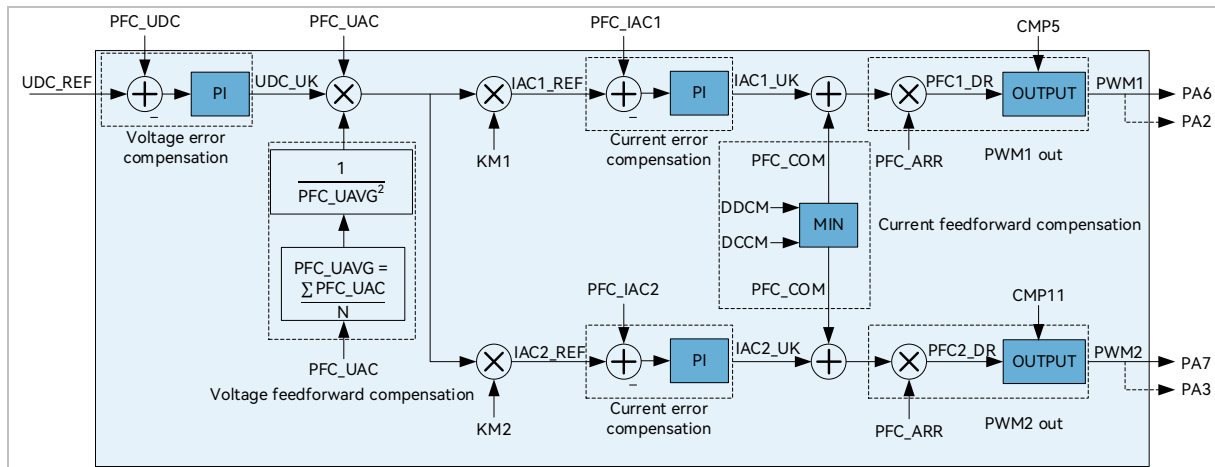


Figure 19-2 Block Diagram of PFC Module



PFC module includes voltage error compensation module, voltage feed-forward compensation module, 2*current error compensation modules, current feed-forward compensation module, current sampling calibration module and 2*PWM output modules.

19.1.2 Voltage Error Compensation Module

Voltage error compensation module is outer loop of the PFC module. Its input is the difference between UDC_REF (user-defined DCV reference) and UDC (sampled DCV by ADC), which is transmitted to PI controller to generate control output UDC_UK .

Outer loop frequency = Inner loop frequency/ $UDC\_ARR = 48M/(PFC\_ARR*2)/UDC\_ARR$.

19.1.3 Voltage Feed-forward Compensation Module

The voltage feed-forward compensation module is mainly used to maintain a constant output power under unstable input AC voltage.

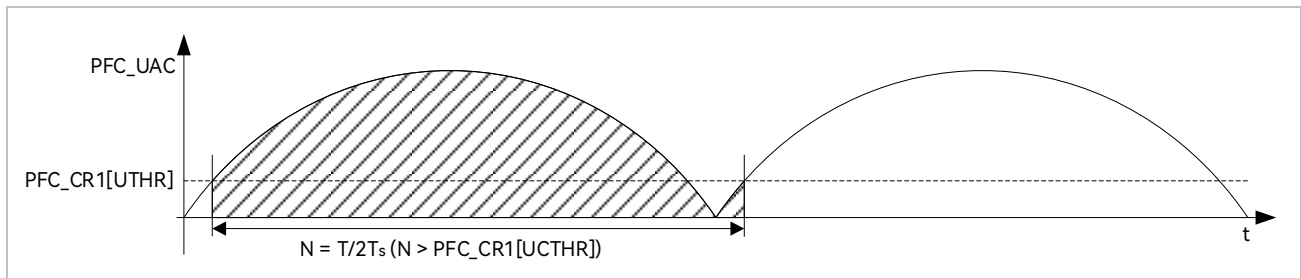
19.1.4 Average Voltage Calculation

PFC_UAVG is the rectified average voltage of AC voltage PFC_UAC . The PFC module calculates PFC_UAVG by hardware automatically. For some special applications, this feature can be disabled and PFC_UAVG is calculated by software. PFC_UAVG is calculated as:

$$PFC\_UAVG = \frac{\sum PFC\_UACx}{N}$$

where, PFC_UAC is the sampling AC voltage, N is the sampling number in time period T_s .

Figure 19-3 Calculation of PFC_UAVG



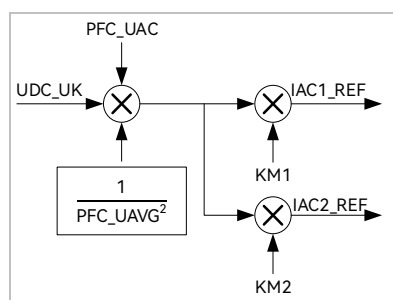
PFC_CR0[UAVGCDIS] is set to “0” to start the calculation of PFC_UAVG by hardware. The calculation period of PFC_UAVG is a half period of power frequency T . PFC_CR1[UTHR] is the first and the last value of sampling voltage. T_s is the sampling period of PFC_UAC. PFC_CR1[UTHR] is the minimum number of PFC_UAC sampling. When PFC_UAC in this sampling period is bigger than PFC_CR1[UTHR] and the former one is smaller, this sampling period is the start or the end of a calculation period. To decrease sampling distortion, N shall be adequate, larger than PFC_CR1[UTHR]. The average voltage (PFC_UAVG) is calculated by summing PFC_UAC samples over a single calculation cycle and normalizing by the total sample count (N):

PFC_CR0[UAVGCDIS] is set to “1” to start the calculation of PFC_UAVG by software. When PFC_CR0[UAVGSW] = 1, the calculation period is the time between the end of last calculation period and this sampling period (PFC_CR0[UAVGSW]). SysTick or other Timer module can be used to generate a frequency cycle for the accurate calculation of PFC_UAVG.

19.1.5 Current Error Compensation Module

Current error compensation module is inner loop of the PFC module. Its input is the difference between IAC1_REF/IAC2_REF (current reference calculated by outer loop) and PFC_IAC1/PFC_IAC2 (sampled current by ADC), which is transmitted to PI controller to generate control output IAC1_UK/IAC2_UK. Inner loop frequency = $48M / (PFC\_ARR * 2)$.

Figure 19-4 Calculation of IACx_REF

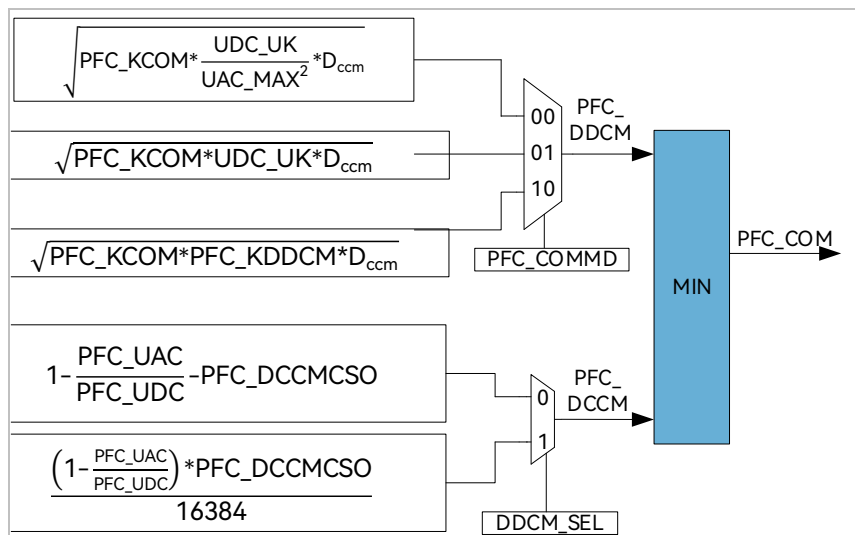


As shown above, IAC1_REF/IAC2_REF are generated by multiplying outer-loop output UDC_UK, input AC voltage PFC_UAC, the output voltage feed-forward compensation module and constant KM1/KM2. The eight low-order bits of PFC_KM register are KM1 and the eight high-order bits are KM2.

19.1.6 Current Feed-forward Compensation Module

Current feed-forward compensation module is mainly used to reduce the control of PI controller on the inner loop, facilitating parameter adjustment of the inner loop and improving the control performances.

Figure 19-5 Calculation of Current Feed-forward Compensation Module



As shown in Figure 19-5, PFC_CR0[COM_MD] decides current feed-forward compensation mode. When PFC_CR0[COM_MD] = 00, the hardware automatically calculates the current feed-forward compensation value PFC_COM but does not apply it to PFC1 or PFC2. When PFC_CR0[COM_MD] = 01, the hardware automatically calculates PFC_COM and applies it to both PFC1 and PFC2. When PFC_CR0[COM_MD] = 10, the hardware automatically calculates PFC_COM and applies it to PFC1, while the register PFC_DDCM is not updated automatically. In this case, PFC_DDCM can be written by software to compensate PFC2. When PFC_CR0[COM_MD] = 11, neither PFC_COM nor PFC_DDCM is updated automatically. In this case, PFC_COM can be written by software to compensate PFC1, and PFC_DDCM to compensate PFC2. When PFC_DDCM is updated automatically by hardware, if PFC_CR2[CMRD] = 0, PFC_DDCM loads the continuous-conduction-mode compensation value DCCM, and if PFC_CR2[CMRD] = 1, PFC_DDCM loads the discontinuous-conduction-mode compensation value DDCM. PFC_CR2[PFC_COMMD] is configured to select calculation mode of PFC_DDCM, which determines parameter configuration of PFC_KCOM and PFC_KDDCM. The hardware automatically calculates PFC_DDCM and compares it with PFC_DCCM, and

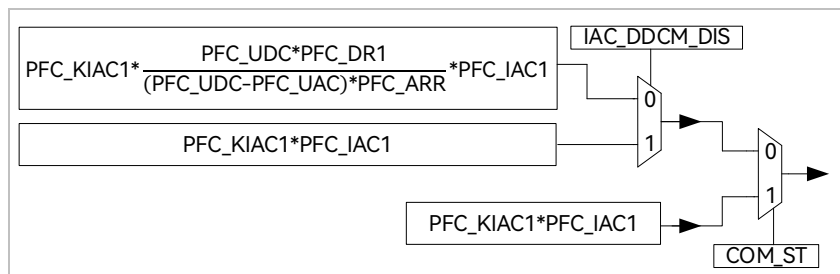
the smaller value is used as PFC_COM. The current feed-forward compensation calculation is performed once in each PFC carrier.

PFC_DCCM is adjusted by setting PFC_DCCMCSO, which is selected by PFC_CR2[DDCM_SEL]. When PFC_CR2[DDCM_SEL] is set as “0”, PFC_DCCMCSO is used as the offset of PFC_DCCM. For example, if PFC_DCCMCSO = 0x1000, PFC_DCCM reduces the calculation result by 0x1000. If PFC_CR2[DDCM_SEL] is set as “1”, PFC_DCCMCSO is used to determine the decrement/increment of PFC_DCCM. For example, if PFC_DCCMCSO = 0x4000, PFC_DCCM keeps unchanged; if PFC_DCCMCSO = 0x1FFF, PFC_DCCM is reduced to half of the calculation result, and if PFC_DCCMCSO = 0x7FFF, PFC_DCCM is increased to twice the calculation result.

19.1.7 Current Sampling Calibration Module

Current sampling calibration module is mainly used to calibrate the current when the motor winding operates in discontinuous current mode. Both the high-side and low-side current of the inner loop are to be calibrated. The following takes sampled current PFC_IAC1 of PFC1 module as an example. The same goes for PFC_IAC2.

Figure 19-6 Schematic Diagram of Current Sampling Calibration Module

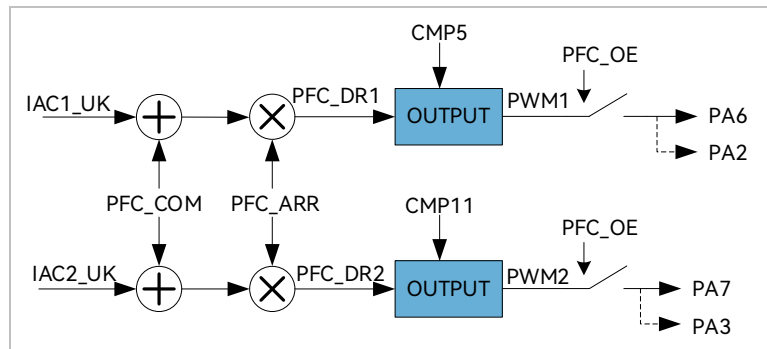


The current may fall to 0 in discontinuous current mode. If the sampled instantaneous current by ADC is used as the effective current, it may get too large. In this mode, the sampled current shall be calibrated and stored PFC_IACx register. Calibration mode is selected by PFC_CR2[IAC_DDCM_DIS]. When PFC_CR2[IAC_DDCM_DIS] = 0, the hardware automatically calculates the calibration coefficient, which is scaled linearly by setting PFC_KIACx. When PFC_KIACx is set as 0x4000 (default), the coefficient remains unchanged; when it is less than 0x4000, the coefficient is reduced accordingly; when it is larger than 0x4000, the coefficient is increased accordingly. When PFC_CR2[IAC_DDCM_DIS] = 1, the appropriate correction factor must be provided and written to PFC_KIACx. The status flag bit COM_ST signifies continuous current mode or discontinuous current mode of the motor winding. COM_ST is “0” in

PFC_DDCM mode, and “1” in PFC_DCCM mode.

19.1.8 PWM Output Module

Figure 19-7 Block Diagram of PWM Output Module



Because PFC outputs work in the same way, the following describes only PWM1 output. PWM1 duty cycle is obtained by adding IAC1_UK (inner-loop output of the PFC) and PFC_COM (current feed-forward compensation value) with the formula $(IAC1\_UK + PFC\_COM) / 32768 * 100\%$. As shown in Figure 19-7, PFC_DR1, $(IAC1\_UK + PFC\_COM) * PFC\_ARR / 32768$, is compared with PFC counter to generate PWM1 signal. When $PFC\_DR1 > PFC1\_CNTR$, PWM1 module outputs logical 1, and when $PFC\_DR1 < PFC1\_CNTR$, PWM1 module outputs logical 0. If PFC_CR0[PFCOE] is set to “1”, PA6 serves as PWM1 output. If PH_SEL1[PFCO1CT] is set to “1”, PWM1 output is switched from PA6 to PA2. If PH_SEL1[PFCO2CT] = 1, PWM2 output is switched from PA7 to PA3.



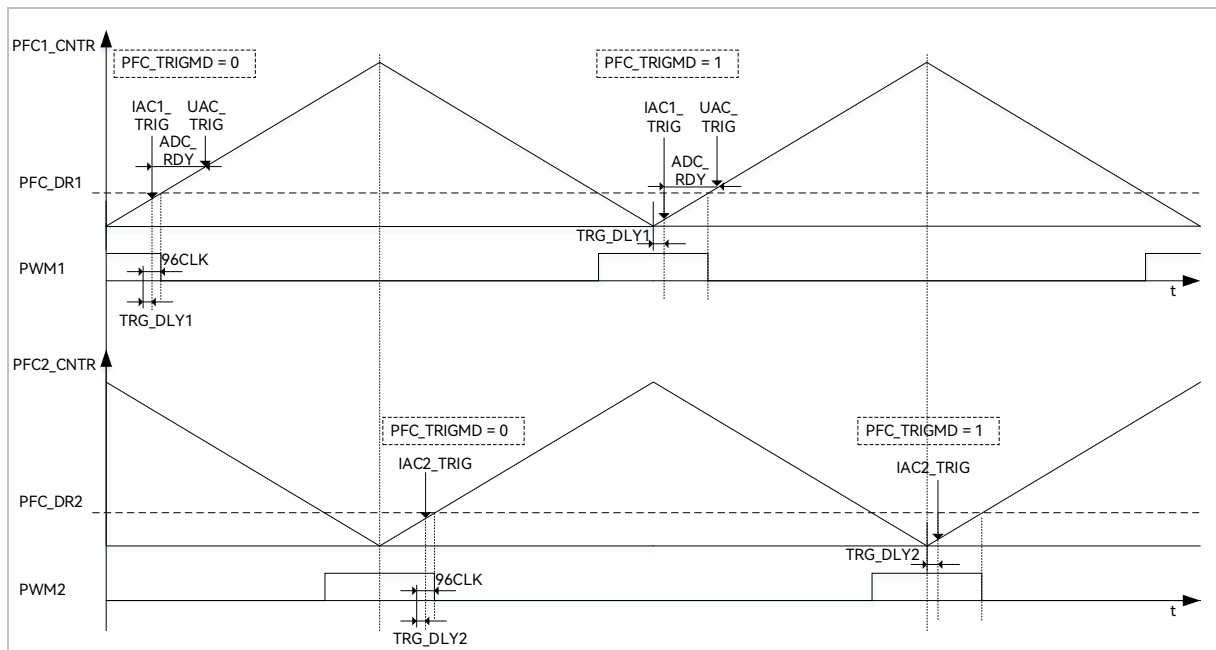
Note:

$$PFC2\_CNTR = PFC\_ARR - PFC1\_CNTR.$$

For test purposes, PFC_CR0[PFC_DR2MD] can be set as “1” to enable $PFC\_DR2 = PFC\_DR1$. When PFC_CR2[DRMIN_EN] = 1, the PWM module outputs the minimum duty cycle. When the output pulse width is less than the minimum width configured by PFC_CR2[DRMIN_THR], the final output is controlled by PFC_CR2[DRMIN_MD]. If PFC_CR2[DRMIN_MD] = 0, the final output is the minimum pulse width set by PFC_CR2[DRMIN_THR], while if PFC_CR2[DRMIN_MD] = 1, the final output becomes 0. The minimum pulse width corresponding to PFC_CR2[DRMIN_THR] is $n * 8 * 20ns$, with a maximum of approximately $31 * 8 * 20ns = 4.96\mu s$. The PFC carrier interrupt mode is selected via PFC_CR2[PFC_IE]. If PFC_CR2[PFC_IE] = 00, no interrupt request is generated. If PFC_CR2[PFC_IE] = 01, the interrupt request is generated when PFC1_CNTR reaches the underflow point. If PFC_CR2[PFC_IE] = 10, the interrupt request is generated when PFC1_CNTR reaches the overflow point. If PFC_CR2[PFC_IE] = 11, the interrupt request is generated

when PFC1_CNTR reaches the underflow or overflow point. When an interrupt request is generated, the interrupt flag PFC_CR2[PFC_IF] is set to “1” by hardware with the priority number at 10. The interrupt priority can be configured by three low-order bits of IP10 register.

Figure 19-8 PWM Output and PFC_IAC1/PFC_IAC2/PFC_UAC Sampling



19.1.9 Over-current Protection and Cycle-by-Cycle Current Limiting

PFC module supports over-current protection and cycle-by-cycle current limiting feature. Configuring CMP_CR1[CMP5EN] = 1 enables PFC1 over-current protection feature. Configuring CMP_CR1[CMP11EN] = 1 enables PFC2 over-current protection feature. When CMP_CR0[PFCOA] = 1, cycle-by-cycle current limiting feature is enabled. CMP_CR0[PFC_FM] determines protection activities when the system receives an over-current signal. If CMP_CR0[PFC_FM] is set as “0” and an over-current signal of CMP5 is detected, PFC module only protects the PFC circuit where CMP5 is mounted. Similarly, when an over-current signal of CMP11 is detected, PFC module only protects the PFC circuit where CMP11 is mounted. If CMP_CR0[PFC_FM] is set as “1”, either an over-current signal of CMP5 or CMP11 is detected, PFC module protects both the PFC circuits where CMP5 and CMP11 are mounted. After “1” is written to CMP5, an over-current protection signal is generated and PWM module outputs low level. When this hardware OCP occurs, the system only pulls the output low and does not clear PFC_CR0[PFCEN], PFC_CR0[IAC2EN] and PFC_CR0[PFCOE]. Under this condition, PFC_CR0[PFC_FORC1] and PFC_CR0[PFC_FORC2] can be read to determine if such forced pull-down has occurred. The over-current protection state is released when

PFC_CR0[PFCOE] = 0.

19.2 PFC_UAC/PFC_IAC1/PFC_IAC2/PFC_UDC Sampling

19.2.1 PFC_UDC Sampling

- PFC_UDC is sampled by FOC module in every FOC carrier cycle.
- ADC1 channel 2 is used by default.

19.2.2 PFC_IAC1/PFC_IAC2 Sampling

- Sample once during PWM ON in every inner loop cycle.
- The sampling point is determined according to PFC_CR2[PFC_TRIGMD] and PFC_TRGDLY (as shown in Figure 19-8). If PFC_CR2[PFC_TRIGMD] = 0, sampling is triggered 96CLK ahead of the falling edge of PWM. If PFC_CR2[PFC_TRIGMD] = 1, sampling is triggered at the center point during PWM ON. The time delay for PFC_IAC1 sampling is configured by eight low-order bits of PFC_TRGDLY register and that for PFC_IAC2 sampling by eight high-order bits. In center-point sampling mode, a write of “1” to bit7 and bit15 advances the sampling time. For example, if PFC_CR2[PFC_TRIGMD] = 1 and PFC_TRGDLY = 0x0102, PFC_IAC1 sampling is delayed by one CLK from the central point during PWM1 ON, and PFC_IAC2 sampling is delayed by two CLKs from the central point during PWM2 ON. If PFC_CR2[PFC_TRIGMD] = 1 and PFC_TRGDLY = 0x8182, PFC_IAC1 sampling is advanced by one CLK from the central point during PWM1 ON, and PFC_IAC2 sampling is advanced by two CLKs from the central point during PWM2 ON.
- ADC3 channel 0 is used for PFC_IAC1 sampling by default, and ADC3 channel 2 for PFC_IAC2 sampling.
- PFC_IAC1 offset is set by IAC1_CSO register and PFC_IAC2 offset by IAC2_CSO. Providing that the voltage range of ADC is 0V ~ 5V and the reference value is 2.5V, then $IAC1\_CSO = 2.5/5V \times 32768 = 16384$ (CSR: 0x4000). IAC2_CSO is calculated in the same way.

19.2.3 PFC_UAC Sampling

- PFC_UAC sampling cycle is set by PFC_CR1[UACSAMSEL] (once every 1/2/4/8 inner-loop cycles). When PFC1 is enabled only, PFC_UAC is sampled after sampling of PFC_IAC1. When both PFC1 and PFC2 are enabled, PFC_UAC is sampled after sampling of PFC_IAC2.
- ADC3 channel 1 is used by default.

- PFC_UAC reference offset is set by UAC_CSO. Providing that the voltage range of ADC is 0V ~ 5V and the reference value is 2.5V, then $UAC\_CSO = 32768 \times 2.5 / 5V = 16384$ (CSR: 0x4000)

Figure 19-9 PFC_UAC Single-bridge Sampling

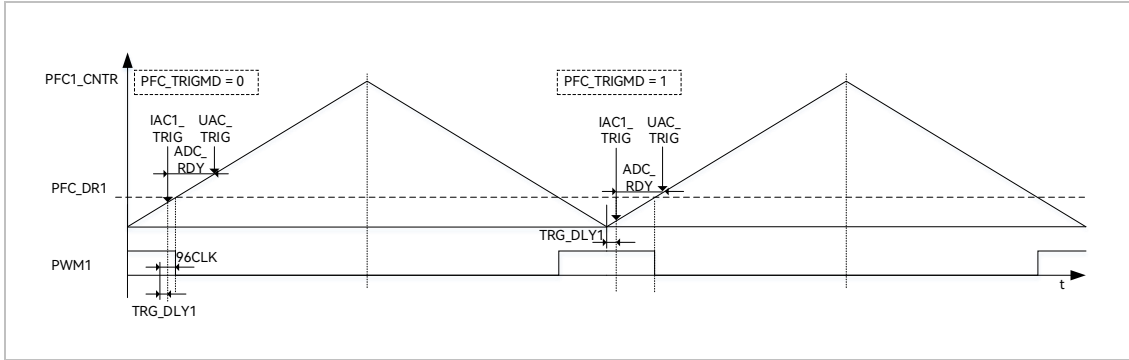
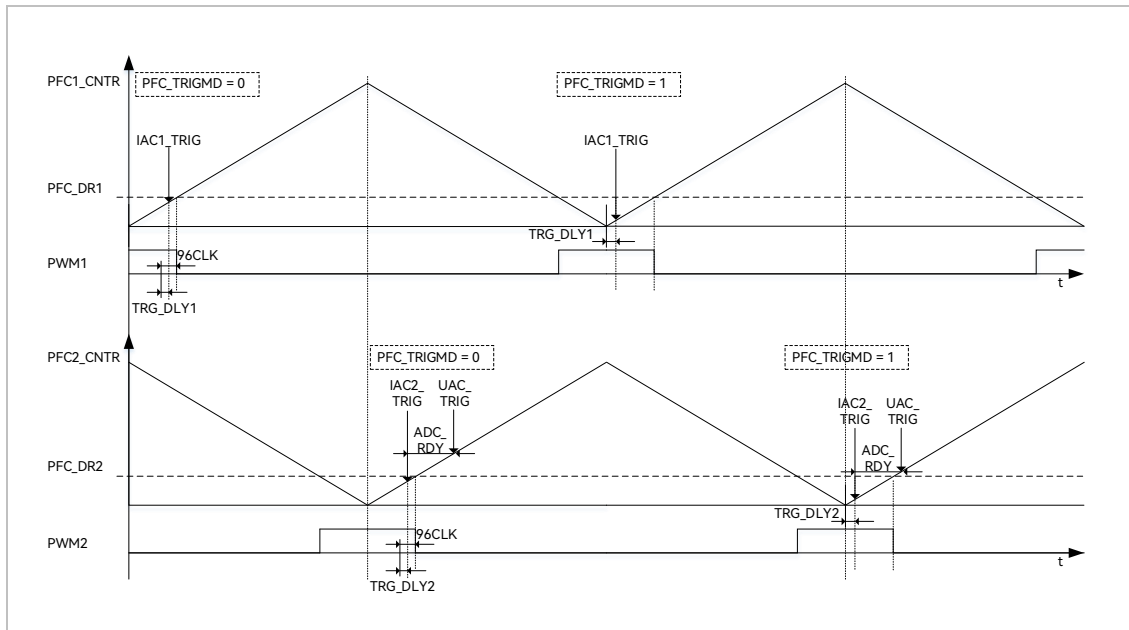


Figure 19-10 PFC_UAC Dual-bridge Sampling



19.3 PFC Registers

19.3.1 PFC_CR0 (CSR: 0x5C0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																COM_ST	UAVGSW	PFC_FORC2	PFC_FORC1	RSV		PFC_DR2MD	PFC_UDCSEL	COM_MD		PFC_FM	UAVGDIS	PFCOA	IAC2EN	PFCOE	PFCEN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	rw	rw	rw	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	-	-	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	COM_ST	Feed-forward Compensation Status Flag 0: DDCM 1: DCCM
[14]	UAVGSW	PFC_UAVG Calculation by Software After PFC_UAVG calculation starts, PFC_UAVG value is updated. This bit is set to “1” by software, and automatically cleared to “0” by hardware. A write of “0” has no effect. 0: Disable 1: Enable
[13]	PFC_FORC2	PFC2 Output Forced Pull-down 0: Disable 1: Enable
[12]	PFC_FORC1	PFC1 Output Forced Pull-down 0: Disable 1: Enable
[11:10]	RSV	Reserved
[9]	PFC_DR2MD	PFC2 Hardware Conformance Test Mode Enable 0: Disable. PFC2 module operates according to its configurations 1: Enable. PFC2 module is forced to mirror PFC1’s output for hardware conformance testing
[8]	PFC_UDCSEL	Bus Voltage Source for PFC Calculation 0: NFOCx_UDCFLT 1: NOFCx_UDC

[7:6]	COM_MD	Feedforward Compensation Mode Selection 00: Both PFC_DDCM and PFC_COM are updated by hardware, but PFC_COM is not applied to PFC1 and PFC2. 01: Both PFC_DDCM and PFC_COM are updated by hardware, and PFC_COM is applied to PFC1 and PFC2. 10: PFC_COM is updated by hardware, and is applied to PFC1. PFC_DDCM cannot be updated by hardware and must be written by software to compensate PFC2. 11: PFC_COM cannot be updated by hardware and must be written by software to compensate PFC1. PFC_DDCM cannot be updated by hardware and must be written by software to compensate PFC2.
[5]	PFC_FM	OCP Activities Selection 0: PFC module only protects the PFC circuit where an over-current signal (triggered by CMP5 or CMP11) is detected. 1: Either an over-current signal of CMP5 or CMP11 is detected, PFC module protects both the PFC circuits where CMP5 and CMP11 are mounted.
[4]	UAVGCDIS	PFC_UAVG Calculation by Hardware Enable When this bit is disabled, the hardware does not calculate PFC_UAVG at each power frequency period. In this case, PFC_CR0[UAVGSW] can be configured in software to start PFC_UAVG calculation. PFC_UAVG calculation also starts automatically when internal counter overflows. 0: Enable 1: Disable
[3]	PFCOA	Cycle-by-cycle Current Limiting Feature Enable After CMP5 or CMP11 is enabled, over-current protection feature is enabled by default. When an over-current event occurs, PFC module turns off the output in the current circuit, and decides whether to turn off the output in the other based on PFC_FM configuration. After PFCOA is enabled, the hardware automatically restores the output after the over-current protection state is released, that is, cycle-by-cycle current limiting feature. 0: Disable 1: Enable
[2]	IAC2EN	PFC2 Enable 0: Disable 1: Enable
[1]	PFCOE	PFC Output Enable After this bit is enabled, PWM signal generated by PFC1 module outputs to PA6, and that generated by PFC2 module to PA7. 0: Disable

		1: Enable
		 Note: If it is necessary to clear this bit to “0”, PA5 and PA6 must first be configured as digital output mode and set to output “0”.
[0]	PFCEN	PFC1 Enable 0: Disable 1: Enable

19.3.2 PFC_CR1 (CSR: 0x5C1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								UACSMSEL		UTHR	UCTHR				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:6]	UACSMSEL	PFC_UAC Sampling Cycle PFC_UAC sampling is performed once every x PFC cycle(s). 00: 1 PFC cycle 01: 2 PFC cycles 10: 4 PFC cycles 11: 8 PFC cycles
[5]	UTHR	PFC_UAC Cycle Start Point PFC_UAC uses this value to determine the start and end points of one mains cycle, primarily for calculating PFC_UAVG. This setting is related to UAC_BASE, i.e., the hardware voltage divider ratio for PFC_UAC. 0: $1/16 \cdot \text{UAC\_BASE}$ 1: $1/8 \cdot \text{UAC\_BASE}$
[4:0]	UCTHR	Minimum Number of PFC_UAC Sampling Once the hardware obtains the mains cycle via PFC_CR1[UTHR], the number of PFC_UAC samples taken within that period must exceed the count set by PFC_CR1[UCTHR]. Minimum sampling times: $\text{PFC\_CR1[UCTHR]} \cdot 32$

19.3.3 PFC_CR2 (CSR: 0x5C2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_IF	CMRD	IAC_DDCM_DIS	DDCM_SEL	PFC_IE		DRMIN_MD	DRMIN_EN	PFC_COMMD	PFC_TRIGMD	DRMIN_THR					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	PFC_IF	PFC Carrier Underflow Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[14]	CMRD	Value Read from PFC_DDCM Register 0: DCCM 1: DDCM
[13]	IAC_DDCM_DIS	PFC_KIACx Calibration Mode Selection 0: It is automatically calculated by hardware with the formula $(PFC\_UDC * PFC\_DR) / ((PFC\_UDC - PFC\_UAC) * PFC\_ARR)$ 1: It requires manual calculation with the formula $(PFC\_UDC * PFC\_DR) / ((PFC\_UDC - PFC\_UAC) * PFC\_ARR)$
[12]	DDCM_SEL	Control Mode of PFC_DCCMCSO 0: PFC_DCCMCSO is used as the offset of PFC_DCCM. If PFC_DCCMCSO is positive, PFC_DCCM reduces the calculation result by PFC_DCCMCSO. 1: PFC_DCCMCSO is used to determine the decrement/increment of PFC_DCCM. Q15 format.
[11:10]	PFC_IE	PFC Carrier Interrupt Enable 00: Disable 01: The interrupt generated at PFC underflow point. 10: The interrupt is generated at PFC overflow point. 11: The interrupt is generated at PFC overflow or underflow point.

[9]	DRMIN_MD	Minimum Duty Cycle Mode Selection 0: The minimum value is output when the output duty cycle falls below the set minimum value. 1: “0” is output when the output duty cycle falls below the set minimum value.
[8]	DRMIN_EN	Minimum Duty Cycle Output Enable 0: Disable. When the output duty cycle falls below the set minimum value, secondary filtering is applied to the sampled current. 1: Enable. When the output duty cycle falls below the set minimum value, the output pulse width is determined according to DRMIN_MD.
[7:6]	PFC_COMMD	Feed-forward Compensation Selection 00: UDC_UK/(PFC_UAVG*PFC_UAVG) is calculated. 01: UDC_UK is calculated. 1x: KDDCM is written in software.
[5]	PFC_TRIGMD	Sampling Point Selection for PFC_IAC1 and PFC_IAC2 0: At the end of high level 1: In the middle of high level
[4:0]	DRMIN_THR	Minimum Duty Cycle Output Minimum pulse width for 2-channel PWM outputs Calculation formula: $n*8*CLK$, where n is at most 31, about 4.96μs  Note: The minimum duty cycle shall be set to “0” at initialization, then gradually ramped to the target value. Otherwise, excessive current may occur in the first two cycles.

19.3.4 PFC_KM (CSR: 0x5C3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_KM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_KM	KM1/KM2 Coefficient of PFC Outputs The eight low-order bits of PFC_KM register correspond to KM1 and the eight high-order bits to KM2. Range [0,255]

**Note:**

When $KM_x = 0$, the corresponding $IACx\_REF$ register is no longer automatically updated, and shall be manually written.

19.3.5 UAC_CSO (CSR: 0x5C4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UAC_CSO															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UAC_CSO	PFC_UAC Sampling Reference Offset A data can be written to UAC_CSO register to set PFC_UAC reference offset. Range [0,32767]  Note: Providing that ADC voltage range is 0V ~ 5V, the reference value is 2.5V, then $UAC\_CSO = 32768 \times 2.5V/5V = 16384$ (CSR: 0x4000).

19.3.6 IACx_CSO (CSR: 0x5C5/CSR: 0x5C6) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_CSO															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_CSO	PFC_IACx Sampling Reference Offset A data can be written to IACx_CSO register to set PFC_IACx reference offset.

		Range [0,32767]  Note: Providing that ADC voltage range is 0V ~ 5V, the reference value is 2.5V, then $UAC\_CSO = 32768 \times 2.5V/5V = 16384$ (CSR: 0x4000).

19.3.7 PFC_ARR (CSR: 0x5C7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				PFC_ARR											
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:12]	RSV	Reserved
[11:0]	PFC_ARR	Reload Value of PFC Counter. It configures the carrier period and operation mode (center-alignment mode). An overflow event occurs when PFC counter counts from 0 and reaches PFC_ARR, and then it counts down to 0. This register is write-only. Range [0,4095]

19.3.8 PFC_DRx (CSR: 0x5C8/CSR: 0x5C9) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RSV																				PFC_DRx																
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w	w	w	w	w					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0					

Bit	Name	Description
[31:12]	RSV	Reserved
[11:0]	PFC_DRx	Comparison Value by PFC to Generate PWMx Signal Logic 1 is output when PFC counter is less than PFC_DRx, otherwise, logical 0 is output. When the PFC module is enabled, PFC_DRx is automatically updated by hardware.

Range [0,4095]

19.3.9 UDC_ARR (CSR: 0x5CA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RSV																				UDC_ARR																
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0					

Bit	Name	Description
[31:12]	RSV	Reserved
[11:0]	UDC_ARR	Outer-loop Frequency of PFC Module This bit is used to set outer-loop frequency of PFC module, or PI controller frequency of UDC. Formula: Outer-loop frequency = Inner-loop frequency / UDC_ARR = 48M / (2*PFC_ARR) / UDC_ARR For example, if the clock runs at 48MHz(20.83ns), PFC_ARR = 150 and UDC_ARR = 200, then inner-loop frequency = 48MHz / (2*PFC_ARR) = 160KHz and outer-loop frequency = 160KHz / UDC_ARR = 800Hz. Range [0,2047]

19.3.10 PFC_TRGDLY (CSR: 0x5CB)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_TRGDLY															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_TRGDLY	ADC Sampling Delay of PFC_IAC1 and PFC_IAC2

		The eight low-order bits defines the time delay TRG_DLY1 for PFC_IAC1 sampling, and the eight low-order bits defines TRG_DLY2 for PFC_IAC2 sampling. If PFC_TRIGMD is 0, it ranges between 0 and 255, and if PFC_TRIGMD is 1, it ranges between -128 and 127. A negative value signifies that the sampling is performed ahead of time. For example, if the clock runs at 48MHz(20.83ns) and PFC_TRGDLY = 5, the sampling is delayed by $20.83 \times 8 \times 5 = 833.2\text{ns}$.

19.3.11 UDC_REF (CSR: 0x5CC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_REF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_REF	User-defined UDC Reference

19.3.12 UDC_UK (CSR: 0x5CD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_UK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_UK	Output Value UK of PI controller for UDC Range [-32768,32767]

19.3.13 UDC_KP (CSR: 0x5CE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_KP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_KP	KP Coefficient of PI Controller for UDC Range [0,32767]; MSB is always 0; Q10 format.

19.3.14 UDC_KI (CSR: 0x5CF)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_KI															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_KI	KI Coefficient of PI Controller for UDC Range [0,32767]; MSB is always 0; Q15 format.

19.3.15 UDC_UKMAX (CSR: 0x5D0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_UKMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_UKMAX	Maximum Output of PI Controller for UDC Range [-32768,32767]

19.3.16 UDC_UKMIN (CSR: 0x5D1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																UDC_UKMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	UDC_UKMIN	Minimum Output of PI Controller for UDC Range [-32768,32767]

19.3.17 IACx_REF (CSR: 0x5D2/CSR: 0x5D8) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_REF															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_REF	User-defined PFC_IACx Reference Range [-32768,32767]

19.3.18 IACx_UK (CSR: 0x5D3/CSR: 0x5D9) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_UK															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_UK	Output Value UK of PI Controller for PFC_IACx Range [-32768,32767]

19.3.19 IACx_KP (CSR: 0x5D4/CSR: 0x5DA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_KP															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_KP	KP Coefficient of PI Controller for PFC_IACx Range [0,32767]; MSB is always 0; Q10 format

19.3.20 IACx_KI (CSR: 0x5D5/CSR: 0x5DB) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_KI															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_KI	KI Coefficient of PI Controller for PFC_IACx Range [0,32767]; MSB is always 0; Q15 format

19.3.21 IACx_UKMAX (CSR: 0x5D6/CSR: 0x5DC) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_UKMAX															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_UKMAX	Maximum Output of PI Controller for PFC_IACx Range [-32768,32767]

19.3.22 IACx_UKMIN (CSR: 0x5D7/CSR: 0x5DD) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IACx_UKMIN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IACx_UKMIN	Minimum Output of PI Controller for PFC_IACx Range [-32768,32767]

19.3.23 PFC_UAC (CSR: 0x5DE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_UAC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_UAC	Sampling Threshold Triggered by ADC Voltage

19.3.24 PFC_IACx (CSR: 0x5DF/CSR: 0x5E0) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_IACx															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_IACx	Sampling Threshold Triggered by ADC Current

19.3.25 PFC_UDC (CSR: 0x5E1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_UDC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_UDC	ADC Sampling Triggered by Output Voltage

19.3.26 PFC_UAVG (CSR: 0x5E2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_UAVG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_UAVG	Average PFC_UAC in One Frequency Cycle Range [-32768,32767]  Note: When the input power source is DC, PFC_CR0[UAVGSW] must be manually written to trigger a single PFC_UAVG sampling. Otherwise, PFC_UAVG cannot be timely calculated by hardware via PFC_CR1[UTHR], causing PFC_UAVG to change abruptly from 0.

19.3.27 PFC_COM (CSR: 0x5E3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_COM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_COM	Inner-loop Feed-forward Compensation Value Range [-32768,32767]

19.3.28 PFC_KCOM (CSR: 0x5E4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_KCOM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_KCOM	Inner-loop Feed-forward Compensation Coefficient for PFC_DDCM Range [0,32767]

19.3.29 PFC_DDCM (CSR: 0x5E5)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_DDCM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊	⌊
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_DDCM	Inner-loop Feed-forward Compensation Value in DDCM Mode It works with PFC_CR2[CMRD] Range [0,32767]

19.3.30 PFC_KDDCM (CSR: 0x5E7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_KDDCM															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡	≡
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_KDCCM	Compensation Coefficient in DDCM Mode When PFC_COMMD is set to "1x", PFC_KDDCM is written to update UDC_UK. Range [0,32767]

19.3.31 PFC_DCCMCSO (CSR: 0x5E8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_DCCMCSO															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_DCCMCSO	Adjustment Coefficient of the Compensation Value in DCCM Mode When DDCM_SEL is set as "0", PFC_DCCMCSO is used as the offset of PFC_DCCM. If PFC_DCCMCSO is positive, PFC_DCCM reduces the calculation result by PFC_DCCMCSO. When DDCM_SEL is set as "1", PFC_DCCMCSO is used to determine the decrement/increment of PFC_DCCM. If PFC_DCCMCSO is 0x4000, PFC_DCCM keeps unchanged. If PFC_DCCMCSO is larger than 0x4000, PFC_DCCM is increased accordingly. If PFC_DCCMCSO is lower than 0x4000, PFC_DCCM is reduced accordingly. Range [-32768,32767]

19.3.32 PFC_KIACx (CSR: 0x5E9/CSR: 0x5EA) (x = 1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PFC_KIACx															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PFC_KIACx	Calibration Coefficient of IACx Sampling for Feed-forward Compensation in DDCM Mode When IAC_DDCM_DIS is set to “0”, the sampled current is $PFC\_KIACx \cdot PFC\_UDC \cdot PFC\_DRx \cdot PFC\_IACx / ((PFC\_UDC - PFC\_UAC) \cdot PFC\_ARR)$. When IAC_DDCM_DIS is set to “1”, the sampled current is $PFC\_KIACx \cdot PFC\_IACx$ Range [0,32767]

20 Systick

20.1 Systick Instructions

The chip can generate Systick interrupts at a fixed interval, and the interrupt cycle is controlled by SYST_ARR. Systick interrupt is enabled when SYST_SR[SYSTIE] is set to “1”, and the interrupts are accessed by 15.

20.2 Systick Registers

20.2.1 SYST_ARR (CSR: 0x440)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																						SYST_ARR									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0	1	1	1	0	1	1	0

Bit	Name	Description
[31:9]	RSV	Reserved
[8:0]	SYST_ARR	Systick Reloaded Value This bit determines the cycle at which Systick interrupts are generated, which defaults to 1ms. Calculation formula is as follows: Systick interrupt rate = SYSCLK/128 * (SYST_ARR[8:0]) Range [1, 511]

20.2.2 SYST_SR (CSR: 0x441)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												SYSTIF	SYSTIE		
																												rw0	rw		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Description
[31:2]	RSV	Reserved
[1]	SYSTIF	Systick Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[0]	SYSTIE	Systick Interrupt Enable 0: Disable 1: Enable

21 System Clock

21.1 Introduction

The clock consists of three modules: internal fast clock, PLL Clock and internal slow clock. The system clock operates either as an internal fast clock or a PLL Clock. The PLL clock source can be an internal fast clock or an external fast clock, which is selected by the associated register or switched by software program. PLL clock can be configured as external clock input or external crystal oscillator input, and internal slow clock is used as WDT for configuring overflow time of the watchdog. External slow clock is used for RTC counts.

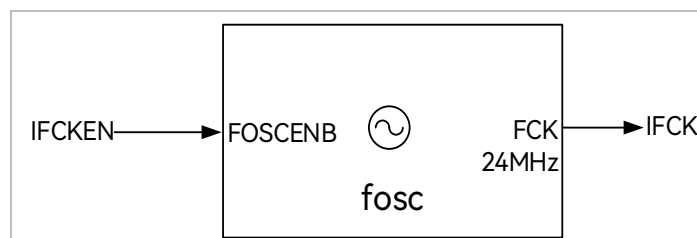
Table 21-1 Operation Modes of System Clock

Operation Mode	PLLSRC	FCKMOD	ECMOD	PLLFSEL
Internal Fast Clock (24M)	0	0	0(X)	0(X)
PLL 24M (Internal Fast Clock)	0	1	0(X)	1
PLL 48M (Internal Fast Clock)	0	1	0(X)	0
PLL 24M (External Fast Clock - Crystal)	1	1	0	1
PLL 48M (External Fast Clock - Crystal)	1	1	0	0
PLL 24M (External Fast Clock - Active Clock)	1	1	1	1
PLL 48M (External Fast Clock - Active Clock)	1	1	1	0

21.2 Clock Operations

21.2.1 Internal Fast Clock

Figure 21-1 Input/Output of Internal Fast Clock

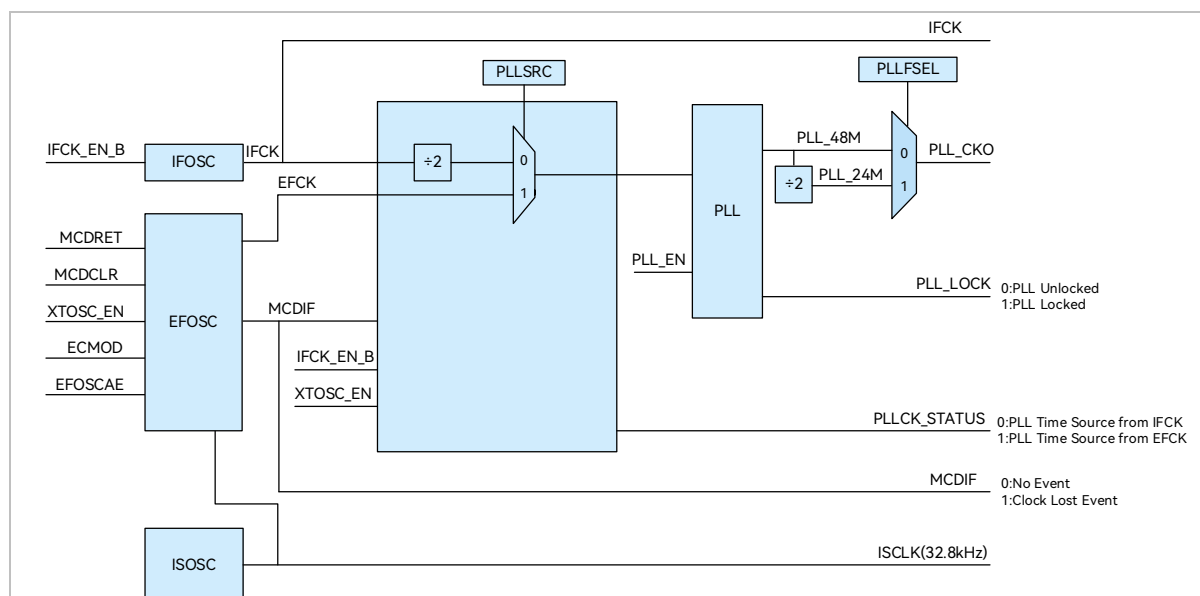


The I/O pins of the internal fast clock are shown in Figure 21-1. Internal fast clock is used to produce an accurate clock running at a rate of 24MHz. It is enabled after Internal CLK option in System Clk Setting (as shown in Figure 21-5) is checked. In sleep mode (PCON[STOP] = 1), this clock is disabled.

21.2.2 PLL Clock

PLL clock can be sourced from an internal fast clock or an external fast clock. The external fast clock supports crystal input mode and external clock input mode, as shown below.

Figure 21-2 Block Diagram of PLL Clock



21.2.2.1 PLL Clock Sourced from An Internal Fast Clock

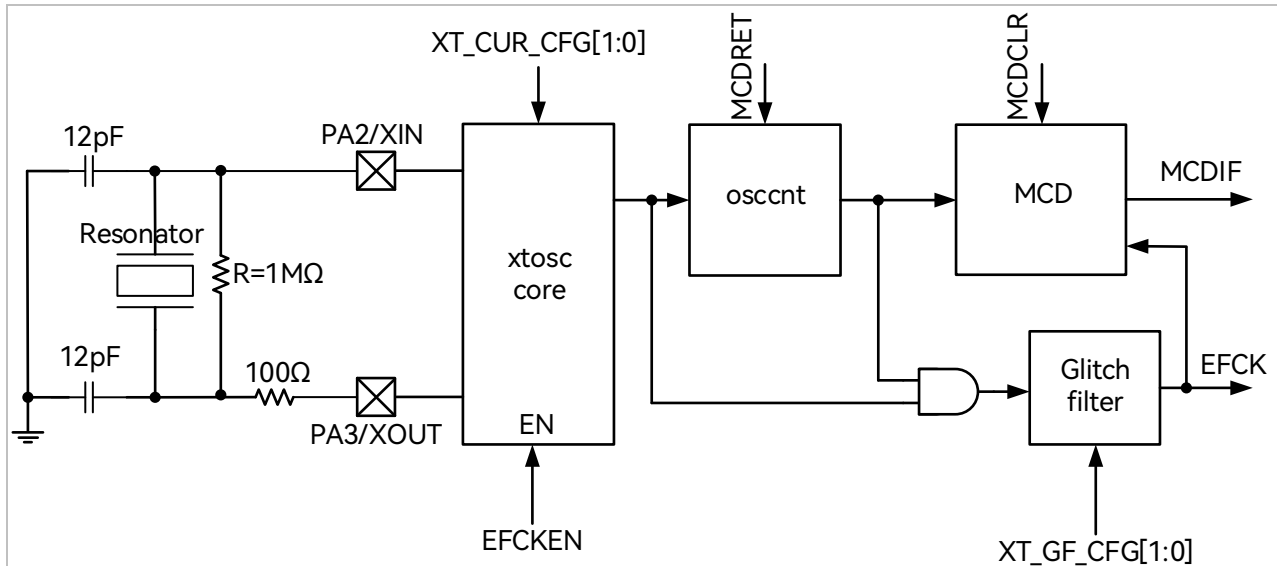
As shown in Figure 21-5, PLL clock is enabled after PLL option in System Clk Setting is checked or OSC_CR[PLLEN] is set as “1” by software. PLL clock rate, 48M or 24M, is selected in PLL Setting.

21.2.2.2 PLL Clock Sourced from An External Fast Clock

As shown in Figure 21-5, PLL clock is enabled after PLL option in System Clk Setting is checked or OSC_CR[PLLEN] is set as “1” by software. PLL clock rate, 48M or 24M, is selected in PLL Setting. When Enable EC Mode is selected, external fast clock serves as the input source of PLL clock. If Crystal Mode (in External Clk Mode) is selected, this external fast clock works in crystal input mode, and if Oscillator Mode (in External Clk Mode) is selected, it works in external clock input mode.

21.2.2.2.1 Crystal Input Mode

Figure 21-3 Crystal Input Mode of External Fast Clock xtosc

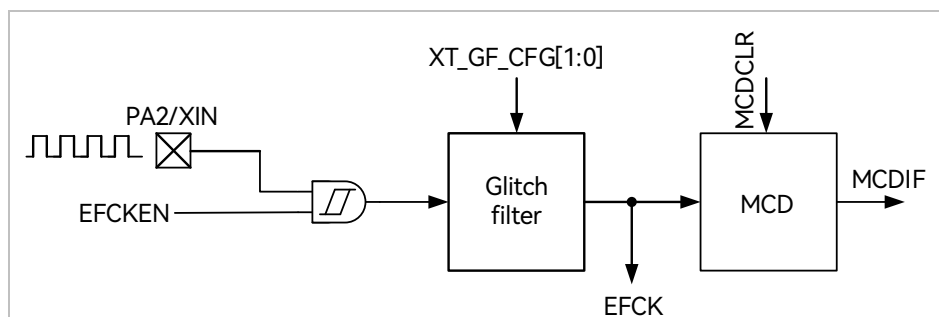


Crystal input mode of the external fast clock is shown in Figure 21-3. External fast clock is used to produce an accurate clock running at a rate of 24MHz.

As shown in Figure 21-5, PLL clock is enabled after PLL option in System Clk Setting is checked or OSC_CR[PLLEN] is set as “1” by software. PLL clock rate, 48M or 24M, is selected in PLL Setting. When Enable EC Mode is selected, external fast clock serves as the input source of PLL clock. If Crystal Mode (in External Clk Mode) is selected, this external fast clock works in crystal input mode. As shown Figure 21-3, the external crystal oscillator is switched on and the clock xtosc works in the crystal input mode.

21.2.2.2.2 External Clock Input Mode

Figure 21-4 External Clock Input Mode of External Fast Clock



External clock input mode of the external fast clock is shown in Figure 21-4. External clock is input through XIN pin. PLL clock is enabled after PLL option in System Clk Setting is checked or OSC_CR[PLLEN] is set as “1” by software. PLL clock rate, 48M or 24M, is selected in PLL Setting. If Oscillator Mode (in External

Clk Mode) is selected, external clock serves as the input source, that is, the clock xtosc works in the external clock input mode.

MCDRET is the signal to clear OST counter (active High). When the transistor circuit runs in crystal input mode, OST counter counts 1024 clocks and EFCK outputs clock after it stabilizes. OST counter does not work in external clock input mode.

OST counter is automatically cleared to “0” by hardware when transistor circuit is not enabled. When the clock is missing, the system automatically switches the clock to the internal clock, and then the software switches the clock to the external clock again. At this time, it sends a high level to MCDRET to clear OST counter.

Figure 21-5 System Clock Configurations

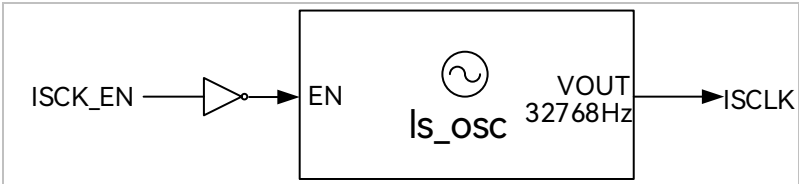
The screenshot shows the 'System Clock Configurations' dialog box with the following settings:

- Cache Option:** ☐ Cache Data, ☐ Cache XData, ☐ Cache Code
- Clk Setting:**
 - System Clk Setting:** ☒ Internal Fck, ☐ PLL
 - PLL Setting:** ☒ 48MHz, ☐ 24MHz
 - External Clk Mode:** ☐ Crystal Mode, ☒ Oscillator Mode
- General Setting:**
 - ☐ ECC Disable
 - ☐ Enable watch-dog
 - ☐ Enable Eos Reset
 - ☒ Enable EC Mode
- LVW Setting:** ☒ Disable LVW, ☐ Enable LVW Interrupt, ☒ 4.2V, ☐ 4.5V
- LVR Setting:** ☐ 3.0V, ☐ 3.5V, ☐ 3.8V
- Eos Setting:** ☒ Level0, ☐ Level1, ☐ Level2, ☐ Level3
- Encrypt Config:**
 - ☐ Enable memory encrypt
 - ☐ Full Encrypt, ☒ Partial Encrypt
 - Start Sector: 0
 - End Sector: 128
- Step into, program stop at:** main function (dropdown), ☐ Non fixed code region
- Memory cache mode:** No Cache (dropdown)

Buttons: Ok, Cancel, Reset

21.2.2.3 Internal Slow Clock

Figure 21-6 Input/Output of Internal Slow Clock ISOSC



The I/O pins of the internal slow clock are shown in Figure 21-6. Internal slow clock is used to produce clock signals at a rate of 32768Hz. In sleep mode (PCON[STOP] = 1), this clock is disabled.

21.2.3 Clock Registers

21.2.3.1 CCFG2 (CSR: 0xFFD)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								LVWPD	LVWIE	IWDTEN	RSV			PLLSRC	FCKMOD
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	-	-	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	-	-	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	LVWPD	Low Voltage Warning Enable 0: Disable 1: Enable
[6]	LVWIE	Low Voltage Warning Interrupt Enable 0: Disable 1: Enable
[5]	IWDTEN	IWDT (Independent Watchdog Timer) Enable 0: Disable 1: Enable
[4:2]	RSV	Reserved
[1]	PLLSRC	Source of PLL Clock 0: PLL clock is sourced from the internal fast clock. 1: PLL clock is sourced from the external fast clock in 12MHz crystal input mode or 12MHz external clock input mode.

[0]	FCKMOD	System Clock Frequency Selection 0: Internal oscillator clock: 24MHz 1: PLL clock works and the clock rate is determined by FCKMOD and CCFG3[PLLFSEL].

21.2.3.2 CCFG3 (CSR: 0xFFC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOSSET				RSV			LVRSEL		RSV							EOS_RST_EN	RSV						LWSEL	RSV		XT_CUR_CFG		XT_GF_CFG		ECMOD	PLLFSEL
RW	RW	RW	RW	-	-	-	RW	RW	-	-	-	-	-	-	-	RW	-	-	-	-	-	-	RW	-	-	RW	RW	RW	RW	RW	RW
0	0	0	0	-	-	-	0	0	-	-	-	-	-	-	-	0	-	-	-	-	-	-	0	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:28]	EOSSET	Electrical Overstress (EOS) Level with 0000 by Default The lower the level, the lower the EOS sensitivity. 00: Level 0, where EOS sensitivity is the lowest. 01: Level 1 10: Level 2 11: Level 3, where EOS sensitivity is the highest.
[27:25]	RSV	Reserved
[24:23]	LVRSEL	Low Voltage Reset Threshold Voltage VDD5 is detected for the low voltage reset. 00: 3.0V 01: No effect 10: 3.5V 11: 3.8V
[22:16]	RSV	Reserved
[15]	EOS_RST_EN	EOS Reset Enable 0: Disable 1: Enable
[14:9]	RSV	Reserved
[8]	LWSEL	VDD5 Voltage for Low Voltage Warning 0: 4.2V 1: 4.5V
[7:6]	RSV	Reserved

[5:4]	XT_CUR_CFG	Drive Capability for Crystal Circuit 10: Weak, which is suitable for 0MHz ~ 12MHz crystals (0.32mA) 11: Medium, which is suitable for 4MHz ~ 24MHz crystals (0.64mA) 00: Strong, which is suitable for 16MHz ~ 24MHz crystals (1.28mA) 01: Very strong, which is suitable for crystals ≥24MHz (2.56mA)
[3:2]	XT_GF_CFG	Clock Glitch Filter Selection 00: Clock glitch filter 0 01: Clock glitch filter 1
[1]	ECMOD	External Fast Clock Input Mode 0: Crystal Input Mode 1: External Clock Input Mode
[0]	PLLFSEL	PLL Clock Rate Selection. In crystal input mode, 12MHz external crystal oscillator shall be used. 0: 48MHz 1: 24MHz

21.2.3.3 OSC_CR (CSR: 0x463)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								MCDRET	PLLLIE	MCDIE	EFOSCAE	RSV		PLLEN	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w1	rw	rw	rw	-	-	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	-	-	0

Bit	Name	Description
[31:7]	RSV	Reserved
[6]	MCDRET	OST Counter Clear Signal 0: No effect 1: OST counter is cleared
[5]	PLLLIE	PLL Loss Interrupt Enable 0: Disable 1: Enable
[4]	MCDIE	External Fast Clock Missing Interrupt Enable 0: Disable 1: Enable
[3]	EFOSCAE	PA2 and PA3 Mode Selection 0: PA2 and PA3 work in GPIO mode.

		1: If CCFG3[ECMOD] = 0, both PA2 and PA3 work as analog inputs for crystal oscillator circuit. If CCFG3[ECMOD] = 1, PA2 works as an analog input for external clock, and PA3 works in GPIO mode.
[2:1]	RSV	Reserved
[0]	PLLEN	PLL Enabled 0: Disable 1: Enable

21.2.3.4 OSC_SR (CSR: 0x464)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												PLL_LOCK	PLLCK_STATUS	PLLLIF	MCDIF
																												r	r	rw0	rw0
																												r	r	rw0	rw0
																												0	0	0	0

Bit	Name	Description
[31:4]	RSV	Reserved
[3]	PLL_LOCK	PLL Lock Status Flag 0: PLL clock is not ready 1: PLL clock is locked and valid
[2]	PLLCK_STATUS	PLL Clock Source Status 0: PLL clock is sourced from IFCK 1: PLL clock is sourced from EFCK
[1]	PLLLIF	PLL Loss Interrupt Flag Read 0: PLL is locked 1: PLL is not locked Write 0: This bit is cleared to “0” 1: No effect
[0]	MCDIF	External Fast Clock Missing Interrupt Flag Read 0: External fast lock is not missing 1: External fast lock is missing

		Write 0: This bit is cleared to “0” 1: No effect  Note: A write of “0” by software generates the flag clear signal MCDCLR

21.3 Clock Calibration

21.3.1 Introduction

Clock calibration is a feature that uses internal slow clock to calibrate the internal fast clock. Working principles: A 14-bit counter is used to count the length of 8 slow clock cycles with the fast clock as the clock source.

Calibration operations:

1. Set CAL_CR[CALBSY] = 1 in software to start the calibration;
2. Read CAL_CR[CALBSY] to check if the calibration process is completed;
3. Read CAL_CR[CAL_ARR] after the calibration is completed (CAL_CR[CALBSY] = 0), which represents the value of the length of counting 8 slow clock cycles.

21.3.2 Clock Calibration Registers

21.3.2.1 CAL_CR (CSR: 0x462)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CALBSY	RSV	CAL_ARR													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw1	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved

[15]	CALBSY	Clock Calibration Status Flag Read: 0: Clock calibration is completed 1: Clock calibration is in progress Write: 0: No effect 1: Clock calibration starts
[14]	RSV	Reserved
[13:0]	CAL_ARR	Calibration Counter Value Count value of 8 slow clock cycles using fast clock  Note: When this value is 0, it indicates that no corresponding slow clock input is detected, and when this value is 0x3FFF, it indicates that the counter overflows (slow clock is too slow or fast clock is too fast).

22 IWDT

The independent watchdog timer (IWDT) is a timer that works on the internal slow clock to monitor the master program operation and prevent the MCU running out. After the independent watchdog is enabled, IWDT starts counting. When IWDT overflows, the independent watchdog sends a signal to reset the MCU and the program restarts running from address 0. During the operation of master program, IWDT has to be initialized at regular intervals to prevent IWDT overflowing.

After the independent watchdog is enabled, IWDT starts counting from 0. When it reaches 0xFFFFC, the independent watchdog outputs a signal that is 4 internal slow clock cycles wide to reset MCU, and the program starts running from address 0. IWDT has to be initialized at regular intervals during operation, and IWDT rolls over to IWDT_REL and restart counting.

22.1 IWDT Features

- A free-running up-counter
- An independent RC oscillator as the clock source (works in standby mode)
- After the independent watchdog is enabled, IWDT resets when it reaches 0xFFFFC
- RST_SR[RSTWDT] is set to “1” when MCU is reset by IWDT overflow

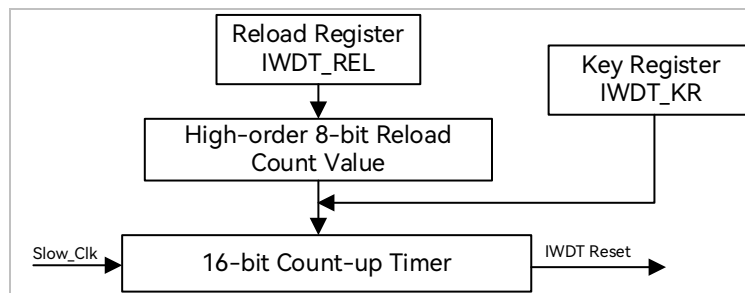
22.2 IWDT Operations

The independent watchdog is enabled after 0xCCCC is written to the key register. IWDT counts up from 0x0000. When reaching 0xFFFFC, IWDT generates a reset signal.

Whenever 0xAAAA is written to the key register, the value held in IWDT_REL is reloaded into IWDT to avoid a reset.

A write of 0x2222 to the key register disables the independent watchdog and stops IWDT. When IWDT is enabled again, it is cleared and starts counting from 0. The IWDT pauses counting whenever the CPU enters idle, stop or halt mode, and counting from the point where it stops once the CPU recovers.

Figure 22-1 Functional Block Diagram of IWDT



22.3 Hardware IWDT Reset

After IWDT is enabled in the project configuration, IWDT automatically starts counting after the system is powered on and reset. If no reset or disable instruction is written to the key register in the software before IWDT stops counting, the system generates a IWDT reset signal.

22.4 Access Protection of Key Register

The key register supports write protection. 0x5555 must be written before IWDT_KR register is updated. A write of a different value enables write protection and the register will not be updated. The reloading operation (a write of 0xAAAA) also enables write protection.

22.5 Debugging Mode

IWDT stops in the debugging mode.

22.6 IWDT Registers

22.6.1 IWDT_KR (CSR: 0x480)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																IWDT_KR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧	≧
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	IWDT_KR	Key Value (Write-only register with a read value 0x0000): 0xAAAA must be written in the software to initialize IWDT at regular intervals, otherwise, IWDT resets when it reaches 0xFFFFC. A write of 0x5555 releases the access protection. A write of 0xCCCC starts the independent watchdog (it is invalid if hardware watchdog reset is enabled). A write of 0x2222 disables the independent watchdog.

22.6.2 IWDT_REL(CSR: 0x481)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																WDT_REL															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≧	≧	≧	≧	≧	≧	≧	≧
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	WDT_REL	IWDT Reload Timer This bit sets eight high-order bits of the initialized value of IWDT.

23 WWDT

23.1 WWDT Introduction

The window watchdog timer (WWDT) is used to detect a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. An MCU reset is produced when WWDT reaches a programmed time period, unless this down-counter is refreshed before it is cleared to “0”. An MCU reset is also generated if this 7-bit down-counter is refreshed before it reaches the window register value. This implies that the down-counter must be refreshed in a limited window.

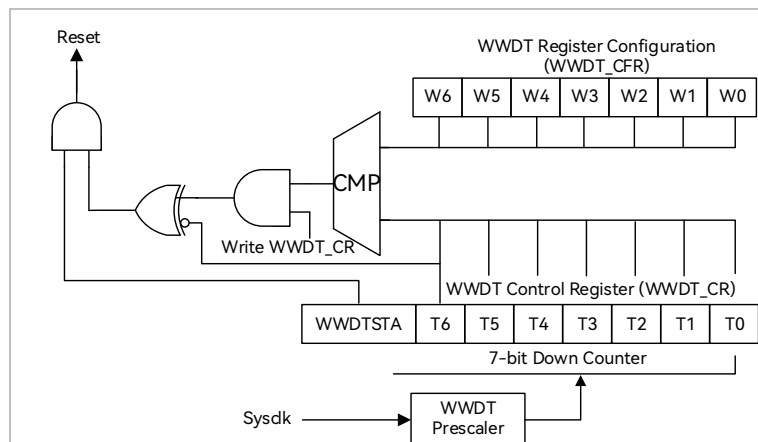
23.2 WWDT Features

- A programmable free-running down-counter
- Reset conditions (after the window watchdog is enabled)
 - WWDT resets when its value is less than 0x40
 - WWDT resets when it is refreshed outside of the window
- After the window watchdog is activated and WWDT interrupt is enabled, an early wake-up interrupt flag bit (WWDT_SR[EWIF]) is generated when this down-counter arrives at 0x40, which can be used for the reload timer to avoid WWDT reset

23.3 WWDT Functional Description

A WWDT reset occurs when the 7-bit down-counter WWDT is enabled and reaches 0x3F from 0x40. A WWDT reset is also generated if the software refreshes WWDT while WWDT is greater than the value held by the Window register.

Figure 23-1 Functional Block Diagram of WWDT



During normal operation, the application program must regularly refresh WWDT_CR register to prevent a MCU reset. The WWDT_CR register can be written in a range between 0xFF and 0xC0 only when the counter is smaller than the value held by the window register.

23.3.1 WWDT Enable

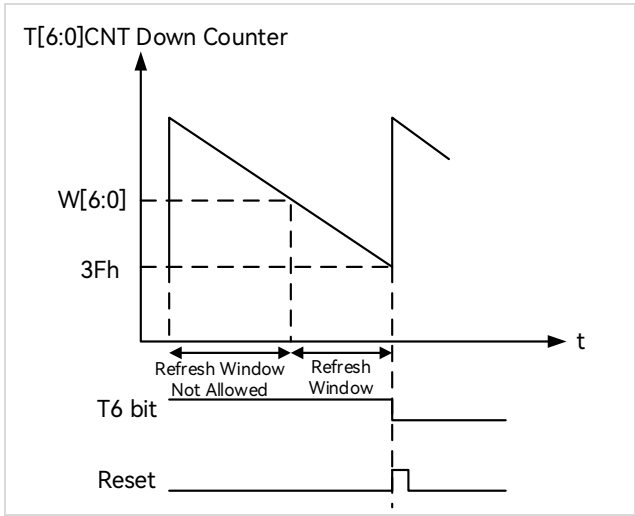
The window watchdog is always disabled after a system reset. Setting WWDT_CR[WWDTSTA] = 1 enables the watchdog, which cannot be disabled unless a reset occurs.

23.3.2 WWDT Control

The WWDT is a free-running timer. It continues decrement even when the window watchdog is disabled. When the window watchdog is enabled, WWDT_CR[TC] must be configured to prevent a reset.

WWDT_CR[TC] holds counting value of the window watchdog before the watchdog resets. The delay time before reset varies between a minimum and a maximum, because the prescaler value is unknown when WWDT_CR register is written. The configuration register (WWDT_CFR) contains maximum value of the window. To prevent a reset, the down-counter must be refreshed when it is smaller than the window register value and greater than 0x3F, where Figure 23-2 describes how the window register works. The early wake-up interrupt (EWIF) flag bit can be also used to refresh the counter. The interrupt flag bit is enabled when WWDT_CFR[WWDTIE] is set as “1”. An early wake-up interrupt is generated when the down-counter reaches 0x40. In this case, the corresponding ISR refreshes the timer to prevent a WWDT reset. A write of “0” to WWDT_SR[EWIF] clears this interrupt.

Figure 23-2 Timing Diagram of WWDT



Timing diagram of WWDT is shown in Figure 23-2. The formula for timeout is as follows:

$$T_{WWDT} = SYSCLK \times 2^{WWDTPSC} \times 4096 \times (T[6:0] + 1)$$

Where,

T_{WWDT} : WWDT Timeout Period

$SYSCLK$: Time Interval of the System Fast Clock

The minimum and maximum timeout period of WWDT under different time bases of the prescaler is shown in Table 23-1.

Table 23-1 Minimum and Maximum Timeout Period of WWDT
under Different Time Bases of Prescaler

WWDTPSC	Minimum Timeout	Maximum Timeout
0	85.3μs	5.46ms
1	170.7μs	10.92ms
2	341.3μs	21.84ms
3	682.6μs	43.69ms

23.4 WWDT Registers

23.4.1 WWDT_CR (CSR: 0x4A0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							WWDTSTA	TC							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw1	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	WWDTSTA	Window Watchdog Enable This bit is set to “1” by software, but can be cleared to “0” by the hardware after reset. When WWDTSTA = 1, a WWDT reset occurs. Read: 0: WWDT is disabled 1: WWDT is enabled Write: 0: No effect 1: WWDT starts
[6:0]	TC	7-bit Counter These bits are used to store counting value of the window watchdog. The counter decreases by 1 for every $SYSCLK \times 2^{WWDTPSC}$ fast clock cycle. A reset is generated when the counter arrives at 3Fh from 40h (T6 becomes 0).

23.4.2 WWDT_CFR (CSR: 0x4A1)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
RSV																					WWDTIE	WWDTPSC		WCFR								
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0		

Bit	Name	Description
[31:10]	RSV	Reserved
[9]	WWDTIE	WWDT Interrupt Enable Flag After this bit is enabled, an interrupt is generated when the counter reaches 40h. This interrupt can only be cleared by the hardware after a reset. 0: Disable 1: Enable
[8:7]	WWDTPSC	Time Base Time base of the prescaler can be set as follows: 00: Timer clock (SYSCLK divided by 4096) divided by 1 01: Timer clock (SYSCLK divided by 4096) divided by 2 10: Timer clock (SYSCLK divided by 4096) divided by 4 11: Timer clock (SYSCLK divided by 4096) divided by 8
[6:0]	WCFR	7-bit Counter These bits are used to store counting value of WWDT. A WWDT reset is generated when WWDT is greater than the value held by window register and WWDT is refreshed.

23.4.3 WWDT_SR (CSR: 0x4A2)

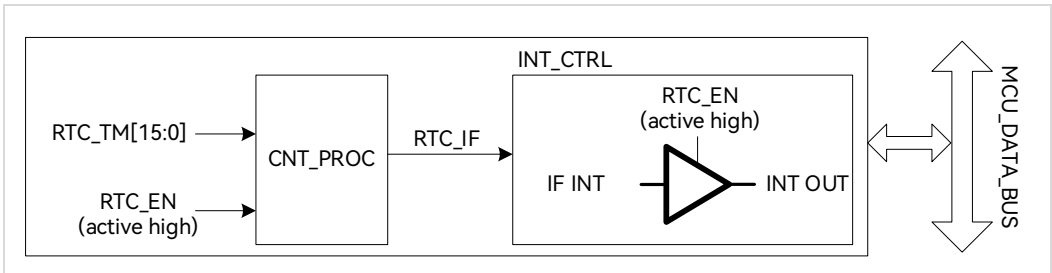
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																															EWIF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

Bit	Name	Description
[31:1]	RSV	Reserved
[0]	EWIF	Window Watchdog Interrupt Flag This bit is set to “1” by hardware when WWDT reaches 40h. It can be cleared to “0” by software only. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

24 RTC

24.1 RTC Functional Block Diagram

Figure 24-1 RTC Functional Block Diagram



24.2 RTC Operations

A write to RTC_DR sets RTC reload value. RTC is enabled when RTC_CR[RTCEN] is set to “1”. RTC interrupt is enabled when PIE[RTCIE] is set to “1”, and the interrupts are accessed by 23.

24.3 RTC Registers

24.3.1 RTC_CR (CSR: 0x460)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							RTCEN	RTCIF	RSV	ISOCEN	RSV				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw0	-	rw	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	-	-	-	-

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	RTCEN	RTC Enable 0: Disable 1: Enable
[6]	RTCIF	RTC Interrupt Flag Read:

		0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect
[5]	RSV	Reserved
[4]	ISOSCEN	Internal Slow Clock Enable 0: Disable 1: Enable
[3:0]	RSV	Reserved

24.3.2 RTC_DR (CSR: 0x461)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																RTC_DR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘	⌘
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	RTC_DR	RTC Counting Memory Read: RTC Current Value Write: RTC Overload Value

25 IO

25.1 IO Introduction

- > FU7512Q1 has up to 46 GPIO pins, including PA0 ~ PA7, PA9 ~ PA15, PB0 ~ PB13, PB15, PC0 ~ PC7, PC9 ~ PC10, PC12 ~ PC13, PC15, PD0, PD2, and PD5.
- > FU7564Q1 has up to 29 GPIO pins, including PA0 ~ PA3, PA10 ~ PA15, PB0 ~ PB6, PB8 ~ PB9, PB11 ~ PB12, PB15, PC3 ~ PC7, PC15, and PD5.
- > FU7565Q1 has up to 21 GPIO pins, including PA0 ~ PA3, PA10 ~ PA12, PB0 ~ PB6, PB8, PB15, PC9 ~ PC11, PD0, and PD5.
- > FU7574Q1 has up to 36 GPIO pins, including PA0 ~ PA3, PB0 ~ PB6, PB8 ~ PB9, PB11 ~ PB12, PB14 ~ PB15, PC0 ~ PC7, PC9 ~ PC10, PC12 ~ PC13, PC15, PD0, and PD2 ~ PD6.

25.2 IO Operations

Each GPIO port pin has relevant registers to meet different application requirements. For example, PA0 ~ PA15 is mapped to register PA, and PB0 ~ PB15 to register PB. PA_OE and PB_OE registers are configured for digital input and output.

- > The enable bits of pull-up resistors and pull-down resistors are configured to “1”. See 25.3.8 PA_PU (CSR: 0x002) ~ 25.3.12 PA_PL (CSR: 0x003) for port pins and registers.
- > See 5.3 GPIO Electrical Characteristics for the values of pull-up resistors and pull-down resistors.
- > The relevant bits of PB_AN/PC_AN/PD_AN registers are configured to “1” to activate analog signal mode. See 25.3.5 PB_AN (CSR: 0x013) ~ 25.3.7 PD_AN (CSR: 0x033) for port pins and registers. After the port pins are configured to analog mode, all their digital features are disabled and the port state is 0 by reading relevant bits in PB/PC/PD registers.

25.3 IO Registers

25.3.1 PA_OE (CSR: 0x001)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PA_OE[15:9]						RSV	PA_OE[7:0]								
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:9]	PA_OE[15:9]	PA15 ~ PA9 Digital I/O Selection 0: Input 1: Output
[8]	RSV	Reserved
[7:0]	PA_OE[7:0]	PA7 ~ PA0 Digital I/O Selection 0: Input 1: Output

25.3.2 PB_OE (CSR: 0x011)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PB_OE[15:0]															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PB_OE[15:0]	PB15 ~ PB0 Digital I/O Selection 0: Input 1: Output

25.3.3 PC_OE (CSR: 0x021)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PC_OE[15]	RSV	PC_OE[13:9]					RSV	PC_OE[7:0]							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	PC_OE[15]	PC15 Digital I/O Selection 0: Input 1: Output
[14]	RSV	Reserved
[13:9]	PC_OE[13:9]	PC13 ~ PC9 Digital I/O Selection 0: Input 1: Output
[8]	RSV	Reserved
[7:0]	PC_OE[7:0]	PC7 ~ PC0 Digital I/O Selection 0: Input 1: Output

25.3.4 PD_OE (CSR: 0x031)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							PD_OE[6:2]					RSV	PD_OE[0]		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	-	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	0	

Bit	Name	Description
[31:7]	RSV	Reserved
[6:2]	PD_OE[6:2]	PD6 ~ PD2 Digital I/O Selection 0: Input 1: Output
[1]	RSV	Reserved
[0]	PD_OE[0]	PD0 Digital I/O Selection 0: Input

1: Output

25.3.5 PB_AN (CSR: 0x013)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PB_AN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PB_AN	PB15 ~ PB0 Analog Mode Enable 0: Disable 1: Enable

25.3.6 PC_AN (CSR: 0x023)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PC_AN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PC_AN	PC15 ~ PC0 Analog Mode Enable 0: Disable 1: Enable

25.3.7 PD_AN (CSR: 0x033)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								PD_AN[6:2]						RSV	PD_AN[0]
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	-	rw

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	0

Bit	Name	Description
[31:7]	RSV	Reserved
[6:2]	PD_AN[6:2]	PD6 ~ PD2 Analog Mode Enable 0: Disable 1: Enable
[1]	RSV	Reserved
[0]	PD_AN[0]	PD0 Analog Mode Enable 0: Disable 1: Enable

25.3.8 PA_PU (CSR: 0x002)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PA_PU[15:9]						RSV	PA_PU[7:0]								
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:9]	PA_PU[15:9]	PA15 ~ PA9 Pull-up Resistor Enable 0: Disable 1: Enable
[8]	RSV	Reserved
[7:0]	PA_PU[7:0]	PA7 ~ PA0 Pull-up Resistor Enable 0: Disable 1: Enable

25.3.9 PB_PU (CSR: 0x012)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PB_PU															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	

[0]	PD_PU[0]	PD0 Pull-up Resistor Enable 0: Disable 1: Enable

25.3.12 PA_PL (CSR: 0x003)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PA_PL[15:9]						RSV	PA_PL[7:4]				ODEN		PA_PL[1:0]		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:4]	PA_PL[15:9]	PA15 ~ PA9 Pull-down Resistor Enable 0: Disable 1: Enable
[8]	RSV	Reserved
[7:4]	PA_PL[7:4]	PA7 ~ PA4 Pull-down Resistor Enable 0: Disable 1: Enable
[3:2]	ODEN	PA1 ~ PA0 Open-Drain Output Enable 0: Disable 1: Enable
[1:0]	PA_PL[1:0]	PA1 ~ PA0 Pull-down Resistor Enable 0: Disable 1: Enable

25.3.13 PH_SEL (CSR: 0x060)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SFRECT	T5SEL	T8CT	DBG1CT	BISSSEL	CMPTCT	MONCT	SPI2TMOD	SPI1TMOD	I2CCT	CANCT	LINCT	UT2CT	UT1CT	T7CT	RSV	T6ACT	T5BCT	T5ACT	T4CT	T3CT	RSV	T2BCT	T2ACT								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0

Bit	Name	Description
[31]	SFRECT	Pin Multiplexed as SFRE 0: PA12 acts as SFRE 1: PA13 acts as SFRE
[30]	T5SEL	Pin Multiplexed as Timer5/QEP1 Combined configuration with PH_SEL[T5ACT] and PH_SEL[T5BCT] > PH_SEL[T5SEL] : PH_SEL[T5ACT] 01: PA13 acts as Timer5 input/output or QEP1A input 11: PA4 acts as Timer5 input/output or QEP1A input > PH_SEL[T5SEL] : PH_SEL[T5BCT] 01: PA14 acts as Timer5 input/output or QEP1B input 11: PA5 acts as Timer5 input/output or QEP1B input > PH_SEL[T5SEL] 00: PA15 acts as QEP1Z input 01: PA6 acts as QEP1Z input
[29:28]	T8CT	Pin Multiplexed as Timer8 00/11: Disable 01: PA9 acts as Timer8 input/output 10: PB2 acts as Timer8 input/output
[27]	DBG1CT	Pin Multiplexed as DBG1 0: PA1 acts as DBG1 1: PA9 acts as DBG1
[26]	BISSSEL	Pin Multiplexed as BISS 0: PA10 and PA11 acts as MA and SLO respectively 1: PA13 and PA14 acts as MA and SLO respectively
[25]	CMPCT	Pin Multiplexed as Comparator Output 0: PA1 acts as comparator output 1: PA3 acts as comparator output
[24:23]	MONCT	Pin Multiplexed as DataMonitor 00: PA9 acts as DataMonitor 01: PA0 acts as DataMonitor 1x: PB0 acts as DataMonitor
[22]	SPI2TMOD	MISO Pin Status after SPI2 Slave Device Completes Transmission 0: Output State 1: High-impedance State
[21]	SPI1TMOD	MISO Pin Status after SPI1 Slave Device Completes Transmission

		0: Output State 1: High-impedance State
[20]	I2CCT	Pin Multiplexed as I ² C1 0: PA0 and PA1 act as SDA1 and SCL1 respectively 1: Disable
[19]	CANCT	Pin Multiplexed as CAN 0: PA0 and PA1 act as CTX and CRX respectively 1: PA5 and PA4 act as CTX and CRX respectively
[18]	LINCT	Pin Multiplexed as LIN 0: PA0 and PA1 act as LTX and LRX respectively 1: PA5 and PA4 act as LTX and LRX respectively
[17:16]	UT2CT	Pin Multiplexed as UART2 00: PA2 and PA3 act as TXD2 and RXD2 respectively 01: PA5 and PA4 act as TXD2 and RXD2 respectively 1x: PB2 (Single-wire Mode: IO; Non-single-wire Mode: O)
[15:14]	UT1CT	Pin Multiplexed as UART1 00: PA0 and PA1 act as TXD1 and RXD1 respectively 01: PA7 and PA6 act as TXD1 and RXD1 respectively 1x: PA10 and PA11 act as TXD1 and RXD1 respectively
[13:12]	T7CT	Pin Multiplexed as Timer7 00: Disable 01: PA1 acts as Timer7 input/output 10: PA3 acts as Timer7 input/output 11: PD0 acts as Timer7 input/output
[11]	RSV	Reserved
[10:9]	T6ACT	Pin Multiplexed as Timer6 0x: Disable 10: PA7 acts as Timer6 input/output 11: PA3 acts as Timer6 input/output
[8]	T5BCT	Pin Multiplexed as Timer5/QEP1B Combined configuration with PH_SEL[T5SEL] PH_SEL[T5SEL]: PH_SEL[T5BCT] 01: PA14 acts as Timer5 input/output or QEP1B input 11: PA5 acts as Timer5 input/output or QEP1B input
[7]	T5ACT	Pin Multiplexed as Timer5/QEP1A Combined configuration with PH_SEL[T5SEL] PH_SEL[T5SEL]: PH_SEL[T5ACT] 01: PA13 acts as Timer5 input/output or QEP1A input 11: PA4 acts as Timer5 input/output or QEP1A input

[6:5]	T4CT	Pin Multiplexed as Timer4 00: Disable 01: PA0 acts as Timer4 input/output 10: PA2 acts as Timer4 input/output 11: PD3 acts as Timer4 input/output
[4:3]	T3CT	Pin Multiplexed as Timer3 00: Disable 10: PA0 acts as Timer3 input/output 11: PA2 acts as Timer3 input/output
[2]	RSV	Reserved
[1]	T2BCT	Pin Multiplexed as Timer2 0: Disable 1: PA11 acts as Timer2 input/output
[0]	T2ACT	Pin Multiplexed as Timer2 0: Disable 1: PA10 acts as Timer2 input/output

25.3.14 PH_SEL1 (CSR: 0x061)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																												PFC02CT	PFC01CT	RSV	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	-

Bit	Name	Description
[31:4]	RSV	Reserved
[3]	PFCO2CT	Pin Multiplexed as PFC PWM2 Output 0: PA7 acts as PFC_O2 1: PA3 acts as PFC_O2S
[2]	PFCO1CT	Pin Multiplexed as PFC PWM1 Output 0: PA6 acts as PFC_O1 1: PA2 acts as PFC_O1S
[1:0]	RSV	Reserved

25.3.15 PA (CSR: 0x000)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PA[15:9]						RSV	PA[7:0]								
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:9]	PA[15:9]	PA15 ~ PA9
[8]	RSV	Reserved
[7:0]	PA[7:0]	PA7 ~ PA0

25.3.16 PB (CSR: 0x010)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PB															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PB	PB15 ~ PB0

25.3.17 PC (CSR: 0x020)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																PC															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	PC	PC15 ~ PC0

25.3.18 PD (CSR: 0x030)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								PD[6:2]					RSV	PD[0]	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	-	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	-	0

Bit	Name	Description
[31:7]	RSV	Reserved
[6:2]	PD[6:2]	PD6 ~ PD2
[1]	RSV	Reserved
[0]	PD[0]	PD0

26 Temperature Sensor

The chip integrates a temperature sensor. Setting TSD_CR[TSEN_EN] to “1” enables temperature sensor. Once activated, the sensor generates a digital code corresponding to the chip’s internal temperature. The sensed temperature ranges from 67.7°C ~ 161.8°C, as shown in Table 26-1.

TSD interrupt is enabled when PIE[TSDIE] is set to “1”, and the interrupts are accessed by 0.

Table 26-1 Mapping between Output Codes and Temperature Levels

TSEN_DR	Temperature (°C)	TSEN_DR	Temperature (°C)
0111111	67.7	1100000	109.1
1000000	68.6	1100001	110.6
1000001	69.7	1100010	112.1
1000010	70.8	1100011	113.6
1000011	71.9	1100100	115.1
1000100	73.1	1100101	116.7
1000101	74.2	1100110	118.2
1000110	75.3	1100111	119.7
1000111	76.5	1101000	121.3
1001000	77.7	1101001	122.9
1001001	78.8	1101010	124.5
1001010	80.0	1101011	126.2
1001011	81.2	1101100	127.8
1001100	82.4	1101101	129.5
1001101	83.7	1101110	131.1
1001110	84.9	1101111	132.9
1001111	86.1	1110000	134.5
1010000	87.3	1110001	136.3
1010001	88.6	1110010	138.0
1010010	89.9	1110011	139.7
1010011	91.2	1110100	141.5
1010100	92.5	1110101	143.3
1010101	93.8	1110110	145.1
1010110	95.1	1110111	146.9
1010111	96.5	1111000	148.7
1011000	97.8	1111001	150.5

TSEN_DR	Temperature (°C)	TSEN_DR	Temperature (°C)
1011001	99.2	1111010	152.4
1011010	100.5	1111011	154.3
1011011	101.9	1111100	156.1
1011100	103.3	1111101	158.0
1011101	104.8	1111110	159.9
1011110	106.3	1111111	161.8
1011111	107.7	-	-

26.1 Temperature Sensor Registers

26.1.1 TSD_CR (CSR: 0x630)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							TSD_EN	TSEN_EN	TSEN_HYS	RSV	TSD_ADJ				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	-	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	1	1	0	1	

Bit	Name	Description				
[31:8]	RSV	Reserved				
[7]	TSD_EN	TSD Enable 0: Disable 1: Enable				
[6]	TSEN_EN	Temperature Sensor Enable 0: Disable 1: Enable				
[5]	TSEN_HYS	Output Filter Width of Temperature Sensor 0: Filter width is 1 code value 1: Filter width is 2 code value				
[4]	RSV	Reserved				
[3:0]	TSD_ADJ	Thermal Shutdown (TSD) Threshold Table 26-2 Mapping between TSD Codes and Protection Temperatures <table><tr><th>TSD_ADJ</th><th>Temperature (°C)</th></tr><tr><td>0000</td><td>82.7</td></tr></table>	TSD_ADJ	Temperature (°C)	0000	82.7
TSD_ADJ	Temperature (°C)					
0000	82.7					

			0001	87.7
			0010	92.7
			0011	97.9
			0100	103.7
			0101	109.3
			0110	115.3
			0111	121.5
			1000	128.1
			1001	134.7
			1010	141.7
			1011	148.7
			1100	156.3
			1101	163.7

26.1.2 TSEN_DR (CSR: 0x631)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								TSEN_DR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	

Bit	Name	Description
[31:7]	RSV	Reserved
[6:0]	TSEN_DR	Temperature Sensor Output Codes Read this register, and find out the temperature of the chip according to Table 26-1 Mapping between Output Codes and Temperature Levels

27 ADC

27.1 ADC Introduction

The ADC module is a 12-bit successive approximation register ADC. There are three independent ADCs in the chip, of which ADC1 has up to 13 channels, ADC2 has up to 15 channels, and ADC3 has up to 3 channels. ADC1 and ADC2 support sequential sampling (from ADC channel 0 to ADC channel 13 in sequence) and triggered sampling (FOC triggered sampling mode), and ADC3 supports sequential sampling and triggered sampling (PFC carrier triggered sampling mode). The results of sequential sampling are stored in ADC1_DRx/ADC2_DRx/ADC3_DR2(x = 0 ~ 13) in a right-aligned or left-second-highest-bit-aligned format. The result of triggered sampling (ADC1 and ADC2) is sent to FOC module for motor control instead of ADC1_DRx/ADC2_DRx. The relevant registers of the FOC module are always left-second-highest-bit-aligned to store the triggered sample results. Triggered sampling is done automatically by hardware, and sequential sampling is controlled by software. The priority of triggered sampling is higher than that of sequential sampling. If both triggered sampling and sequential sampling are applied at the same time, ADC module first performs the triggered sampling, and then automatically restores sequential sampling mode upon completion of triggered sampling.

The clock source of ADC is at a rate of 24MHz and the sampling time is set by ADC1_SCYC, ADC2_SCYC and ADC3_SCYC.

27.2 Block Diagram of ADC Module

Figure 27-1 Functional Block Diagram of ADC1 Multiplexer

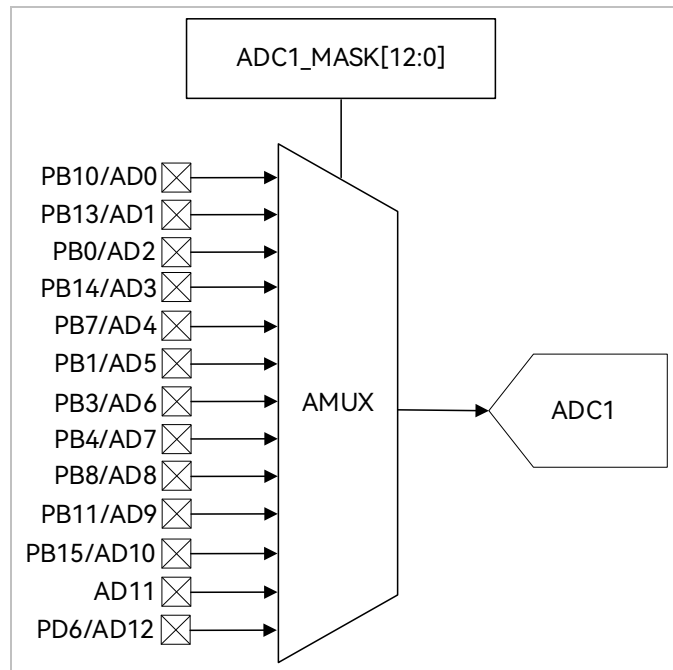


Figure 27-2 Functional Block Diagram of ADC2 Multiplexer

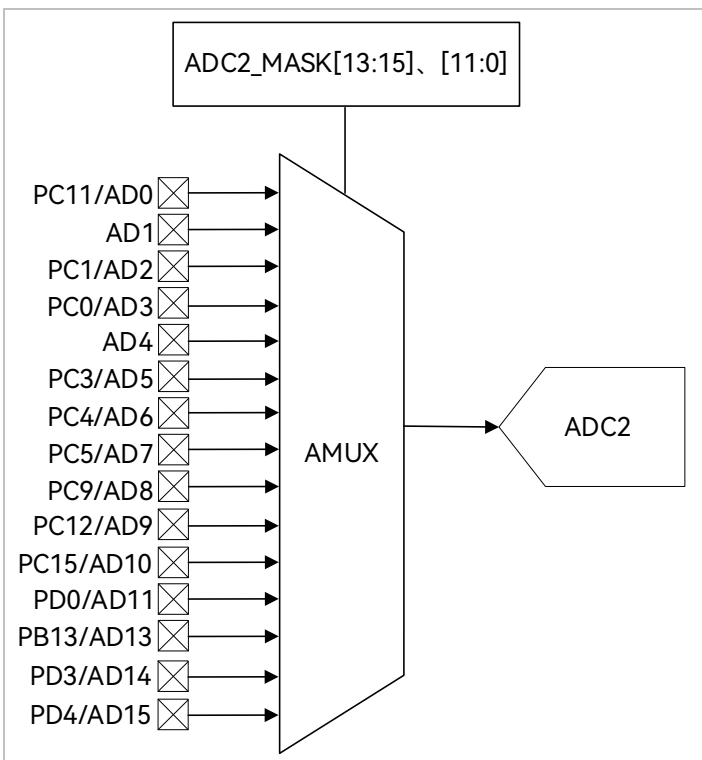


Figure 27-3 Functional Block Diagram of ADC3 Multiplexer

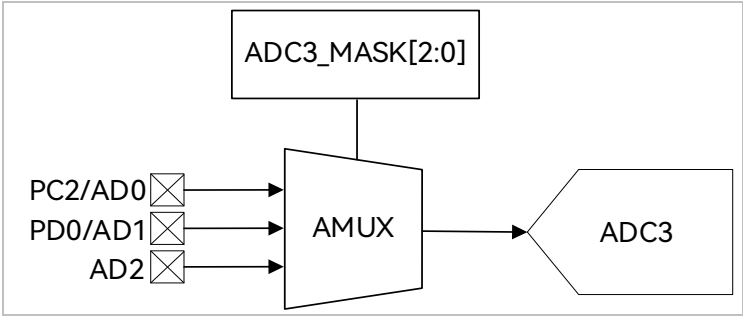


Figure 27-4 Functional Block Diagram of ADC1

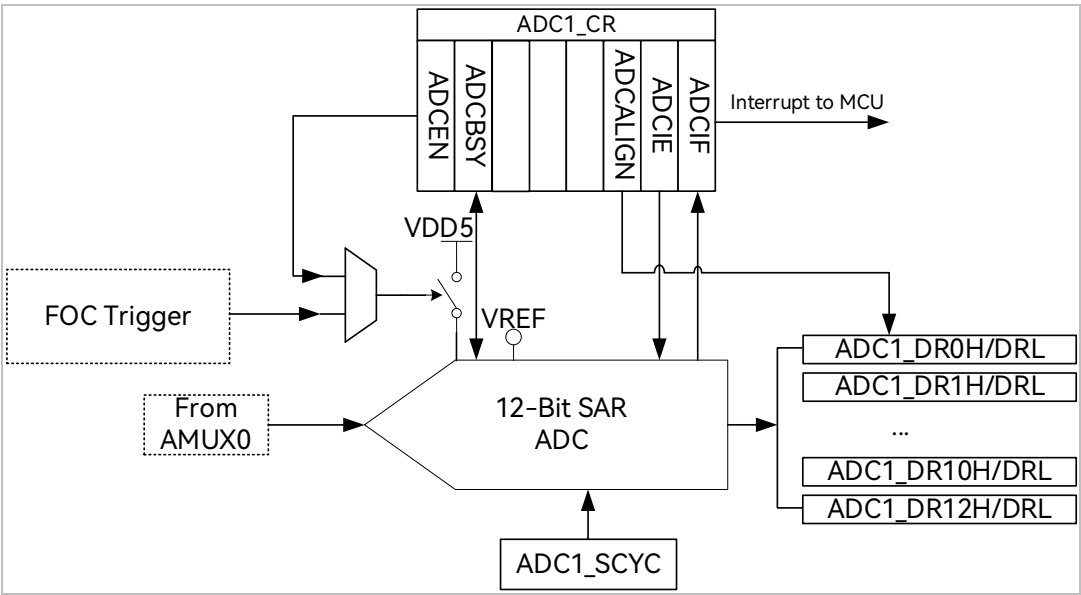


Figure 27-5 Functional Block Diagram of ADC2

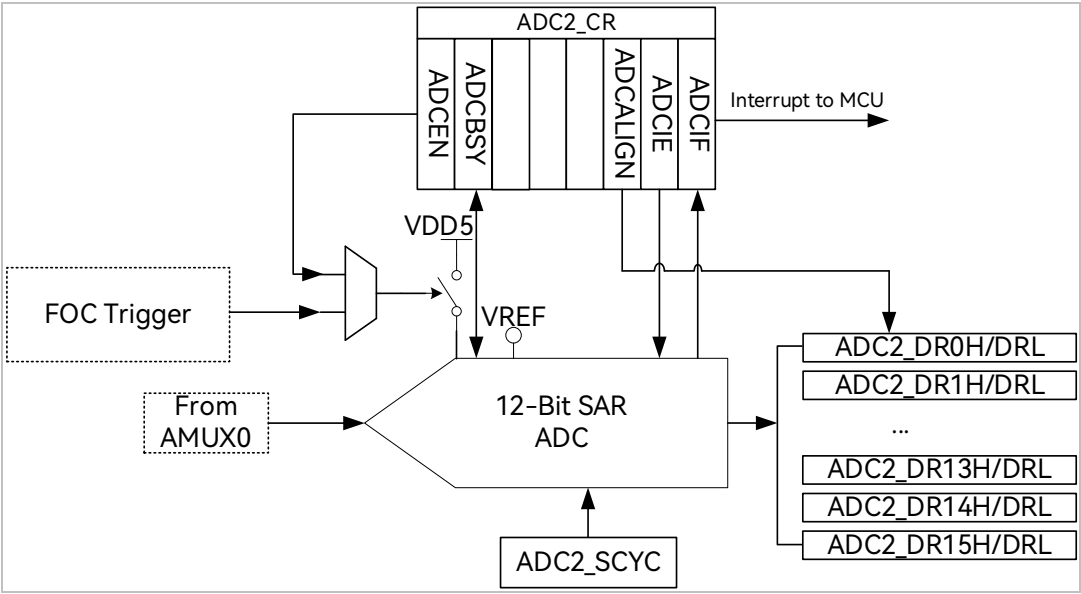
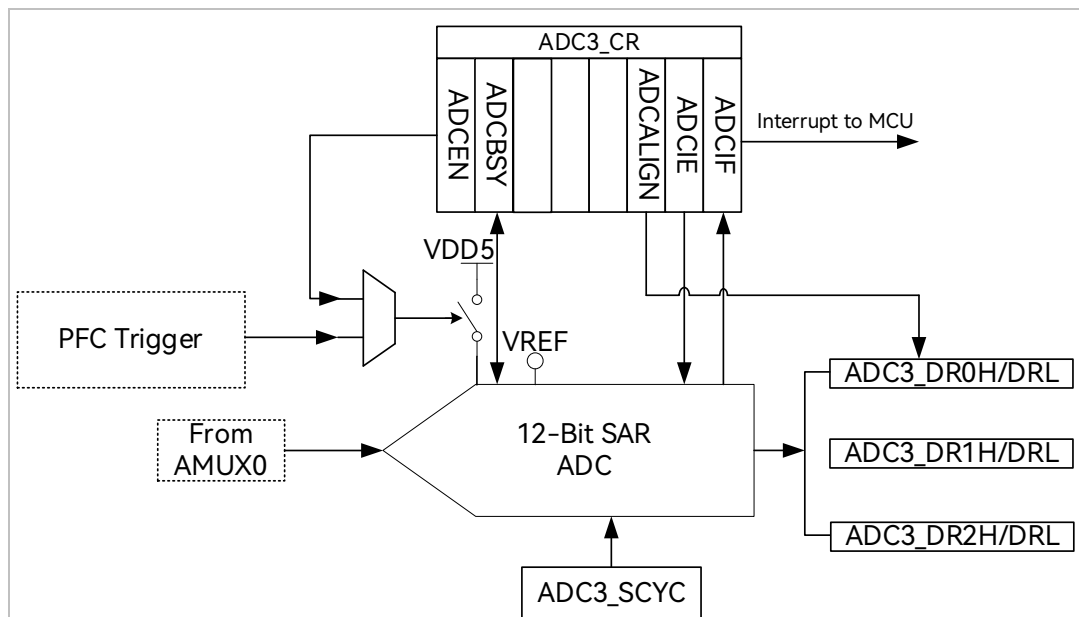


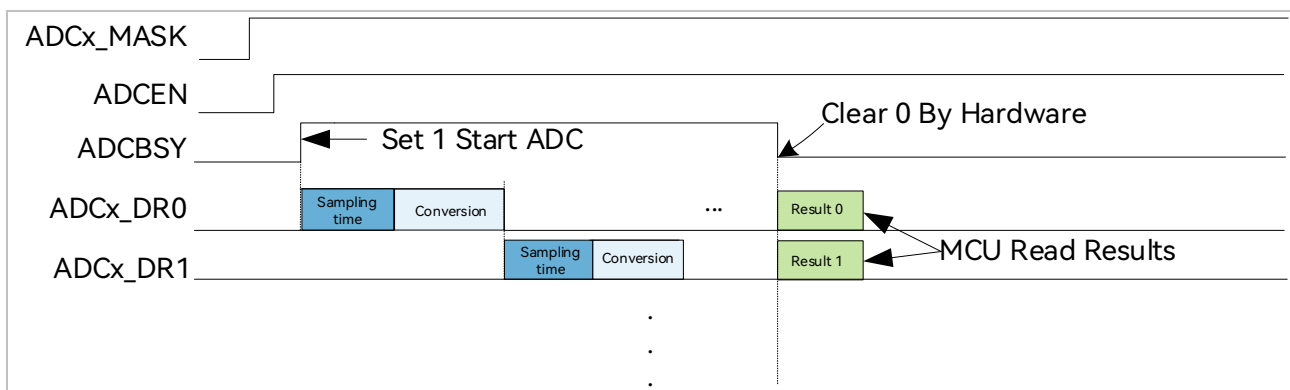
Figure 27-6 Functional Block Diagram of ADC3



27.3 ADC Operations

27.3.1 Sequential Sampling Mode

Figure 27-7 ADC Sequential Sampling Timing



ADC operations:

1. Set the appropriate ADC VREF;
2. Configure ADCx_MASK to enable the corresponding channel required to sample;
3. Configure ADCx_SCYC (minimum value is 3) to select the sampling period of each channel;
4. Configure ADCx_CR[ADCEN] = 1 to enable ADC;

5. Configure `ADCx_CR[ADCBSY] = 1` to start ADC;
6. Read ADC results when `ADCx_CR[ADCBSY] = 0`.

**Note:**

The ADC conversion sequence is from low to high based on the enabled channel (i.e., when channel 2/3/4 is enabled, the signal is sampled in order of 2/3/4, and then a single conversion result is obtained when `ADCx_CR[ADCBSY] = 0`).

27.3.2 Triggered Sampling Mode

27.3.2.1 ADC1

When FOC module is enabled, ADC channel 0/1/2/4 are selected for FOC triggered sampling, and channel 2 is used for bus voltage triggered sampling. In single-shunt current sampling mode, channel 4 is used for itrip sampling. In dual-shunt current sampling mode, channel 0 is used for ia sampling and channel 1 for ib sampling. In triple-shunt current sampling mode, channel 0 is used for ia sampling, channel 1 for ib sampling, and channel 4 for ic sampling.

27.3.2.2 ADC2

When FOC module is enabled, ADC channel 0/1/4 are selected for FOC triggered sampling. In single-shunt current sampling mode, channel 4 is used for itrip sampling. In dual-shunt current sampling mode, channel 0 is used for ia sampling and channel 1 for ib sampling. In triple-shunt current sampling mode, channel 0 is used for ia sampling, channel 1 for ib sampling, and channel 4 for ic sampling.

27.3.2.3 ADC3

When PFC module is enabled, ADC channel 0/1/2 are selected for PFC carrier triggered sampling. Channel 0 is used for PFC current sampling, channel 1 for PFC AC voltage sampling of PFC circuit 1, and channel 2 for current sampling of PFC circuit 2.

27.3.3 Output Data Format

Registers `ADC1_DRx/ADC2_DRx/ADC3_DRx` contain the ADC sampling results. These data can be right-aligned or left-second-highest-bit-aligned by configuring `ADCx_CR[ADCALIGN]`. The relationship between the output values and data alignment is shown in Table 27-1. The bits, which are not used in `ADC1_DRx/ADC2_DRx/ADC3_DRx`, are set to “0”.

Table 27-1 Relation between Output Voltage and Data Alignment

Input Voltage	Right-aligned	Left-second-highest-aligned
0	0x0000	0x0000
VREF/2	0x0800	0x4000
VREF	0x0FFF	0x7FF8

27.4 ADC Registers

27.4.1 ADCx_CR (CSR: 0x660/0x670/0x680) (x = 1/2/3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							ADCEN	ADCBSY	RSV			ADCALIGN	ADCIE	ADCIF	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw1	-	-	-	rw	rw	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	-	-	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	ADCEN	ADC Enable 0: Disable 1: Enable
[6]	ADCBSY	ADC Start & ADC Busy Flag Read: 0: ADC is idle 1: ADC is busy Write: 0: No effect 1: ADC conversion starts  Note: Writing “1” to this bit has no effect when ADC_MASK = 0.
[5:3]	RSV	Reserved
[2]	ADCALIGN	ADC Data Alignment Selection 0: Right-aligned 1: Left-second-highest-bit-aligned

		 Note: The results of triggered sampling mode are always left-second-highest-bit-aligned.
[1]	ADCIE	ADC Interrupt Enable (those in triggered sampling mode are not included) 0: Disable 1: Enable
[0]	ADCIF	ADC Interrupt Flag This bit is set to “1” by hardware when ADC conversion is completed. Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect

27.4.2 ADCx_MASK (CSR: 0x661/0x671/0x681) (x = 1/2/3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CH15EN	CH14EN	CH13EN	CH12EN	CH11EN	CH10EN	CH9EN	CH8EN	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN	CH0EN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15]	CH15EN	ADC Channel 15 Enable
[14]	CH14EN	ADC Channel 14 Enable
[13]	CH13EN	ADC Channel 13 Enable
[12]	CH12EN	ADC Channel 12 Enable
[11]	CH11EN	ADC Channel 11 Enable
[10]	CH10EN	ADC Channel 10 Enable
[9]	CH9EN	ADC Channel 9 Enable
[8]	CH8EN	ADC Channel 8 Enable
[7]	CH7EN	ADC Channel 7 Enable
[6]	CH6EN	ADC Channel 6 Enable
[5]	CH5EN	ADC Channel 5 Enable

[4]	CH4EN	ADC Channel 4 Enable
[3]	CH3EN	ADC Channel 3 Enable
[2]	CH2EN	ADC Channel 2 Enable
[1]	CH1EN	ADC Channel 1 Enable
[0]	CH0EN	ADC Channel 0 Enable



Note:

In triggered sampling mode, it is not required to configure ADCx_MASK.

27.4.3 ADC1_SCYC (CSR: 0x662)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																ADC1_SCYC3[15:12]				ADC1_SCYC2[11:8]				ADC1_SCYC1[7:4]				ADC1_SCYC0[3:0]			
																-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:12]	ADC1_SCYC3 [15:12]	ADC1 Sampling Cycle for ADC Channel 3, 8, 9, 10, and 12 ADC1_SCYC3[15] = 0: ADC1_SCYC3[14:12] ADC clock cycles ADC1_SCYC3[15] = 1: (ADC1_SCYC3[14:12]*8 + 7) ADC clock cycles
[11:8]	ADC1_SCYC2 [11:8]	ADC1 Sampling Cycle for ADC Channel 5, 6 and 7 ADC1_SCYC2[11] = 0: ADC1_SCYC2[10:8] ADC clock cycles ADC1_SCYC2[11] = 1: (ADC1_SCYC2[10:8]*8 + 7) ADC clock cycles
[7:4]	ADC1_SCYC1 [7:4]	ADC1 Sampling Cycle for ADC Channel 2 ADC1_SCYC1[7] = 0: ADC1_SCYC1[6:4] ADC clock cycles ADC1_SCYC1[7] = 1: (ADC1_SCYC1[6:4]*8 + 7) ADC clock cycles
[3:0]	ADC1_SCYC0 [3:0]	ADC1 Sampling Cycle for ADC Channel 0, 1, 4 and 11 ADC1_SCYC0[3] = 0: ADC1_SCYC0[2:0] ADC clock cycles ADC1_SCYC0[3] = 1: (ADC1_SCYC0[2:0]*8 + 7) ADC clock cycles

27.4.4 ADC2_SCYC (CSR: 0x672)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																ADC2_SCYC3[15:12]				ADC2_SCYC2[11:8]				ADC2_SCYC1[7:4]				ADC2_SCYC0[3:0]			
																rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:12]	ADC2_SCYC3 [15:12]	ADC2 Sampling Cycle for ADC Channel 3, 8, 9, 10, 14, and 15 ADC2_SCYC3[15] = 0: ADC2_SCYC3[14:12] ADC clock cycles ADC2_SCYC3[15] = 1: (ADC2_SCYC3[14:12]*8 + 7) ADC clock cycles
[11:8]	ADC2_SCYC2 [11:8]	ADC2 Sampling Cycle for ADC Channel 5, 6 and 7 ADC2_SCYC2[11] = 0: ADC2_SCYC2[10:8] ADC clock cycles ADC2_SCYC2[11] = 1: (ADC2_SCYC2[10:8]*8 + 7) ADC clock cycles
[7:4]	ADC2_SCYC1 [7:4]	ADC2 Sampling Cycle for ADC Channel 2 and 11 ADC2_SCYC1[7] = 0: ADC2_SCYC1[6:4] ADC clock cycles ADC2_SCYC1[7] = 1: (ADC2_SCYC1[6:4]*8 + 7) ADC clock cycles
[3:0]	ADC2_SCYC0 [3:0]	ADC2 Sampling Cycle for ADC Channel 0, 1, 4 and 13 ADC2_SCYC0[3] = 0: ADC2_SCYC0[2:0] ADC clock cycles ADC2_SCYC0[3] = 1: (ADC2_SCYC0[2:0]*8 + 7) ADC clock cycles

27.4.5 ADC3_SCYC (CSR: 0x682)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								ADC3_SCYC1[7:4]				ADC3_SCYC0[3:0]			
																								rW	rW	rW	rW	rW	rW	rW	rW
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:4]	ADC3_SCYC1 [7:4]	ADC3 Sampling Cycle for ADC Channel 0 and 2 ADC3_SCYC1[7] = 0: ADC3_SCYC1[6:4] ADC clock cycles ADC3_SCYC1[7] = 1: (ADC3_SCYC1[6:4]*8 + 7) ADC clock cycles
[3:0]	ADC3_SCYC0 [3:0]	ADC Sampling Cycle for ADC Channel 1 ADC3_SCYC0[3] = 0: ADC3_SCYC0[2:0] ADC clock cycles ADC3_SCYC0[3] = 1: (ADC3_SCYC0[2:0]*8 + 7) ADC clock cycles

27.4.6 ADC1_DRx (0x40000040)

Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
00h	ADC1_DR0														
02h	ADC1_DR1														
04h	ADC1_DR2														
06h	ADC1_DR3														
08h	ADC1_DR4														
0Ah	ADC1_DR5														
0Ch	ADC1_DR6														
0Eh	ADC1_DR7														
10h	ADC1_DR8														
12h	ADC1_DR9														
14h	ADC1_DR10														
16h	ADC1_DR11														
18h	ADC1_DR12														

27.4.7 ADC2_DRx (0x40000060)

Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
00h	ADC2_DR0														
02h	ADC2_DR1														
04h	ADC2_DR2														
06h	ADC2_DR3														
08h	ADC2_DR4														
0Ah	ADC2_DR5														
0Ch	ADC2_DR6														
0Eh	ADC2_DR7														
10h	ADC2_DR8														

Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
12h	ADC2_DR9														
14h	ADC2_DR10														
16h	ADC2_DR11														
18h	RSV														
1Ah	ADC2_DR13														
1Ch	ADC2_DR14														
1Eh	ADC2_DR15														

27.4.8 ADC3_DRx (CSR: 0x683/0x684/0x685) (x = 0/1/2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV												ADC3_DRx																			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1	1	1
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11:0]	ADC3_DRx	ADC3 Channel X Conversion Results in Sequential Sampling Mode Data is aligned according to ADCx_CR[ADCALIGN].  Note: The ADC results are not updated to this register in triggered sampling mode

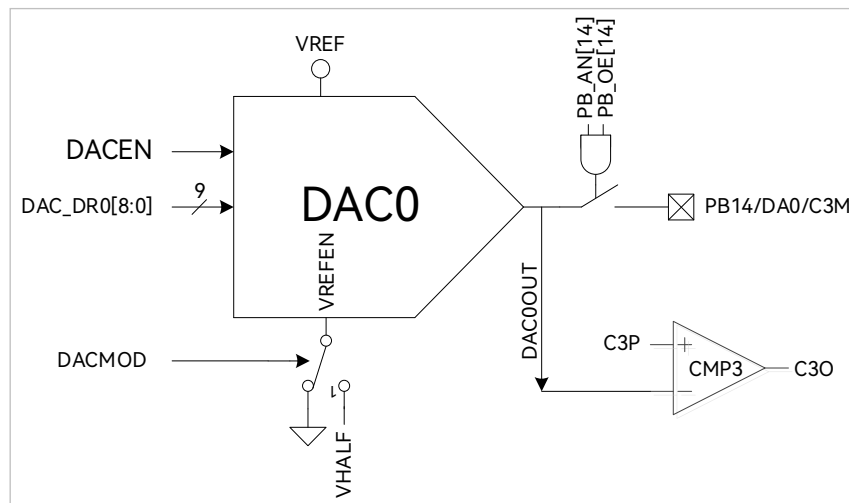
28 DAC

28.1 DAC Introduction

The chip integrates five DAC modules, where DAC0/3 are 9-bit digital-to-analog converters, DAC1/4 are 6-bit digital-to-analog converters and DAC2 is an 8-bit digital-to-analog converter.

28.2 DAC0 Functional Block Diagram

Figure 28-1 DAC0 Functional Block Diagram



As shown in Figure 28-1, DAC0 converts 9-bit digital data into analog voltage and sends the voltage to CMP3 negative input of for bus over-current protection. Its analog output can also be configured to route to pin PB14.



Note:

DAC0 output has no current drive capability and can only carry capacitive load. To carry resistive load, operational amplifiers are used to follow the voltage output.

DAC0 operations are as follows:

1. Configure $PB\_AN[14] = 1$ and $PB\_OE[14] = 1$ to route the DAC0 output to pin PB14 (for DAC0 output testing only; not setting $PB\_OE[14]$ to 1 does not affect the internal DAC0 output).
2. Configure $VREF\_VHALF\_CR[VREFEN] = 1$ and $DAC\_CR[DAC0EN] = 1$. VREF is used as DAC0 reference voltage;

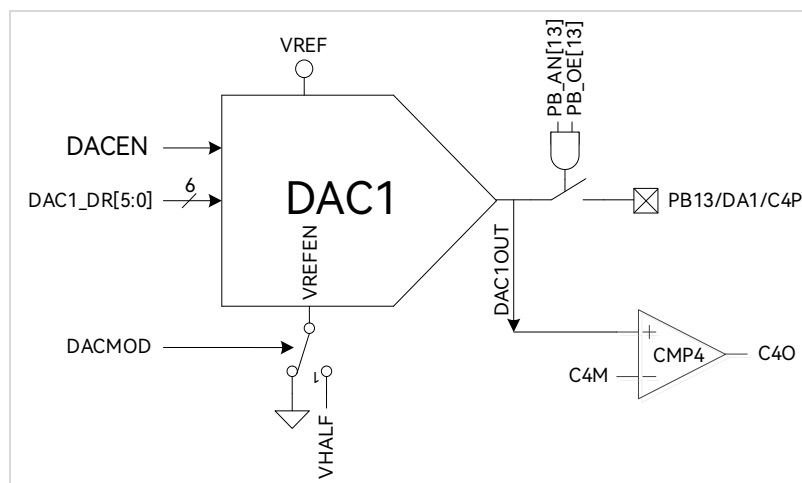
3. The range of output voltage is set by DAC_CR[DACMOD]. When DAC_CR[DACMOD] = 0, full-voltage output mode is active, and the range of output voltage is 0 ~ VREF. When DAC_CR[DACMOD] = 1, half-voltage output mode is active, the range of output voltage is VHALF ~ VREF. Output voltage of DAC0 under different configurations is shown in Table 28-1.

Table 28-1 Voltage Output of DAC0 under Different Configurations

DAC0_DR [8:0]	DAC0 Output Voltage (DAC_CR[DACMOD] = 0)	DAC0 Output Voltage (DAC_CR[DACMOD] = 1)
0x000	0	VHALF
0x100	VREF/2	(VREF - VHALF)/2 + VHALF
0x1FF	VREF*511/512	(VREF - VHALF)*511/512 + VHALF

28.3 DAC1 Functional Block Diagram

Figure 28-2 DAC1 Functional Block Diagram



As shown in Figure 28-2, DAC1 converts 6-bit digital data into analog voltage and sends the voltage to CMP4 positive input for cycle-by-cycle current limiting. This analog output can be configured to route to PB13.



Note:

DAC1 output has no current drive capability and can only carry capacitive load. To carry resistive load, operational amplifiers are used to follow the voltage output.

DAC1 operations are as follows:

1. Configure PB_AN[13] = 1 and PB_OE[13] = 1. DAC1 outputs the voltage to PB13 (this setting is for DAC1 output testing only. Setting PB_OE[13] to “0” does not affect internal output of DAC1

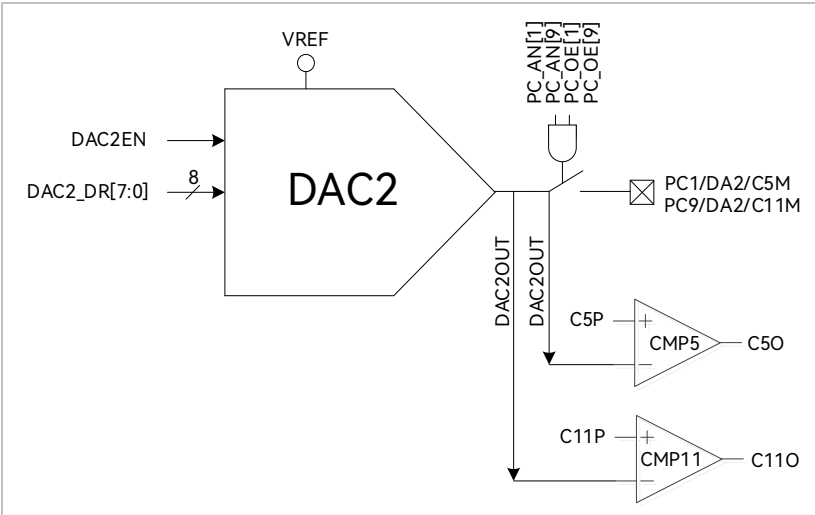
- circuit);
2. Configure $VREF\_VHALF\_CR[VREFEN] = 1$ and $DAC\_CR[DACEN] = 1$. $VREF$ is used as DAC1 reference voltage;
 3. The range of output voltage is set by $DAC\_CR[DACMOD]$. When $DAC\_CR[DACMOD] = 0$, full-voltage output mode is active, and the range of output voltage is $0 \sim VREF$. When $DAC\_CR[DACMOD] = 1$, half-voltage output mode is active, the range of output voltage is $VHALF \sim VREF$. Output voltage of DAC1 under different configurations is shown in Table 28-2.

Table 28-2 Voltage Output of DAC1 under Different Configurations

DAC1_DR[5:0]	DAC1 Output Voltage (DAC_CR[DACMOD] = 0)	DAC1 Output Voltage (DAC_CR[DACMOD] = 1)
0x00	0	VHALF
0x20	$VREF/2$	$(VREF - VHALF)/2 + VHALF$
0x3F	$VREF*63/64$	$(VREF - VHALF)*63/64 + VHALF$

28.4 DAC2 Functional Block Diagram

Figure 28-3 DAC2 Functional Block Diagram



As shown in Figure 28-3, DAC2 converts 8-bit digital data into analog voltage and sends the voltage to negative inputs of CMP5 and CMP11 for PFC over-current protection. These analog outputs can be configured to route to PC1 and PC9.



Note:

DAC2 output has no current drive capability and can only carry capacitive load. To carry resistive load, operational

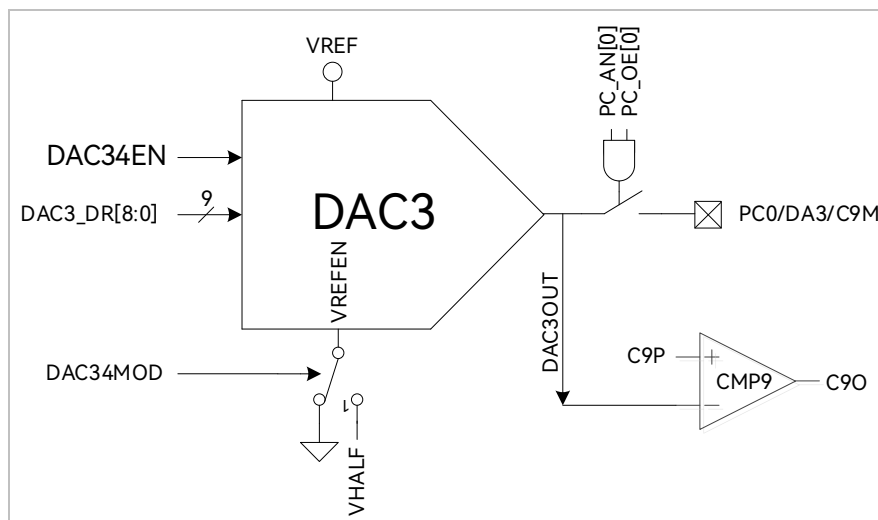
amplifiers are used to follow the voltage output.

DAC2 operations are as follows:

1. Configure PC_AN[1] = 1 and PC_OE[1] = 1. DAC2 outputs the voltage to PC1 (this setting is for DAC2 output testing only. Setting PC_OE[1] to “0” does not affect internal output of DAC2 circuit);
2. Configure PC_AN[9] = 1 and PC_OE[9] = 1. DAC2 outputs the voltage to PC9;
3. Configure VREF_VHALF_CR[VREFEN] = 1 and DAC_CR[DAC2EN] = 1. VDD5 is used as DAC2 reference voltage;
4. The range of output voltage is 0 ~ VREF

28.5 DAC3 Functional Block Diagram

Figure 28-4 DAC3 Functional Block Diagram



As shown in Figure 28-4, DAC3 converts 9-bit digital data into analog voltage and sends the voltage to CMP9 negative input for over-current protection after the sampled motor current is amplified. This analog output can be configured to route to PC0.



Note:

DAC3 output has no current drive capability and can only carry capacitive load. To carry resistive load, operational amplifiers are used to follow the voltage output.

DAC3 operations are as follows:

1. Configure PC_AN[0] = 1 and PC_OE[0] = 1. DAC3 outputs the voltage to PC0 (this setting is for

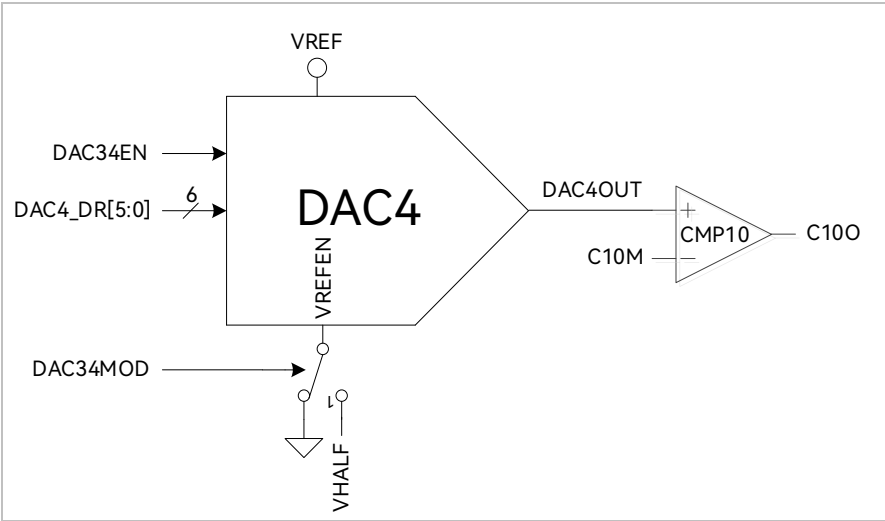
- DAC3 output testing only. Setting PC_OE[0] to “0” does not affect internal output of the DAC3 circuit);
- 2. Configure VREF_VHALF_CR[VREFEN] = 1 and DAC_CR[DAC34EN] = 1. VREF is used as DAC3 reference voltage;
 - 3. The range of output voltage is selected by DAC_CR[DAC34MOD]. When DAC_CR[DAC34MOD] = 0, full-voltage output mode is active, and the range of output voltage is 0 ~ VREF. When DAC_CR[DAC34MOD] = 1, half-voltage output mode is active, the range of output voltage is VHALF ~ VREF. Output voltage of DAC3 under different configurations is shown in Table 28-3.

Table 28-3 Voltage Output of DAC3 under Different Configurations

DAC3_DR [8:0]	DAC3 Output Voltage (DAC_CR[DAC34MOD] = 0)	DAC3 Output Voltage (DAC_CR[DAC34MOD] = 1)
0x000	0	VHALF
0x100	VREF/2	(VREF - VHALF)/2 + VHALF
0x1FF	VREF*511/512	(VREF - VHALF)*511/512 + VHALF

28.6 DAC4 Functional Block Diagram

Figure 28-5 DAC4 Functional Block Diagram



As shown in Figure 28-5, DAC4 converts 6-bit digital data into analog voltage and sends the voltage to CMP10 positive input for cycle-by-cycle current limiting.



Note:

DAC4 output has no current drive capability and can only carry capacitive load. To carry resistive load, operational amplifiers are used to follow the voltage output.

DAC4 operations are as follows:

- 1. Configure $VREF\_VHALF\_CR[VREFEN] = 1$ and $DAC\_CR[DAC34EN] = 1$. VREF is used as DAC4 reference voltage;
- 2. The range of output voltage is selected by $DAC\_CR[DAC34MOD]$. When $DAC\_CR[DAC34MOD] = 0$, full-voltage output mode is active, and the range of output voltage is $0 \sim VREF$. When $DAC\_CR[DAC34MOD] = 1$, half-voltage output mode is active, the range of output voltage is $VHALF \sim VREF$. Output voltage of DAC4 under different configurations is shown in Table 28-4.

Table 28-4 DAC4 Voltage Output under Different Configurations

DAC4_DR[5:0]	DAC4 Output Voltage (DAC_CR[DAC34MOD] = 0)	DAC4 Output Voltage (DAC_CR[DAC34MOD] = 1)
0x00	0	VHALF
0x20	VREF/2	(VREF - VHALF)/2 + VHALF
0x3F	VREF*63/64	(VREF - VHALF)*63/64 + VHALF

28.7 DAC Registers

28.7.1 DAC_CR (CSR: 0x640)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								DAC34MOD	DACMOD	RSV	DAC34EN	DAC2EN	DACEN		
																								rW	rW		rW	rW	rW		
																								0	0	1	0	0	0		
																								1	1	1	1	1	1		
																								1	1	1	1	1	1		

Bit	Name	Description
[31:6]	RSV	Reserved
[5]	DAC34MOD	DAC3/DAC4 Mode Setting 0: Full-voltage Output Mode 1: Half-voltage Output Mode

[4]	DACMOD	DAC0/DAC1 Mode Setting 0: Full-voltage Output Mode 1: Half-voltage Output Mode
[3]	RSV	Reserved
[2]	DAC34EN	DAC3/DAC4 Enable 0: Disable 1: Enable
[1]	DAC2EN	DAC2 Enable 0: Disable 1: Enable
[0]	DACEN	DAC0/DAC1 Enable 0: Disable 1: Enable

28.7.2 DAC0_DR (CSR: 0x641)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																							DAC0_DR									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW	RW	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:9]	RSV	Reserved
[8:0]	DAC0_DR	Date Input of DAC0 Controller

28.7.3 DAC1_DR (CSR: 0x642)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
RSV																								DAC1_DR									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0		

Bit	Name	Description
[31:6]	RSV	Reserved

[5:0]	DAC1_DR	Date Input of DAC1 Controller

28.7.4 DAC2_DR (CSR: 0x643)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								DAC2_DR							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	DAC2_DR	Date Input of DAC2 Controller

28.7.5 DAC3_DR (CSR: 0x644)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																							DAC3_DR									
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:9]	RSV	Reserved
[8:0]	DAC3_DR	Date Input of DAC3 Controller

28.7.6 DAC4_DR (CSR: 0x645)

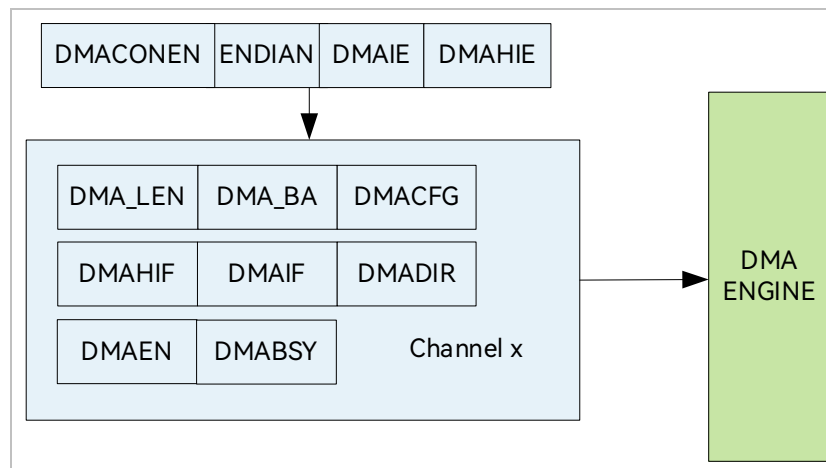
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																										DAC4_DR					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Bit	Name	Description
[31:6]	RSV	Reserved
[5:0]	DAC4_DR	Date Input of DAC4 Controller

29 DMA

29.1 DMA Instructions

Figure 29-1 Functional Block Diagram of DMA Module



The DMA module is a dual-channel DMA controller, which performs direct data transfer between peripherals (Timer5, SPI, UART, I²C, LIN, DataMonitor, etc.) and SRAM. DMA accessing to SRAM does not interfere with the normal CPU read/write operation to SRAM. The length of the transferred data and the start address of SRAM access is configurable. Data transfer mode is configurable and interrupt can be enabled.

29.2 DMA Features

- Six independent configurable channels in total
- Each channel is connected to a dedicated hardware DMA request line and supports software-triggered operations. All these functions are configured via software.
- Support circular buffer management
- Two events flags (DMA Half Transfer and DMA Transfer Complete) are logically ORed in a single interrupt request for each channel
- Support peripheral-to-memory and memory-to-peripheral transfers
- Programmable number of data transfers: up to 1024

29.3 DMA Instructions

29.3.1 DMA Configurations

1. Configure and enable the peripherals, and set associated input and output channels by `DMAx_CR[DMACFG]`;
2. Enable DMA interrupt, set transmission sequence, buffer length and SRAM source, and then configure `DMAx_CR[DMAEN]` and `DMAx_CR[DMABSY] = 1` to start DMA module;
3. When half of the bytes are transferred, an interrupt is generated if the interrupt flag bit `DMAx_CR[DMAHIF]` is set to “1” by hardware. This interrupt flag bit is cleared to “0” by software. At the end of the transfer, an interrupt is generated if the interrupt flag bit `DMAx_CR[DMAIF]` is set to “1” by hardware. This interrupt flag bit is cleared to “0” by software.
4. Configure `DMAx_CR[DMABSY] = 1` to start DMA again.

29.3.2 DMA Arbiter

The DMA arbiter manages SRAM access based on DMA channel numbers, with channel 0 having the highest priority while channel 5 the lowest.

In sending mode, if two or more channel requests are assigned with the same priority level, the arbiter first serves the channel where `DMAx_CR[DMABSY]` is set to “1”, and then others by channel numbers. In receiving mode, if `DMAx_CR[DMABSY] = 1` is programmed before a channel request arrives, the arbiter processes the data according to the channel numbers.

29.3.3 DMA Data Transfer

Each channel can implement DMA transfer between a peripheral register at a fixed address and a memory address. The amount of data to be transferred is programmable up to 1024. The register counter `DMAx_LEN` is incremented by 1 after each transmission.

29.3.3.1 Programmable Data Size

The data sizes of the peripheral and memory to be transferred are programmed by `DMAx_LEN` register.

This register can be written and read, but the data to be written or read is different. The data to be written

is the length of the data to be transferred and this value cannot be read. The data to be read is the amount of the data that has been transferred and this value can be read only.

29.3.3.2 Pointer Increment

Byte is the smallest unit of data that DMA module processes. The DMA pointer increment is 2 when the pointer is applied to a Timer module, and it is 1 when the pointer is applied to other modules.

29.3.3.3 Circular Mode

The circular mode is used to process continuous data flows. This feature is enabled by configuring $\text{DMAx\_CR}[\text{DMACONEN}] = 1$. In circular mode, the number of data to be transferred is automatically refreshed with the initial value programmed during channel configuration, and the DMA requests continued to be served.

29.3.3.4 Endianness

Endianness of the data, big-endian or little-endian, is configured by $\text{DMAx\_CR}[\text{ENDIAN}]$. In DataMonitor mode, little-endian is used.

29.4 DMA Registers

29.4.1 DMAx_CR (CSR: 0x0A0/0x0B0/0x0C0/0x0D0/0x0E0/0x0F0)

x refers to DMA channel number, where x = 0/1/2/3/4/5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																			DMAHIE	DMAIE	DMAONE	DMAEN	DMABSY	DMACFG				DMADIR	ENDIAN	DMAHIF	DMAIF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw1	rw	rw	rw	rw	rw	rw	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:13]	RSV	Reserved
[12]	DMAHIE	DMA Half Transfer Interrupt Enable 0: Disable 1: Enable

[11]	DMAIE	DMA Interrupt Enable 0: Disable 1: Enable
[10]	DMACONEN	Circular Mode 0: Disable 1: Enable
[9]	DMAEN	DMA Module Enable 0: Disable 1: Enable
[8]	DMABSY	DMA Channel Start/Busy Flag Read: 0: DMA channel is idle 1: DMA channel is busy Write: 0: No effect 1: DMA channel starts for data transfer
[7:4]	DMACFG	DMA Channel Peripherals and Transfer Direction Selection 0000: UART1 0001: UART2 0010: Reserved 0011: SPI1 0100: SPI2 0101: I ² C1 0110: I ² C2 0111: LIN 1000: T2DR 1001: T2ARR 1010: T5DR 1011: T5ARR 1100: CRC 1101: DataMonitor  Note: It cannot be configured when the DMA channel is busy.
[3]	DMADIR	DMA Direction Selection 0: From peripheral to RAM 1: From RAM to peripheral

[2]	ENDIAN	DMA Data Transfer Sequence 0: High bytes are received or sent first 1: Low bytes are received or sent first  Note: This bit works in 16-bit data mode, and shall be configured to “0” in 8-bit data mode. It cannot be configured when the DMA channel is busy.
[1]	DMAHIF	DMA Half Transfer Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: The interrupt is generated
[0]	DMAIF	DMA Interrupt Flag Read: 0: No interrupt pending 1: Interrupt pending Write: 0: This bit is cleared to “0” 1: The interrupt is generated

29.4.2 DMAx_LEN (CSR: 0x0A1/0x0B1/0x0C1/0x0D1/0x0E1/0x0F1)

x refers to DMA channel number, where x = 0/1/2/3/4/5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RSV																						DMA_LEN															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0						

Bit	Name	Description
[31:10]	RSV	Reserved
[9:0]	DMA_LEN	Transfer Length of DMA Channel Read: The number of the byte that is currently transferred by DMA Channel (0 denotes the first byte) Write: SRAM data transfer length of DMA channel

		Note: It cannot be configured when the DMA channel is busy. When DMAx_CR [ENDIAN] = 1 (low bytes are received or transmitted first), it is recommended that DMAx_LEN be set to an odd number.

29.4.3 DMAx_BA (CSR: 0x0A2/0x0B2/0x0C2/0x0D2/0x0E2/0x0F2)

x refers to DMA channel number, where x = 0/1/2/3/4/5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA_BA																															
																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

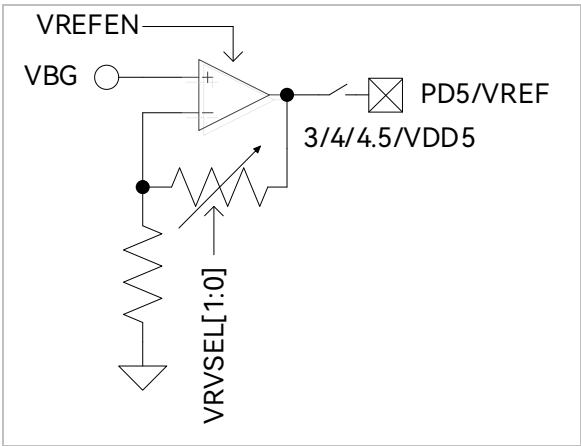
Bit	Name	Description
[31:0]	DMA_BA	Start Address of Data Transfer by DMA Channel It cannot be configured when the DMA channel is busy. Note: SRAM address space for data transfer by DMA channel: DMAx_BA[13:0] ~ (DMAx_BA[13:0] + DMAx_LEN[9:0])

	Note: When I²C is selected as DMA channel peripherals (including from I²C to SRAM and from SRAM to I²C) , START + Address interrupt of I²C communication still requires to be cleared to “0” by MCU software. In I²C slave mode, if STOP is received, I2Cx_SR[I2CSTP] = 0 is configured to clear I²C interrupt and restart the DMA transfer.

30 VREF

30.1 VREF Instructions

Figure 30-1 I/O Pins of VREF Module



The inputs and outputs of the VREF module are shown in Figure 30-1. VREF module generates an internal voltage reference for ADC and DAC modules. VBG is the voltage supplied by the chip internally.

VREF is enabled when VREF_VHALF_CR[VREFEN] is set to “1”. The output voltage is selected by configuring VREF_VHALF_CR[VREFVSEL]. When PD_AN[5] = 1 and PD_OE[5] = 1, VREF is output to PD5, which is connected with a 1μF external capacitor.

30.2 VREF Register

30.2.1 VREF_VHALF_CR (CSR: 0x620)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																						VHALFSEL1	VHALFSEL0	VRVSEL1	VRVSEL0	RSV	VREFEN	RSV				VHALFEN
																						rw	rw	rw	rw	-	rw	-	-	-	-	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	0	0	-	0	-	-	-	0	

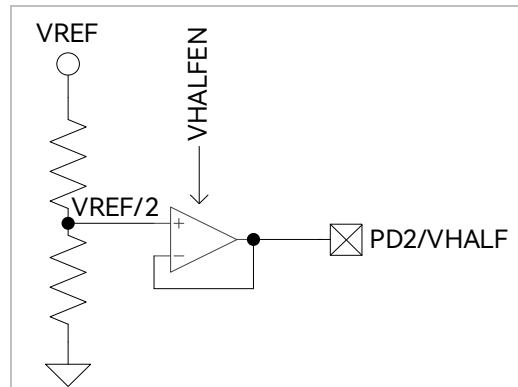
Bit	Name	Description

[31:10]	RSV	Reserved
[9]	VHALFSEL1	VHALF Voltage Selection (VREF Coefficient 1) 00: 1/8 01: 1/4 10: 25/64 11: 1/2 (Default)
[8]	VHALFSEL0	VHALF Voltage Selection (VREF Coefficient 0) 00: 1/8 01: 1/4 10: 25/64 11: 1/2 (Default)
[7]	VRVSEL1	VREF Voltage 1 00: 4.5V 01: 5V 10: 3V 11: 4V
[6]	VRVSEL0	VREF Voltage 0 00: 4.5V 01: 5V 10: 3V 11: 4V
[5]	RSV	Reserved
[4]	VREFEN	VREF Module Enable 0: Disable 1: Enable
[3:1]	RSV	Reserved
[0]	VHALFEN	VHALF Module Enable 0: Disable 1: Enable

31 VHALF

31.1 VHALF Instructions

Figure 31-1 I/O Pins of VREF Module



The inputs and outputs of the VHALF module are shown in Figure 31-1. VHALF module generates the voltage reference 00: $VREF/8$, 01: $VREF/4$, 10: $VREF \cdot 25/64$ or 11: $VREF/2$ (default), which is configured by `VREF_VHALF_CR[VHALFSEL]`.

VHALF is enabled when `VREF_VHALF_CR[VHALFEN]` is set to “1”. The voltage is output to PD2, which is connected with a $1\mu F$ external capacitor.

31.2 VHALF Register

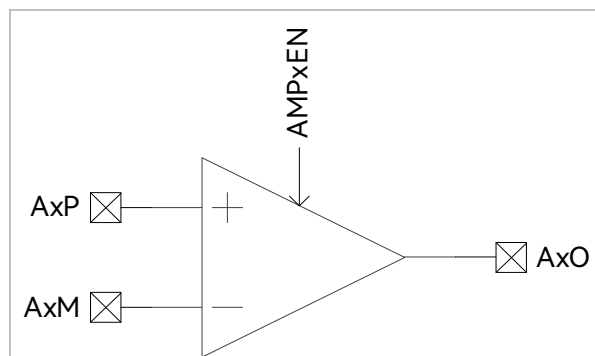
See section 30.2.1.

32 Operational Amplifiers

32.1 Introduction

The chip integrates 7 high-speed independent operational amplifiers (AMP0 ~ AMP6). Each operational amplifier has a separate enable bit, and can be configured as a PGA.

Figure 32-1 Schematic Diagram of Operational Amplifier Module

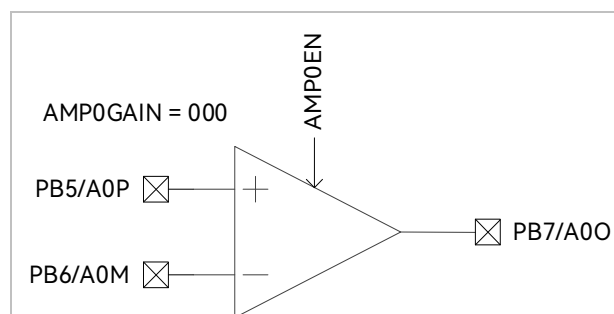


32.2 Operational Amplifier Instructions

32.2.1 Bus Current Sampling Operational Amplifier (AMP0)

32.2.1.1 AMP0 Normal Mode

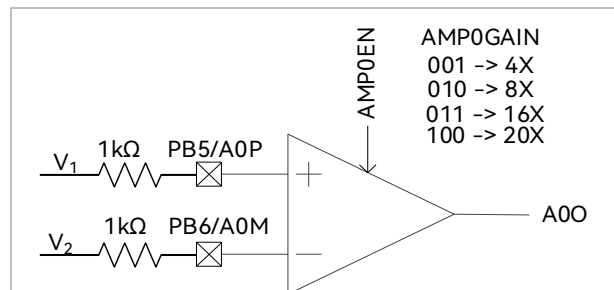
Figure 32-2 AMP0 in Normal Mode



The I/O pins of AMP0 are shown in Figure 32-2. AMP0 is enabled when $\text{AMP\_CR0}[\text{AMP0EN}] = 1$, and PB5, PB6 and PB7 are automatically configured to analog mode by hardware, that is, $\text{PB\_AN}[7:5]$ is set to 111 automatically.

32.2.1.2 AMP0 PGA Differential Input Mode

Figure 32-3 AMP0 in PGA Differential Input Mode



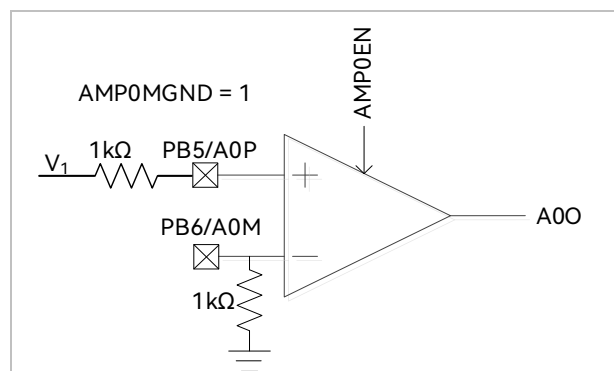
As shown in Figure 32-3, positive and negative inputs of AMP0 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by AMP_CR1[AMP0GAIN], and AMP0 is enabled when AMP_CR0[AMP0EN] =

1. The relation between output and input of the operational amplifier: $V_{out} = V_{HALF} + (V_1 - V_2) * AMP0GAIN$.

32.2.1.3 AMP0 PGA Single-ended Input Mode

Figure 32-4 AMP0 in PGA Single-ended Input Mode



As shown in Figure 32-4, positive input of AMP0 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMP0GAIN]. Configuring AMP_CR0[AMP0MGND] = 1 connects the negative input to GND, and setting AMP_CR0[AMP0EN] = 1 enables AMP0. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMP0GAIN$.



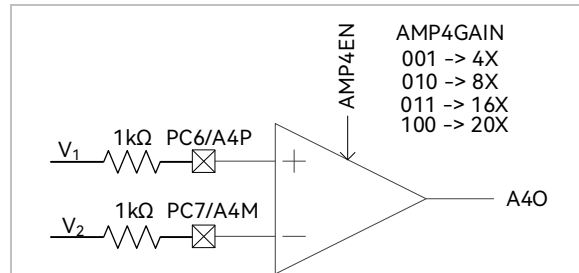
Note:

When the negative input of AMP0 is connected to GND, PB6 cannot be used as an I/O pin.

32.2.2 Bus Current Sampling Operational Amplifier (AMP4)

32.2.2.1 AMP4 PGA Differential Input Mode

Figure 32-5 AMP4 in PGA Differential Input Mode

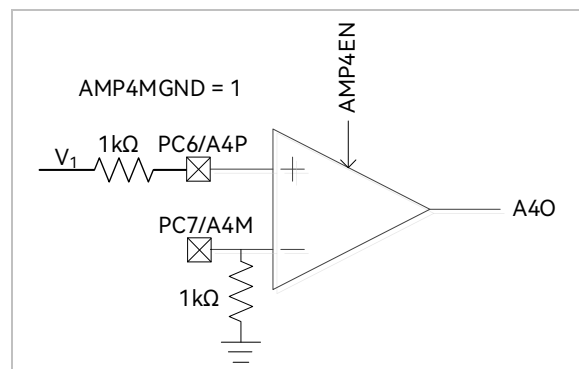


As shown in Figure 32-5, positive and negative inputs of AMP4 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by AMP_CR1[AMP4GAIN], and AMP4 is enabled when AMP_CR0[AMP4EN] = 1. The relation between output and input of the operational amplifier: $V_{out} = V_{HALF} + (V1 - V2) * AMP4GAIN$.

32.2.2.2 AMP4 PGA Single-ended Input Mode

Figure 32-6 AMP4 in PGA Single-ended Input Mode



As shown in Figure 32-6, positive input of AMP4 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMP4GAIN]. Configuring AMP_CR0[AMP4MGND] = 1 connects the negative input to GND, and setting AMP_CR0[AMP4EN] = 1 enables AMP4. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMP4GAIN$.



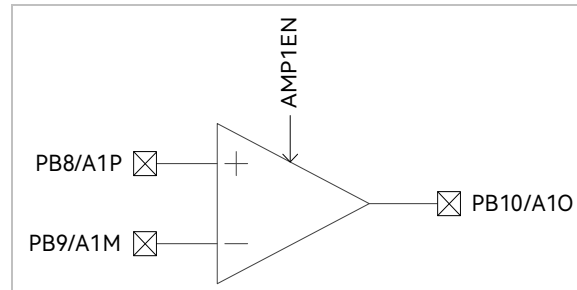
Note:

When the negative input of AMP4 is connected to GND, PC7 cannot be used as an I/O pin.

32.2.3 Phase Current Operational Amplifier (AMP1)

32.2.3.1 AMP1 Normal Mode

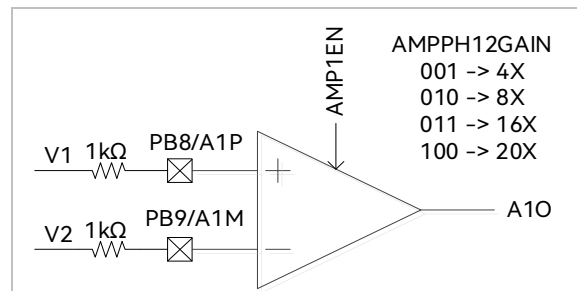
Figure 32-7 AMP1 in Normal Mode



The I/O pins of AMP1 are shown in Figure 32-7. AMP1 is enabled when $\text{AMP\_CR0}[\text{AMP1EN}] = 1$. PB8, PB9 and PB10 are automatically configured to analog mode by hardware, that is, $\text{PB\_AN}[10:8]$ is set to 111 automatically.

32.2.3.2 AMP1 PGA Differential Input Mode

Figure 32-8 AMP1 in PGA Differential Input Mode

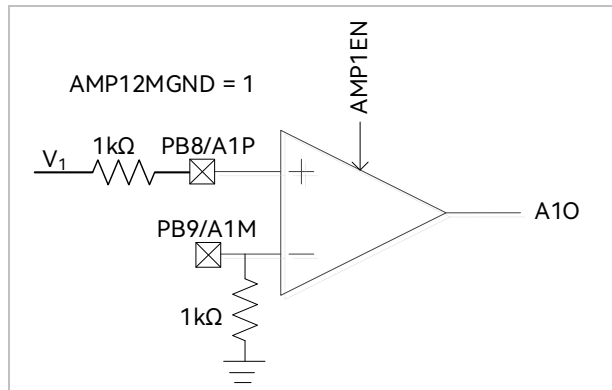


As shown in Figure 32-8, positive and negative inputs of AMP1 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by $\text{AMP\_CR1}[\text{AMPPH12GAIN}]$, and AMP1 is enabled when $\text{AMP\_CR0}[\text{AMP1EN}] = 1$. The relation between output and input of the operational amplifier: $V_{\text{out}} = V_{\text{HALF}} + (V_1 - V_2) * \text{AMPPH12GAIN}$.

32.2.3.3 AMP1 PGA Single-ended Input Mode

Figure 32-9 AMP1 in PGA Single-ended Input Mode



As shown in Figure 32-9, positive input of AMP1 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMPPH12GAIN]. Configuring AMP_CR0[AMP12MGND] = 1 connects the negative input to GND, and setting AMP_CR0[AMP1EN] = 1 enables AMP1. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMPPH12GAIN$.



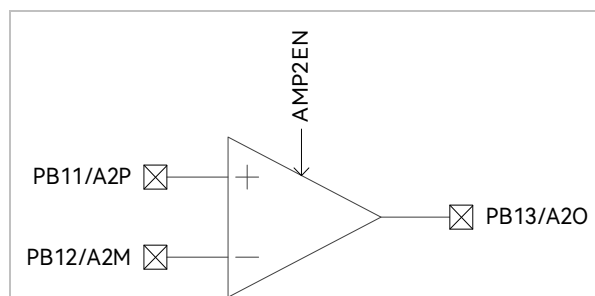
Note:

When the negative input of AMP1 is connected to GND, PB9 cannot be used as an I/O pin.

32.2.4 Phase Current Operational Amplifier (AMP2)

32.2.4.1 AMP2 Normal Mode

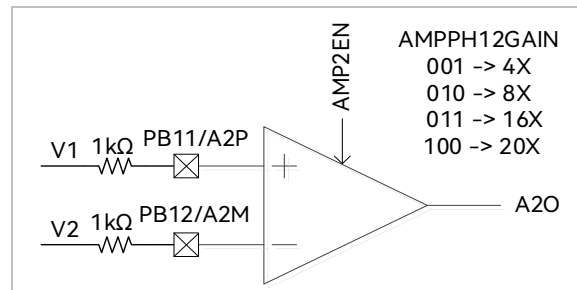
Figure 32-10 AMP2 in Normal Mode



The I/O pins of AMP2 are shown in Figure 32-10. AMP2 is enabled when AMP_CR0[AMP2EN] = 1. PB11, PB12 and PB13 are automatically configured to analog mode by hardware, that is, PB_AN[13:11] is set to 111 automatically.

32.2.4.2 AMP2 PGA Differential Input Mode

Figure 32-11 AMP2 in PGA Differential Input Mode

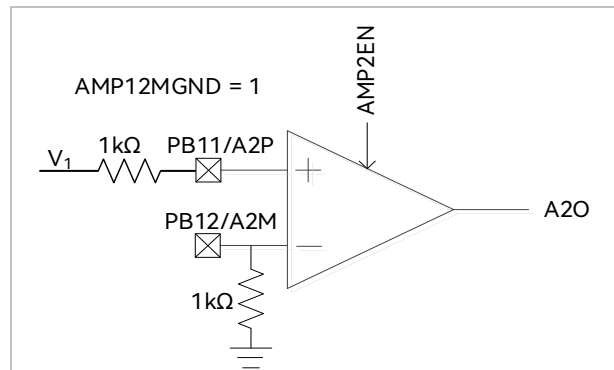


As shown in Figure 32-11, positive and negative inputs of AMP2 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by AMP_CR1[AMPPH12GAIN], and AMP2 is enabled when AMP_CR0[AMP2EN] = 1. The relation between output and input of the operational amplifier: $V_{out} = V_{HALF} + (V1 - V2) * AMPPH12GAIN$.

32.2.4.3 AMP2 PGA Single-ended Input Mode

Figure 32-12 AMP2 in PGA Single-ended Input Mode



As shown in Figure 32-12, positive input of AMP2 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMPPH12GAIN]. Configuring AMP_CR0[AMP12MGND] = 1 connects the negative input to GND, and setting AMP_CR[AMP2EN] = 1 enables AMP2. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMPPH12GAIN$.



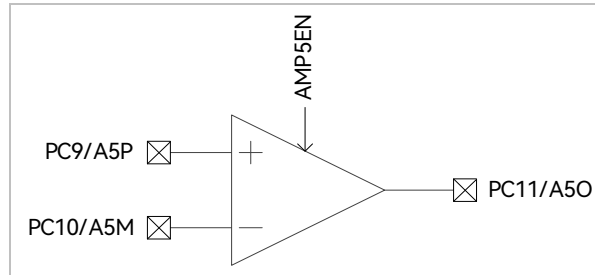
Note:

When the negative input of AMP2 is connected to GND, PB12 cannot be used as an I/O pin.

32.2.5 Phase Current Operational Amplifier (AMP5)

32.2.5.1 AMP5 Normal Mode

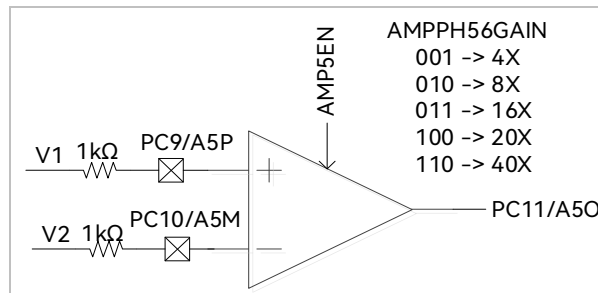
Figure 32-13 AMP5 in Normal Mode



The I/O pins of AMP5 are shown in Figure 32-13. AMP5 is enabled when $\text{AMP\_CR0}[\text{AMP5EN}] = 1$. The three associated pins (PC9, PC10, and PC11) are configured to analog mode by hardware, that is, $\text{PC\_AN}[11:9]$ is set to 111 automatically.

32.2.5.2 AMP5 PGA Differential Input Mode

Figure 32-14 AMP5 in PGA Differential Input Mode

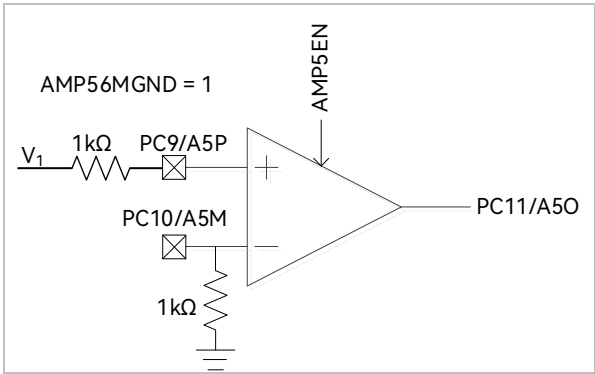


As shown in Figure 32-14, positive and negative inputs of AMP5 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by $\text{AMP\_CR1}[\text{AMPPH56GAIN}]$. AMP5 is enabled when $\text{AMP\_CR0}[\text{AMP5EN}] = 1$. The relation between output and input of the operational amplifier: $V_{\text{out}} = V_{\text{HALF}} + (V_1 - V_2) * \text{AMPPH56GAIN}$.

32.2.5.3 AMP5 PGA Single-ended Input Mode

Figure 32-15 AMP5 in PGA Single-ended Input Mode



As shown in

Figure 32-15, positive input of AMP5 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMPPH56GAIN]. Configuring AMP_CR0[AMP56MGND] = 1 connects the negative input to GND, and setting AMP_CR0[AMP5EN] = 1 enables AMP5. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMPPH56GAIN$.



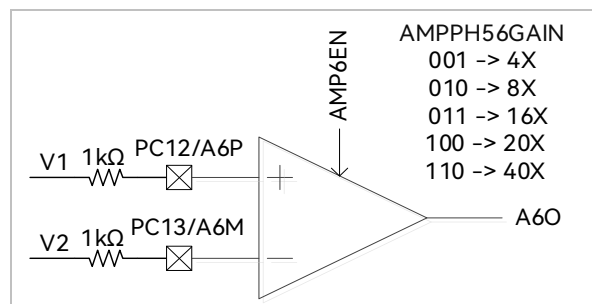
Note:

When the negative input of AMP5 is connected to GND, PC10 cannot be used as an I/O pin.

32.2.6 Phase Current Operational Amplifier (AMP6)

32.2.6.1 AMP6 PGA Differential Input Mode

Figure 32-16 AMP6 in PGA Differential Input Mode

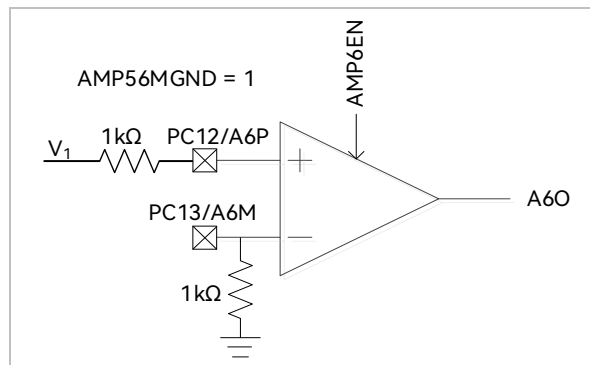


As shown in Figure 32-16, positive and negative inputs of AMP6 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by AMP_CR1[AMPPH56GAIN]. AMP6 is enabled when AMP_CR0[AMP6EN] = 1. The relation between output and input of the operational amplifier: $V_{out} = V_{HALF} + (V_1 - V_2) * AMPPH56GAIN$.

32.2.6.2 AMP6 PGA Single-ended Input Mode

Figure 32-17 AMP6 in PGA Single-ended Input Mode



As shown in Figure 32-17, positive input of AMP6 is connected in series with a 1kΩ resistor in the external circuit, and negative input is connected to the ground through a 1kΩ resistor inside the MCU.

In this mode, the gain is set by AMP_CR1[AMPPH56GAIN]. Configuring AMP_CR0[AMP56MGND] = 1 connects the negative input to GND, and setting AMP_CR0[AMP6EN] = 1 enables AMP6. The relation between output and input of operational amplifier: $V_{out} = V_{HALF} + V1 * AMPPH56GAIN$.



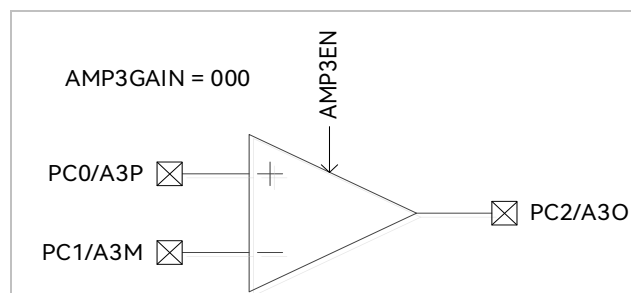
Note:

When the negative input of AMP6 is connected to GND, PC13 cannot be used as an I/O pin.

32.2.7 Operational Amplifier AMP3

32.2.7.1 AMP3 Normal Mode

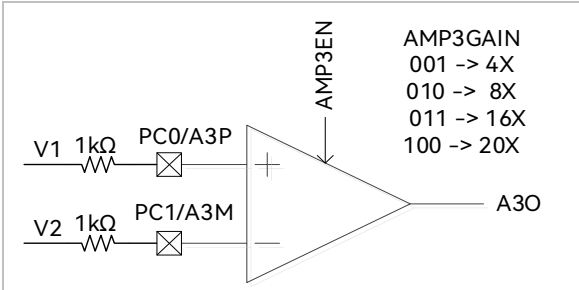
Figure 32-18 AMP3 in Normal Mode



The I/O pins of AMP3 are shown in Figure 32-18. AMP3 is enabled when AMP_CR0[AMP3EN] = 1 and PC0, PC1 and PC2 are automatically configured to analog mode by hardware, that is, PC_AN[2:0] is set to 111 automatically.

32.2.7.2 AMP3 PGA Differential Input Mode

Figure 32-19 AMP3 in PGA Differential Input Mode



As shown in Figure 32-19, positive and negative inputs of AMP3 are connected with a 1kΩ resistor in the external circuit respectively.

In this mode, the gain is set by AMP_CR1[AMP3GAIN], and AMP3 is enabled when AMP_CR0[AMP3EN] =

1. The relation between output and input of the operational amplifier: $V_{out} = V_{HALF} + (V1 - V2) * AMP3GAIN$.

32.3 Operational Amplifier Registers

32.3.1 AMP_CR0 (CSR: 0x621)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		CP1EN	CP0SEL	CP0EN	AMP56MGND	AMP4MGND	AMP12MGND	AMP0MGND	AMP6EN	AMP5EN	AMP4EN	AMP3EN	AMP2EN	AMP1EN	AMP0EN
																		r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
																		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13]	CP1EN	AMP4 Constant Power Enable 0: Disable 1: Enable
[12]	CP0SEL	AMP0 Average Current Sampling Channel Selection This configuration takes effect only when AMP_CR0[CP0EN] = 1. 0: Sample average current from AD1 channel 10 (PB15). 1: Sample average current from AD1 channel 12 (PD6).

**Note:**

AMP0 output (PB7) is routed to PB15 or PD6 via an internal 16 kΩ resistor. A 1 μF external capacitor shall be connected to PB15 or PD6 for the current sampling.

[11]	CP0EN	AMP0 Constant Power Enable 0: Disable 1: Enable
[10]	AMP56MGND	AMP5&6 Negative Input Wired to GND 0: Disable 1: Enable
[9]	AMP4MGND	AMP4 Negative Input Wired to GND 0: Disable 1: Enable
[8]	AMP12MGND	AMP1&2 Negative Input Wired to GND 0: Disable 1: Enable
[7]	AMP0MGND	AMP0 Negative Input Wired to GND 0: Disable 1: Enable
[6]	AMP6EN	AMP6 Enable 0: Disable 1: Enable
[5]	AMP5EN	AMP5 Enable 0: Disable 1: Enable
[4]	AMP4EN	AMP4 Enable 0: Disable 1: Enable
[3]	AMP3EN	AMP3 Enable 0: Disable 1: Enable
[2]	AMP2EN	AMP2 Enable 0: Disable 1: Enable
[1]	AMP1EN	AMP1 Enable 0: Disable 1: Enable
[0]	AMP0EN	AMP0 Enable

		0: Disable 1: Enable

32.3.2 AMP_CR1 (CSR: 0x622)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																	AMPPH56GAIN			AMPPH12GAIN			AMP4GAIN			AMP3GAIN			AMP0GAIN		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:15]	RSV	Reserved
[14:12]	AMPPH56GAIN	AMP5/AMP6 Amplification Gain Settings 000: The gain is configured by external circuit 001: 4x 010: 8x 011: 16x 100: 20x 101: Reserved 110: 40x 111: Reserved
[11:9]	AMPPH12GAIN	AMP1/AMP2 Amplification Gain Settings 000: The gain is configured by external circuit 001: 4x 010: 8x 011: 16x 100: 20x 101: Reserved 110: Reserved 111: Reserved
[8:6]	AMP4GAIN	AMP4 Amplification Gain Settings 000: The gain is configured by external circuit 001: 4x 010: 8x 011: 16x 100: 20x 101: Reserved

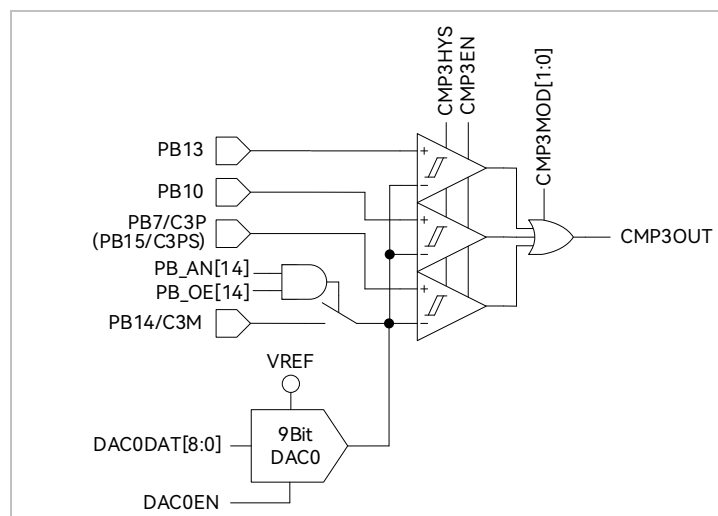
		110: Reserved 111: Reserved
[5:3]	AMP3GAIN	AMP3 Amplification Gain Settings 000: The gain is configured by external circuit 001: 4x 010: 8x 011: 16x 100: 20x 101: Reserved 110: Reserved 111: Reserved
[2:0]	AMP0GAIN	AMP0 Amplification Gain Settings 000: The gain is configured by external circuit 001: 4x 010: 8x 011: 16x 100: 20x 101: Reserved 110: Reserved 111: Reserved

33 Comparators

33.1 Comparator Operations

33.1.1 CMP3

Figure 33-1 CMP3 I/O Pins



The I/O pins of CMP3 are shown in Figure 33-1.

CMP3 configurations are as follows:

1. The negative input reference voltage can be supplied from an external circuit or from the internal DAC0 output;
 - To use an external input, set PB_AN[14] = 1 and PB_OE[14] = 1 to route the CMP3 negative input to pin PB14.
 - To use the DAC0 output, enable DAC0 by setting DAC_CR[DACEN] = 1, then program the desired DAC0 code value.
 - Optionally, while DAC0 is enabled, you may also set PB_AN[14] = 1 and PB_OE[14] = 1. In this case, connect an external capacitor (100 pF recommended) between PB14 and ground, and allow sufficient time for the DAC0 output to stabilize.
2. Configure CMP_CR1[CMP3MOD] to select single-comparator input, dual-comparator input or triple-comparator input mode;

- When `CMP_CR1[CMP3MOD] = 00`, CMP3 works in single-comparator input mode. The connection diagram is shown in Figure 33-2;
- When `CMP_CR1[CMP3MOD] = 01`, CMP3 works in dual-comparator input mode. The connection diagram is shown in Figure 33-3;
- When `CMP_CR1[CMP3MOD] = 1x`, CMP3 works in triple-comparator input mode. The connection diagram is shown in

> Figure 33-4;

3. Configure CMP_CR1[CMP3HYS] to enable or disable hysteresis;
4. Configure CMP_CR1[CMP3EN] = 1 to enable CMP3.

Figure 33-2 Single-comparator Input Mode

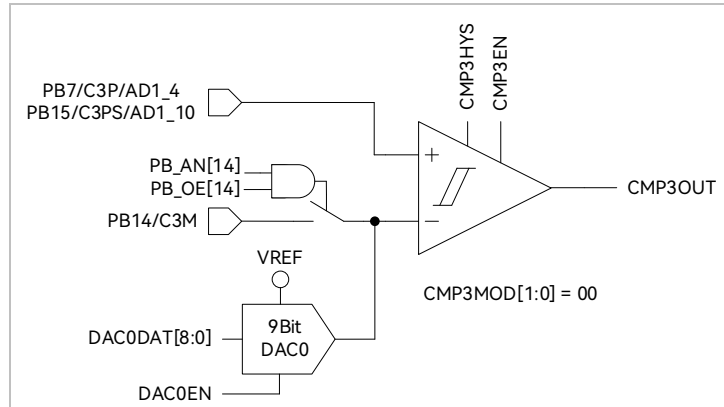


Figure 33-3 Dual-comparator Input Mode

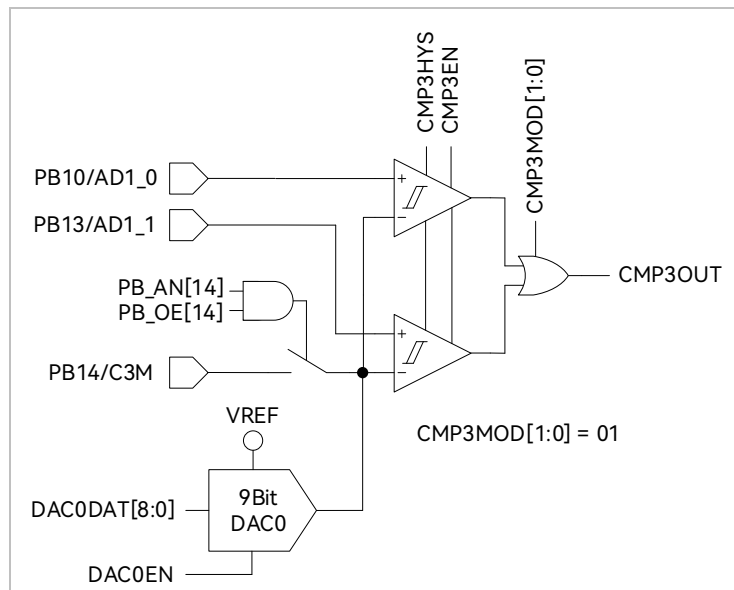
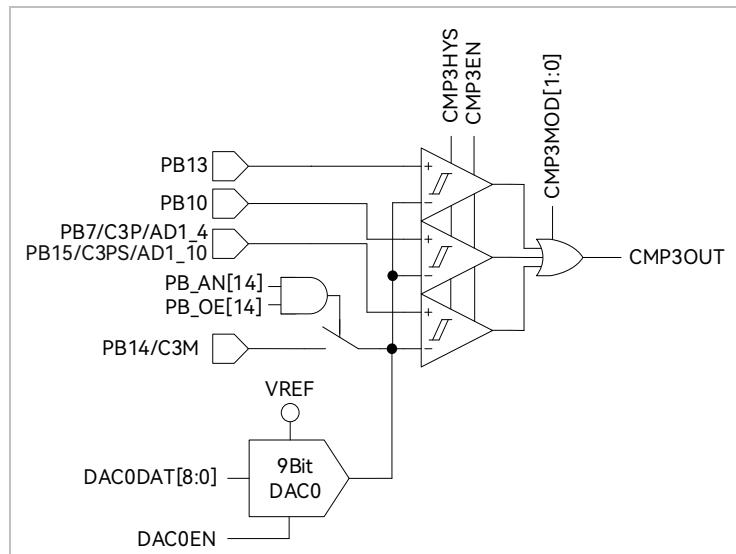


Figure 33-4 Triple-comparator Input Mode



33.1.1.1 Over-current Protection (OCP) of Master Motor

When an over-current protection signal is generated, DRV1_OUT[MOE] is automatically cleared to output idle voltage to stop master motor for chip and motor protection. OCP feature is enabled when DRV1_CR[MOEMD] = 01, which automatically turns off the output and generates an OCP interrupt request if the current exceeds the threshold. When DRV1_CR[MOEMD] = 00, the output is not automatically turned off if the current exceeds the threshold. However, an OCP request is generated by the hardware.

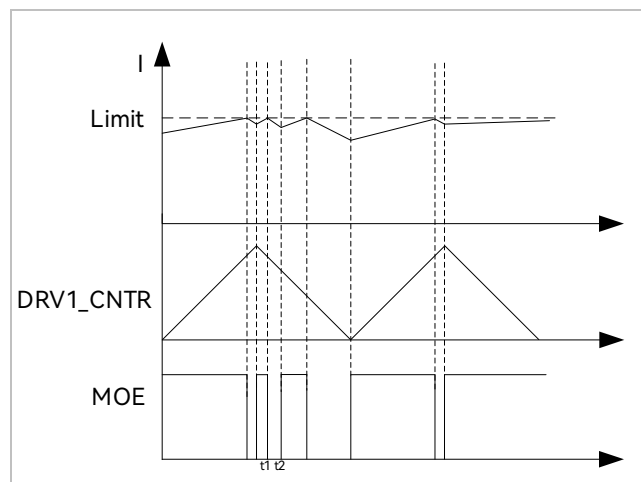
The source of OCP interrupt is selected by configuring DRV1_CR[MOEMD] $\neq$ 00 and DRV1_CR[OCP_MOEMD] = 01, namely CMP3 interrupt. When CMP_CR0[CMP3IM] = 01, the OCP output is generated on the raising edge of CMP3. At this time, the source of OCP interrupt is CMP3. In triple-shunt current sampling mode, CMP_CR1[CMP3MOD] is configured to select triple-comparator input mode. When the current of any phase is over the threshold, CMP3 generates an OCP signal. For other sampling modes, CMP_CR1[CMP3MOD] is configured to choose single-comparator input mode. When the bus current is over the threshold, CMP3 generates an OCP signal.

Configuring CMP_CR3[CMP3FSEL] enables the filtering of interrupt signals for OCP and programming CMP_CR3[CMP3FSEL] = 01/10/11 selects filter width of 4/8/16 clock cycles. When the filtering feature is enabled, the filtered signal is delayed by 4/8/16 clock cycles compared to the signal before filtering.

33.1.1.2 Cycle-by-cycle Current Limiting of Master Motor

When an OCP event occurs, DRV1_OUT[MOE] is set to “1” by hardware after it has been cleared to “0” for a period of time, so that the motor drive is automatically restored. When CMP_CR0[**CMP3IM**] = 11, DRV1_OUT[MOE] is cleared to “0” on the rising edge of CMP3OUT to protect the motor. When DRV1_CR[**MOEMD**] = 10, the outputs are automatically turned off upon an OCP interrupt. DRV1_OUT[MOE] is enabled automatically upon driver counter overflow/underflow event or after 10μs to restore motor drive. When DRV1_CR[**MOEMD**] = 11, the outputs are automatically turned off upon an OCP interrupt. DRV1_OUT[MOE] is enabled automatically upon driver counter overflow/underflow event or after 5μs to restore motor drive.

Figure 33-5 Cycle-by-cycle Current Limiting Waveform ($t_2 - t_1 = 10\mu\text{s}$)
when DRV1_CR[MOEMD] = 10



33.1.2 CMP9

CMP9 supports single-comparator input mode only, and its configurations are as follows:

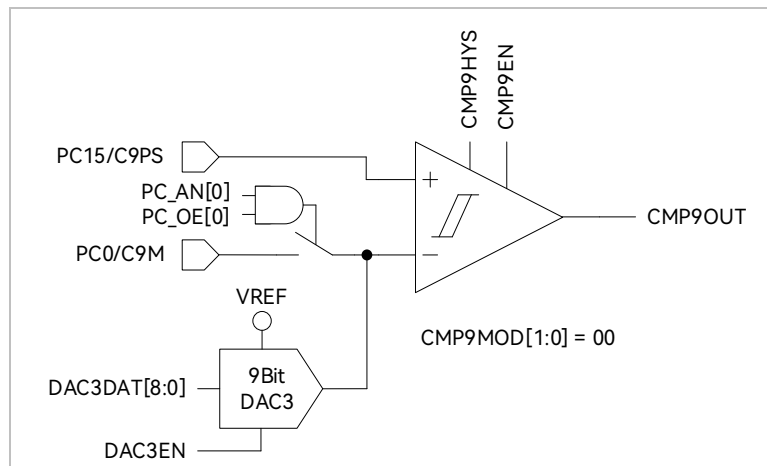
1. Select the reference voltage for the negative input of CMP9. The voltage source can be on-chip DAC3 output or external circuit input;
 - For the external circuit input, configure PC_AN[0] = 1 and PC_OE[0] = 1 to apply the external voltage via PC0 as the reference voltage for the negative input of CMP9;
 - For DAC3 output, configure DAC_CR[**DAC34EN**] = 1 to enable DAC3, then set the corresponding DAC3 code value to apply its output as the reference voltage for the negative input of CMP9;

- When DAC3 is enabled, you can also configure PC_AN[0] = 1 and PC_OE[0] = 1, and connect a 100pF external capacitor (recommended) between PC0 and GND. This helps stabilize DAC3 output voltage over time;

Configure CMP_CR5[CMP9MOD] = 00 to select CMP9 as single-comparator input mode; the corresponding I/O pins are shown in Figure 33-6;

2. Configure CMP_CR5[CMP9HYS] to enable or disable hysteresis;
3. Configure CMP_CR5[CMP9EN] = 1 to enable CMP9.

Figure 33-6 Single-comparator Input Mode



33.1.2.1 Over-current Protection (OCP) of Slave Motor

When an over-current protection signal is generated, DRV2_OUT[MOE] is automatically cleared to output idle voltage to stop motor drive for chip and motor protection. OCP feature is enabled when DRV2_CR[MOEMD] = 01, which automatically turns off the output and generates an OCP interrupt request if the current exceeds the threshold. When DRV2_CR[MOEMD] = 00, the output is not automatically turned off if the current exceeds the threshold. However, an OCP request is generated by the hardware.

The source of OCP interrupt is selected by configuring DRV2_CR[MOEMD] ≠ 00, and DRV2_CR[OCP_MOEMD] = 1, namely CMP9 interrupt. When CMP_CR4[CMP9IM] = 01, the OCP output is generated on the raising edge of CMP9. At this time, the source of OCP interrupt is CMP9. In triple-shunt current sampling mode, CMP_CR5[CMP9MOD] is configured to select triple-comparator input mode. When the current of any phase is over the threshold, CMP9 generates an OCP signal. For other sampling modes,

CMP_CR5[CMP9MOD] is configured to choose single-comparator input mode. When the bus current is over the threshold, CMP9 generates an OCP signal.

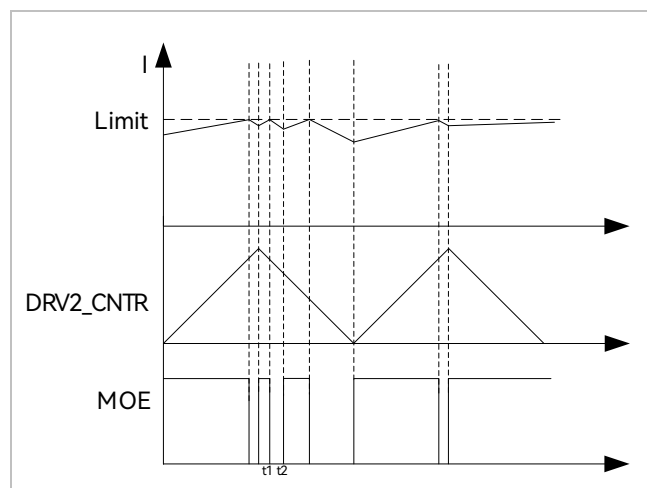
Configuring CMP_CR3[CMP9FSEL] enables the filtering of interrupt signals for OCP, and programming CMP_CR3[CMP9FSEL]= 01/10/11 selects filter width of 4/8/16 clock cycles. When the filtering feature is enabled, the filtered signal is delayed by 4/8/16 clock cycles compared to the signal before filtering.

33.1.2.2 Cycle-by-cycle Current Limiting of Slave Motor

When an OCP event occurs, DRV2_OUT[MOE] is set to “1” by hardware after it has been cleared to “0” for a period of time, so that the motor drive is automatically restored. When CMP_CR4[CMP9IM] = 11, DRV2_OUT[MOE] is cleared to “0” on the rising edge of CMP3OUT to protect the motor. When DRV2_CR[MOEMD] = 10, the outputs are automatically turned off upon an OCP interrupt. DRV2_OUT[MOE] is enabled automatically upon driver counter overflow/underflow events or after 10 μ s to restore motor drive. When DRV2_CR[MOEMD] = 11, the outputs are automatically turned off upon an OCP interrupt. DRV2_OUT[MOE] is enabled automatically upon driver counter overflow/underflow events or after 5 μ s to restore motor drive.

Figure 33-7 Cycle-by-cycle Current Limiting Waveform ($t_2 - t_1 = 10\mu$ s)

when DRV2_CR[MOEMD] = 10



33.1.3 CMP4

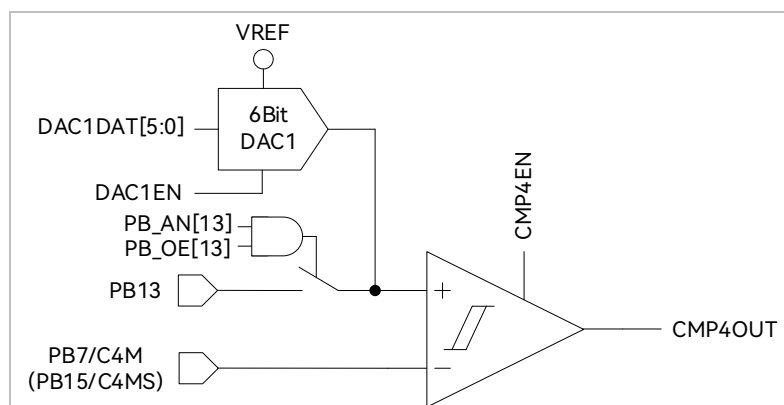
The I/O pins of CMP4 are shown in Figure 33-8. CMP4OUT can be read by software or reversed on the external interrupt EXTI0. When CMP3 is used for cycle-by-cycle current limiting protection, CMP4 is used for bus over-current protection. When bus current OCP feature of CMP4 is triggered, the output must be

turned off by software.

CMP4 configurations are as follows:

1. Select the reference voltage for the positive input of CMP4. The voltage source can be on-chip DAC1 output or external circuit input;
 - For the external circuit input, configure $PB\_AN[13] = 1$ and $PB\_OE[13] = 1$ to apply the external voltage via PB13 as the reference voltage for the positive input of CMP4;
 - For DAC1 output, configure $DAC\_CR[DACEN] = 1$ to enable DAC1, then set the corresponding DAC1 code value to apply its output as the reference voltage for the positive input of CMP4;
 - When DAC1 is enabled, you can also configure $PB\_AN[13] = 1$ and $PB\_OE[13] = 1$, and connect a 100pF external capacitor (recommended) between PB13 and GND. This helps stabilize DAC1 output voltage over time;
2. Configure $PB\_AN[7] = 1$ to assign PB7 to analog signal (PB7's functions can be assigned to PB15);
3. Configure $CMP\_CR1[CMP4EN] = 1$ to enable CMP4;
4. Configure $CMP\_IFR[CMP4IF] = 0$ to clear the interrupt flag bit of CMP4;
5. Configure $CMP\_CR0[CMP4IM] = 10$ to select falling edge to trigger CMP4 interrupt.

Figure 33-8 CMP4 I/O Pins



33.1.4 CMP10

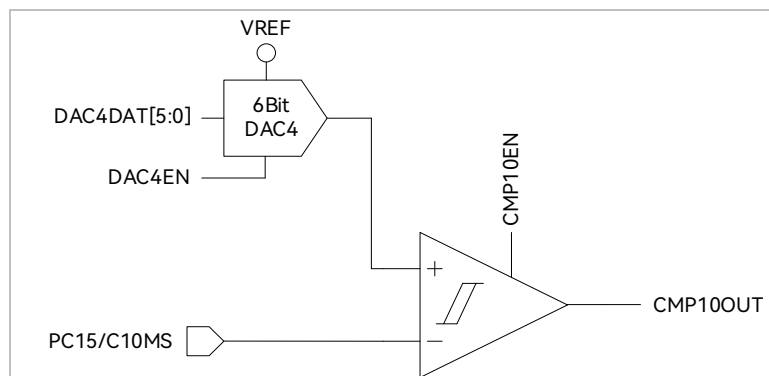
The I/O pins of CMP10 are shown in Figure 33-9. CMP10OUT can be read by software or reversed on external interrupt EXTI0. When CMP9 is used for cycle-by-cycle current limiting protection, CMP10 is used

for bus over-current protection of the master motor. When the bus current OCP feature of CMP10 is triggered, the output must be turned off by software.

CMP10 configurations are as follows:

1. Configure PC_AN[15] = 1 to assign PC15 to analog signal;
2. Configure CMP_CR5[CMP10EN] = 1 to enable CMP10;
3. Configure CMP_IFR[CMP10IF] = 0 to clear the interrupt flag bit of CMP10;
4. Configure CMP_CR4[CMP10IN] = 10 to select falling edge to trigger CMP10 interrupt.

Figure 33-9 CMP10 I/O Pins



33.1.5 CMP5

CMP5 is a hysteresis comparator as shown in Figure 33-10. CMP5OUT can be read by the software. CMP5 is used for PFC over-current protection.



Note:

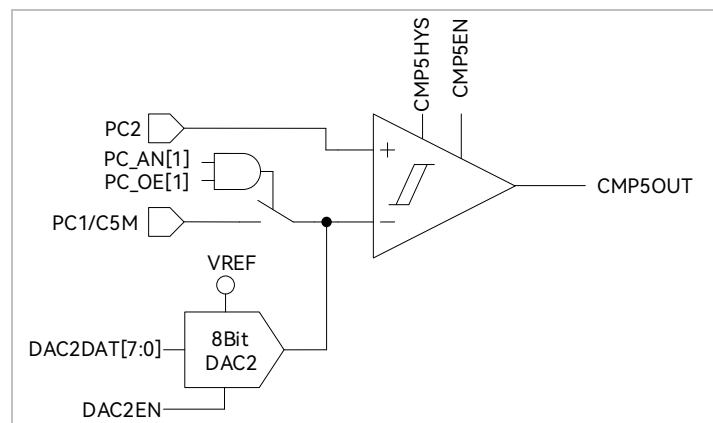
When an OCP event occurs, CMP5 forces PFC1 output low. It does not clear PFC_CR0[PFCEN] and PFC_CR0[PFCOE]. In this case, PFC_CR0[PFC_FORC1] can be read to determine if such forced pull-down has occurred.

CMP5 configurations are as follows:

1. Select the reference voltage for the negative input of CMP5. The voltage source can be on-chip DAC2 output or external circuit input.
 - For the external circuit input, configure PC_AN[1] = 1 and PC_OE[1] = 1 to apply the external voltage via PC1 as the reference voltage for the negative input of CMP5;

- For DAC2 output, configure `DAC_CR[DAC2EN] = 1` to enable DAC2, then set the corresponding DAC2 code value to apply its output as the reference voltage for the negative input of CMP5;
 - When DAC2 is enabled, you can also configure `PC_AN[1] = 1` and `PC_OE[1] = 1`, and connect a 100pF external capacitor (recommended) between PC1 and GND. This helps stabilize DAC2 output voltage over time;
2. Configure `PC_AN[2] = 1` to assign PC2 to analog signal;
 3. Configure `CMP_CR1[CMP5HYS] = 1` to enable CMP5;
 4. Configure `CMP_CR1[CMP5EN] = 1` to enable CMP5.

Figure 33–10 CMP5 I/O Pins



33.1.6 CMP11

CMP11 is a hysteresis comparator, as shown in Figure 33–11. CMP11OUT can be read by software. CMP11 is used for PFC OCP.



Note:

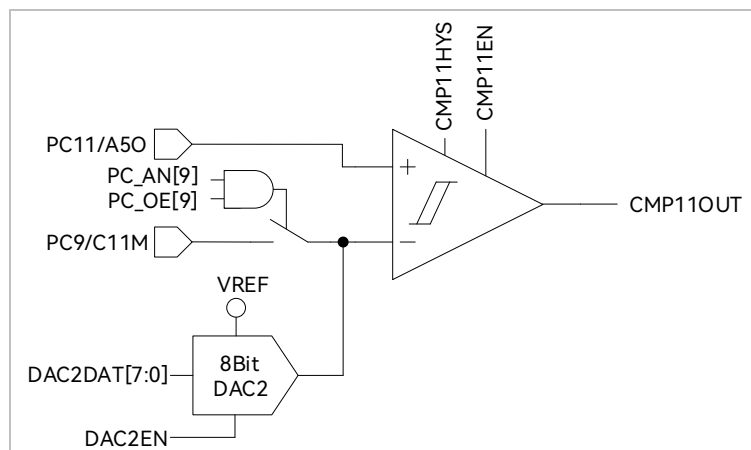
When an OCP event occurs, CMP11 forces PFC2 output low. It does not clear `PFC_CR0[IAC2EN]` and `PFC_CR0[PFCOE]`. In this case, `PFC_CR0[PFC_FORC2]` can be read to determine if such forced pull-down has occurred.

CMP11 configurations are as follows:

1. Select the reference voltage for the negative input of CMP11. The voltage source can be on-chip DAC2 output or external circuit input.
 - For the external circuit input, configure `PC_AN[9] = 1` and `PC_OE[9] = 1` to apply the external voltage via PC9 as the reference voltage for the negative input of CMP11;

- For DAC2 output, configure `DAC_CR[DAC2EN] = 1` to enable DAC2, then set the corresponding DAC2 code value to apply its output as the reference voltage for the negative input of CMP11;
 - When DAC2 is enabled, you can also configure `PC_AN[9] = 1` and `PC_OE[9] = 1`, and connect a 100pF external capacitor (recommended) between PC9 and GND. This helps stabilize DAC2 output voltage over time;
2. Configure `PC_AN[11] = 1`. PC11 is analog signal mode.
 3. Configure `CMP_CR1[CMP11HYS] = 1` to enable CMP11 hysteresis.
 4. Configure `CMP_CR1[CMP11EN] = 1` to enable CMP11.

Figure 33-11 CMP11 I/O Pins



33.1.7 Comparator Group 1 (CMPG1)

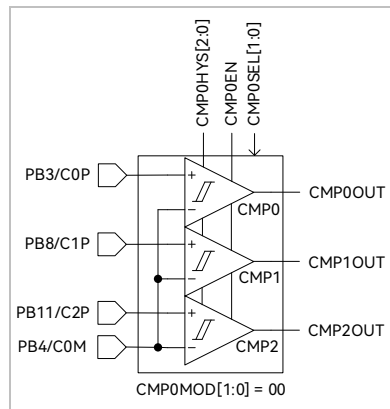
Comparator Group 1 (CMPG1) is a collection of CMP0, CMP1, and CMP2, with multiple comparison modes for different applications.

33.1.7.1 Three Comparators without Built-in Resistors Mode

When `CMP_CR2[CMP0MOD] = 00`, CMPG1 works with three comparators without built-in resistors. The I/O pins of CMPG1 are shown in Figure 33-12. It is used for BEMF detection with external virtual neutral point by the resistor. The negative inputs of the three comparators are connected together to PB4, and the positive inputs are connected to PB3, PB8 and PB11 respectively. The outputs are CMP0OUT, CMP1OUT and CMP2OUT respectively. The number of comparators working in this mode is defined by `CMP_CR2[CMP0SEL]`. When `CMP_CR2[CMP0SEL] = 00`, CMP0, CMP1 and CMP2 work simultaneously, which is the recommended configuration. When `CMP_CR2[CMP0SEL] = 01`, only CMP0 works. When

CMP_CR2[CMP0SEL] = 10, only CMP1 works. When CMP_CR2[CMP0SEL] = 11, only CMP2 works.

Figure 33-12 CMPG1 in Three Comparators Mode (Without Built-in Resistor)

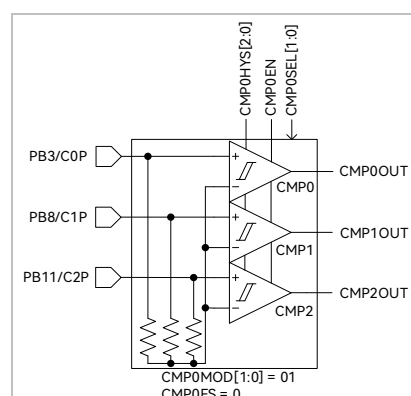


33.1.7.2 Three Comparators with Built-in Resistors Mode

When CMP_CR2[CMP0MOD] = 01, CMPG1 works with three comparators with built-in resistors. It is used for BEMF detection with internal virtual neutral point by the resistor. The input pins can be selected by setting the function switching bit CMP_CR2[CMP0FS]. The number of comparators in this mode is defined by CMP_CR2[CMP0SEL]. When CMP_CR2[CMP0SEL] = 00, CMP0, CMP1 and CMP2 work simultaneously, which is the recommended configuration. When CMP_CR2[CMP0SEL] = 01, only CMP0 works. When CMP_CR2[CMP0SEL] = 10, only CMP1 works. When CMP_CR2[CMP0SEL] = 11, only CMP2 works.

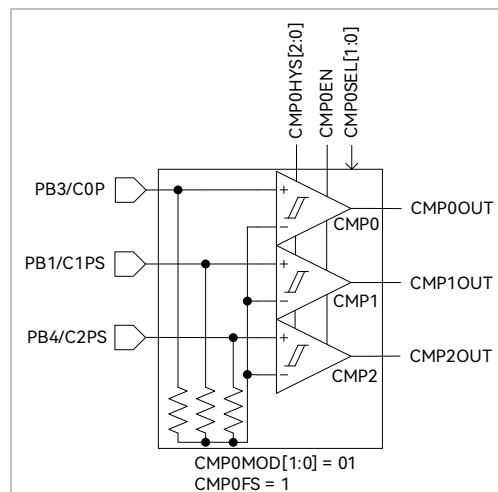
When CMP_CR2[CMP0FS] = 0, the I/O pins of CMPG1 are shown in Figure 33-13. The negative inputs of the three comparators are connected together to the center point of the built-in resistors. The positive inputs are connected to PB3, PB8, and PB11 respectively, and the outputs are CMP0OUT, CMP1OUT, and CMP2OUT respectively.

Figure 33-13 CMPG1 in Built-in Three Comparators and Resistors Mode without Function Switching



When $\text{CMP\_CR2}[\text{CMP0FS}] = 1$, the I/O pins of CMPG1 are shown in Figure 33-14. The negative inputs of the three comparators are connected together to the center point of the built-in resistors. The positive inputs are connected to PB3, PB1 and PB4 respectively, and the outputs are CMP0OUT, CMP1OUT and CMP2OUT respectively.

Figure 33-14 CMPG1 in Built-in Three Comparators and Resistors Mode with Function Switching

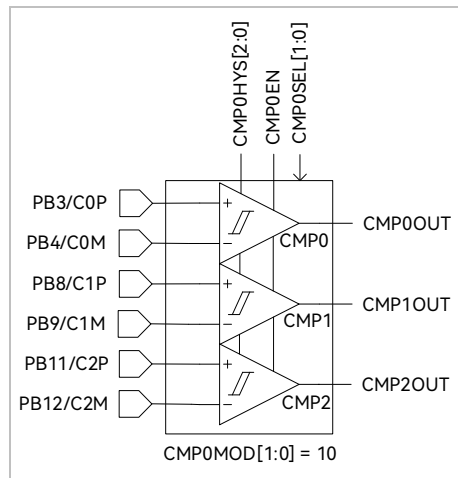


33.1.7.3 Triple-differential-comparator Mode

When $\text{CMP\_CR2}[\text{CMP0MOD}] = 10$, CMPG1 works in triple-differential-comparator mode, where the motor rotor position is detected by differential Hall signals. The I/O pins of CMPG1 are shown in

Figure 33–15. The negative inputs of the three comparators are respectively connected to PB4, PB9 and PB12, and the positive inputs are respectively connected to PB3, PB8 and PB11. The outputs are CMP0OUT, CMP1OUT and CMP2OUT respectively. The number of comparators working in this mode is defined by CMP_CR2[CMP0SEL]. When CMP_CR2[CMP0SEL] = 00, CMP0, CMP1 and CMP2 work simultaneously, which is the recommended configuration. When CMP_CR2[CMP0SEL] = 01, only CMP0 works. When CMP_CR2[CMP0SEL] = 10, only CMP1 works. When CMP_CR2[CMP0SEL] = 11, only CMP2 works.

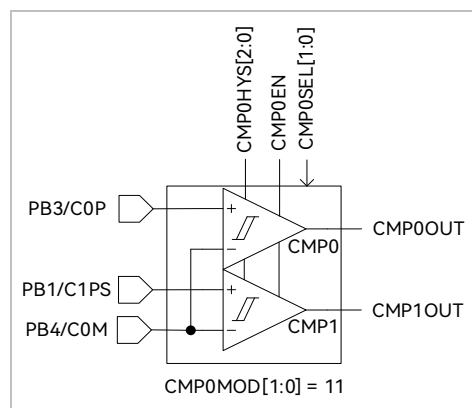
Figure 33-15 CMPG1 in Triple-differential-comparator Mode



33.1.7.4 Dual-comparator mode

When $\text{CMP\_CR2}[\text{CMP0MOD}] = 11$, CMPG1 works in dual-comparator mode. The I/O pins of CMPG1 are shown in Figure 33-16. The negative inputs of the two comparators are connected together to PB4, and the positive inputs are connected to PB3 and PB1 respectively. The outputs are CMP0OUT and CMP1OUT respectively. The number of comparators in this mode is defined by $\text{CMP\_CR2}[\text{CMP0SEL}]$. When $\text{CMP\_CR2}[\text{CMP0SEL}] = 00$, CMP0 and CMP1 work simultaneously, which is the recommended configuration. When $\text{CMP\_CR2}[\text{CMP0SEL}] = 01$, only CMP0 works. When $\text{CMP\_CR2}[\text{CMP0SEL}] = 10$, only CMP1 works.

Figure 33-16 CMPG1 in Dual-comparator Mode



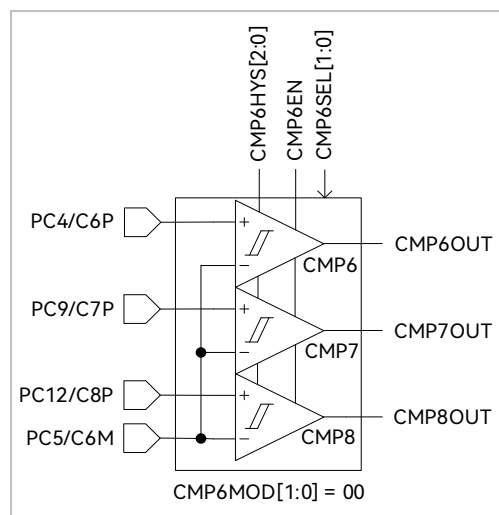
33.1.8 Comparator Group 2 (CMPG2)

Comparator Group 2 (CMPG2) is a collection of CMP6, CMP7 and CMP8, with multiple comparison modes for different applications.

33.1.8.1 Three Comparators without Built-in Resistors Mode

When $\text{CMP\_CR6}[\text{CMP6MOD}] = 00$, CMPG2 with three comparators without built-in resistors. The I/O pins of CMPG2 are shown in Figure 33-17. It is used for BEMF detection with external virtual neutral point by the resistor. The negative inputs of the three comparators are connected together to PC5, and the positive inputs are connected to PC4, PC9 and PC12 respectively. The outputs are CMP6OUT, CMP7OUT and CMP8OUT respectively. The number of comparators working in this mode is defined by $\text{CMP\_CR6}[\text{CMP6SEL}]$. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 00$, CMP6, CMP7 and CMP8 work simultaneously, which is the recommended configuration. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 01$, only CMP6 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 10$, only CMP7 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 11$, only CMP8 works.

Figure 33-17 CMPG2 in Three Comparators Mode
(without Built-in Resistor)



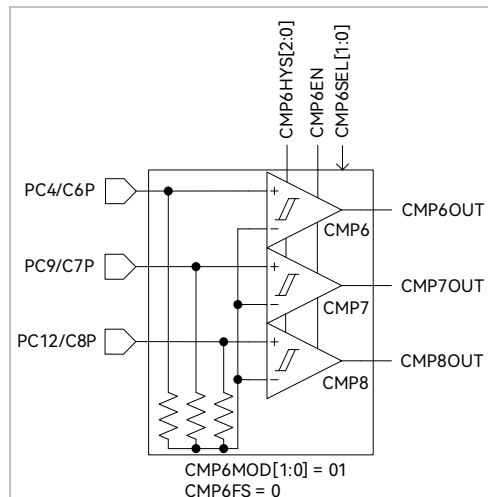
33.1.8.2 Three Comparators with Built-in Resistors Mode

When $\text{CMP\_CR6}[\text{CMP6MOD}] = 01$, CMPG2 works with three comparators with built-in resistors. It is used for BEMF detection with internal virtual neutral point by the resistor. The input pins can be selected by setting the function switching bit $\text{CMP\_CR6}[\text{CMP6FS}]$. The number of comparators operating in this mode is defined by $\text{CMP\_CR6}[\text{CMP6SEL}]$. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 00$, CMP6, CMP7 and CMP8 work simultaneously, which is the recommended configuration. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 01$, only CMP6 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 10$, only CMP7 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 11$, only CMP8 works.

When $\text{CMP\_CR6}[\text{CMP6FS}] = 0$, the I/O pins of CMPG2 are shown in Figure 33-18. The negative inputs of

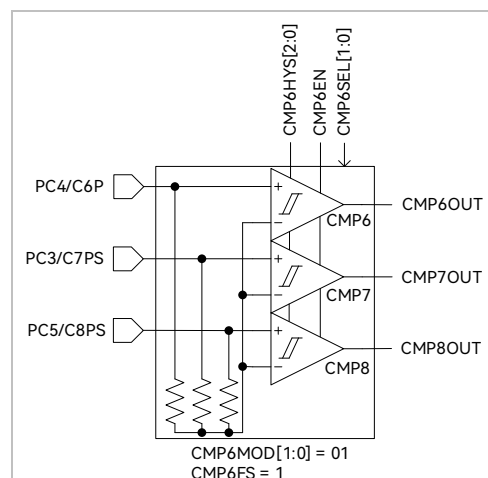
the three comparators are connected together to the center point of the built-in resistors. The positive inputs are connected to PC4, PC9 and PC12 respectively, and the outputs are CMP6OUT, CMP7OUT and CMP8OUT respectively.

Figure 33-18 CMPG2 in Built-in Three Comparators
and Resistors Mode without Function Switching



When $\text{CMP\_CR6}[\text{CMP6FS}] = 1$, the I/O pins of CMPG2 are shown in Figure 33-19. The negative inputs of the three comparators are connected together to the center point of the built-in resistors. The positive inputs are connected to PC4, PC3 and PC5 respectively, and the outputs are CMP6OUT, CMP7OUT and CMP8OUT respectively.

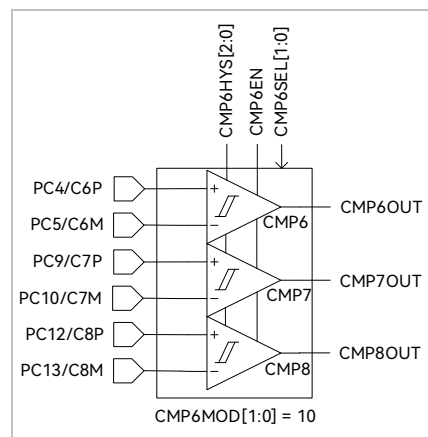
Figure 33-19 CMPG2 in Built-in Three Comparators
and Resistors Mode with Function Switching



33.1.8.3 Triple-differential-comparator Mode

When $\text{CMP\_CR6}[\text{CMP6MOD}] = 10$, CMPG works in triple-differential-comparator mode, where the motor rotor position is detected by differential Hall signals. The I/O pins of CMPG2 are shown in Figure 33-20. The negative inputs of the three comparators are respectively connected to PC5, PC10 and PC13, and the positive inputs are respectively connected to PC4, PC9 and PC12. The outputs are CMP6OUT, CMP7OUT and CMP8OUT respectively. The number of comparators working in this mode is defined by $\text{CMP\_CR6}[\text{CMP6SEL}]$. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 00$, CMP6, CMP7 and CMP8 work simultaneously, which is the recommended configuration. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 01$, only CMP6 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 10$, only CMP7 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 11$, only CMP8 works.

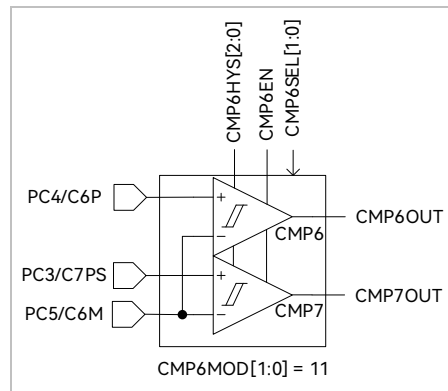
Figure 33-20 CMPG2 in Triple-differential-comparator Mode



33.1.8.4 Dual-comparator Mode

When $\text{CMP\_CR6}[\text{CMP6MOD}] = 11$, CMPG works in dual-comparator mode. The I/O pins of CMPG2 are shown in Figure 33-21. The negative inputs of the two comparators are connected together to PC5, and the positive inputs are connected to PC4 and PC3 respectively. The outputs are CMP6OUT and CMP7OUT respectively. The number of comparators in this mode is defined by $\text{CMP\_CR6}[\text{CMP6SEL}]$. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 00$, CMP6 and CMP7 work simultaneously, which is the recommended configuration. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 01$, only CMP6 works. When $\text{CMP\_CR6}[\text{CMP6SEL}] = 10$, only CMP7 works.

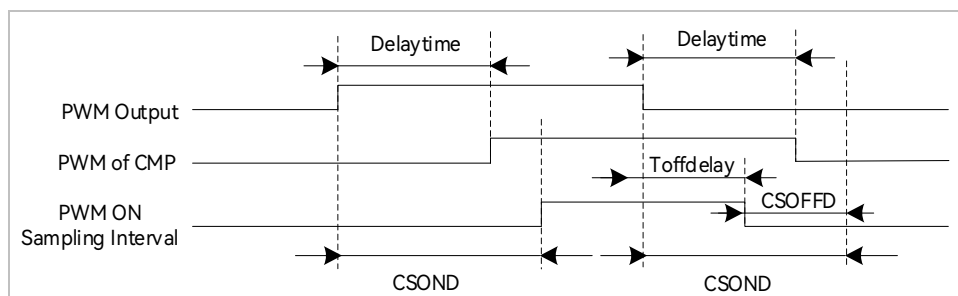
Figure 33-21 CMPG2 in Dual-comparator Mode



33.1.9 Comparator Sampling

The comparator sampling feature is mainly used for the square-wave control and RSD, which eliminates switching interference from driving circuit. See section 16.2.5.1 for RSD.

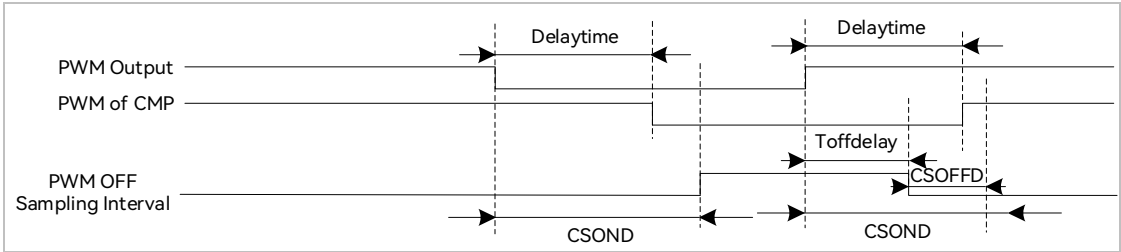
Figure 33-22 PWM ON Sampling Mode



There is a delay from the PWM output to the output of the comparator, which is mainly affected by the following factors: resistance value of drive resistor, switching speed of the power ICs, and input delay and hysteresis settings of the comparator. As shown in the figure above, the delay time is from the chip output to the comparator output. When high-level sampling is performed, the sampling interval shall be enveloped by actual high-level output of the comparator. First, the sampling ON-delayed time $\text{CMP\_SAMR}[\text{CSOND}]$ is set to overcome the output delay and the oscillation interval of the power device. At the end of the sampling interval, $\text{CMP\_SAMR}[\text{CSOND}]$ is delayed after the falling edge of PWM, at which time the actual sampling window has exceeded the corresponding high-level interval. The advanced sampling time in PWM OFF mode $\text{CMP\_SAMR}[\text{CSOFFD}]$ is set to stop sampling Toffdelay after the PWM output falling edge, where $\text{Toffdelay} = \text{CMP\_SAMR}[\text{CSOND}] - \text{CMP\_SAMR}[\text{CSOFFD}]$. By configuring $\text{CMP\_SAMR}[\text{CSOND}]$ and $\text{CMP\_SAMR}[\text{CSOFFD}]$, the sampling interval can be located in the high-level

interval of the actual output of the comparator.

Figure 33-23 PWM OFF Sampling Mode



Similarly, when low-level sampling is performed, the delayed sampling time in PWM ON mode `CMP_SAMR[CSOND]` and advanced sampling time in PWM OFF mode `CMP_SAMR[CSOFFD]` are set reasonably to ensure that the actual sampling interval is located in the actually low-level output interval of the comparator.

Method for measuring the delay of PWM output to comparator: `CMP_CR2[CMPSAMSEL] = 00` to disable the comparator sampling delay feature. Enable the PWM output and comparator, manually rotate the motor to change the comparator value, and measure the delay between the PWM output and the comparator output.

33.2 Comparator Registers

33.2.1 CMP_CR0 (CSR: 0x600)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMP5IM		CMP4IM		CMP3IM		CMP2IM		CMP1IM		CMP0IM	
																				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11:10]	CMP5IM	CMP5 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge.

		11: The interrupt flag CMP_IFR[CMP5IF] is set to “1” upon falling edge, but no interrupt is generated.  Note: When an interrupt event occurs, if PFC_CR0[PFC_FM] is set as “0”, CMP5 forces PFC1 output (PWM1) low, while if PFC_CR0[PFC_FM] is set as “1”, CMP5 forces PFC1/PFC2 outputs (PWM1 and PWM2) low, but it does not clear PFC_CR0[PFCEN], PFC_CR0[IAC2EN] and PFC_CR0[PFCOE].
[9:8]	CMP4IM	CMP4 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: The interrupt flag CMP_IFR[CMP4IF] is set to “1” upon both rising/falling edges, but no interrupt is generated.
[7:6]	CMP3IM	CMP3 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. If DRV1_CR[MOEMD] is not set as “0”, DRV1_CR[MOE] is cleared to “0”^[1] 10: An interrupt is generated upon falling edge. If DRV1_CR[MOEMD] is not set as “0”, DRV1_CR[MOE] is cleared to “0” 11: DRV1_CR[MOE] is cleared to “0” upon rising edge. The interrupt flag CMP_IFR[CMP3IF] is set to “1”, but no interrupt is generated^[2]  Note: > [1] See section 18.16.2.3 for MOE configurations > [2] When CMP3 is used for cycle-by-cycle current limiting, DRV1_CR[MOEMD] is set to 10/11
[5:4]	CMP2IM	CMP2 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge 10: An interrupt is generated upon falling edge 11: An interrupt is generated upon both rising/falling edges
[3:2]	CMP1IM	CMP1 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge 10: An interrupt is generated upon falling edge 11: An interrupt is generated upon both rising/falling edges

[1:0]	CMP0IM	CMP0 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge 10: An interrupt is generated upon falling edge 11: An interrupt is generated upon both rising/falling edges

33.2.2 CMP_CR1 (CSR: 0x601)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSV																CMP0HYSDIG	CMP0HYSMOD	CMP3P4MFS	CMP11HYS	CMP5HYS	CMP11EN	CMP5EN	CMP4EN	CMP3MOD		CMP3EN	CMP3HYS	RSV	CMP0HYS			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	-	-	r/w	r/w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:15]	RSV	Reserved
[14]	CMP0HYSDIG	CMPG1 Hysteresis Direction Selection It works when CMP_CR1[CMP0HYSMOD] is set to “1”. The hysteresis voltage is set via the bit CMP0HYS. 0: Positive Hysteresis 1: Negative Hysteresis
[13]	CMP0HYSMOD	CMPG1 Hysteresis Output Control It is valid only when CMPG1 is in BEMF mode, and invalid in freewheeling mode or polling mode. 0: The hysteresis direction follows comparator output 1: The hysteresis direction follows CMP0HYSDIG configuration
[12]	CMP3P4MFS	Functions of C3P and C4M are switched to PB15. The output is used for bus current sampling (A0O output is connected to PB15) and then directly fed into the over-current comparator. 0: Disable 1: Enable. In this case, there is only one input for CMP3 positive side.
[11]	CMP11HYS	CMP11 Hysteresis 0: Disable 1: Enable
[10]	CMP5HYS	CMP5 Hysteresis 0: Disable

		1: Enable
[9]	CMP11EN	CMP11 Enable 0: Disable 1: Enable
[8]	CMP5EN	CMP5 Enable 0: Disable 1: Enable
[7]	CMP4EN	CMP4 Enable 0: Disable 1: Enable
[6:5]	CMP3MOD	CMP3 Mode Selection Negative input connected to PB14 or DAC0 output 00: Single-comparator mode, where PB7 (PB15) is connected to the positive input, as shown in Figure 33-2. 01: Dual-comparator mode, where PB10 and PB13 are connected to the positive inputs, as shown in Figure 33-3. 1x: Triple-comparator mode, where PB7, PB10 and PB13 are connected to the positive inputs, as shown in Figure 33-4.
[4]	CMP3EN	CMP3 Enable 0: Disable 1: Enable
[3]	CMP3HYS	CMP3 Hysteresis 0: Disable 1: Enable
[2]	RSV	Reserved
[1:0]	CMP0HYS	CMP0/1/2 Hysteresis Voltage Selection 00: Disable 01: $\pm 3\text{mV}$ 10: $\pm 6\text{mV}$ 11: $\pm 12\text{mV}$

33.2.3 CMP_CR2 (CSR: 0x602)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMPSAMSEL		RSV	HALL0EN	CMP0FS	CMP0MOD		CMP0SEL		CMP0CSEL		CMP0EN
																				rw	rw										
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11:10]	CMPSAMSEL	Sampling Delay for CMP0, CMP1 and CMP2 during PWM ON/OFF 00: Sampling during PWM ON and OFF without time delay 01: Sampling during PWM OFF only, with time delay based on CMP_SAMR 10: Sampling during PWM ON only, with time delay based on CMP_SAMR 11: Sampling during PWM ON and OFF, with time delay based on CMP_SAMR
[9]	RSV	Reserved
[8]	HALL0EN	Hall0 Enable 0: Disable 1: Enable
[7]	CMP0FS	CMP1/CMP2 Function Switching 0: Disable 1: Enable. This bit works only when CMP_CR2[CMP0MOD] = 01.
[6:5]	CMP0MOD	CMPG1 Mode Setting 00: BEMF mode without internal virtual neutral point by the resistors, as shown in Figure 33-12 01: BEMF mode with internal virtual neutral point by the resistors, as shown in Figure 33-13 and Figure 33-14 10: Triple-differential-comparator mode, as shown in Figure 33-15 11: Dual-comparator mode, as shown in Figure 33-16
[4:3]	CMP0SEL	CMPG1 Pin Combination Selection It works with CMP_CR2[CMP0MOD]. Table 33-1 Function Description on Combination of CMPG1 Pins and CMP_CR2[CMP0MOD]

CMP0MOD	CMP0SEL	Description

	00	00	CMP0/1/2 work simultaneously, as shown in Figure 33-12. The negative input of these comparators are connected to C0M. The hardware automatically compares the positive inputs C0P, C1P and C2P with C0M, and the output results are transferred to CMP_SR[CMP0OUT], CMP_SR[CMP1OUT] and CMP_SR[CMP2OUT] respectively.
		01	Only CMP0 works. The positive input is connected to C0P, and the negative input to C0M. The output results are transferred to CMP_SR[CMP0OUT].
		10	Only CMP1 works. The positive input is connected to C1P, and the negative input to C0M. The output results are transferred to CMP_SR[CMP1OUT].
		11	Only CMP2 works. The positive input is connected to C2P, and the negative input to C0M. The output results are transferred to CMP_SR[CMP2OUT].
	01	00	CMP0/1/2 work simultaneously, as shown in Figure 33-13 and Figure 33-14. The negative inputs of these comparators are connected to the center of built-in BEMF resistors. When CMP_CR2[CMP0FS] = 0, the hardware automatically compares the positive inputs C0P, C1P and C2P with C0M. When CMP_CR2[CMP0FS] = 1, the hardware automatically compares the positive inputs C0P, C1PS and C2PS with C0M. The output results are transferred to CMP_SR[CMP0OUT], CMP_SR[CMP1OUT] and CMP_SR[CMP2OUT] respectively.
		01	Only CMP0 works. The positive input is connected to C0P, and the negative input to the center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP0OUT].
		10	Only CMP1 works. When CMP_CR2[CMP0FS] = 0, the positive input is connected to C1P, and when CMP_CR2[CMP0FS] = 1, it is connected to C1PS. The negative input is connected to the center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP1OUT].
		11	Only CMP2 works. When CMP_CR2[CMP0FS] = 0, the positive input is connected to C2P, and when

				CMP_CR2[CMP0FS] = 1, it is connected to C2PS. The negative input is connected to the center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP2OUT].
		10	00	CMP0/1/2 work simultaneously, as shown in Figure 33-15. The positive inputs of these comparators are connected to C0P, C1P and C2P respectively, and the negative inputs are connected to C0M, C1M and C2M respectively. The output results are transferred to CMP_SR[CMP0OUT], CMP_SR[CMP1OUT] and CMP_SR[CMP2OUT] respectively.
			01	Only CMP0 works. The positive input is connected to C0P, and the negative input to C0M. The output results are transferred to CMP_SR[CMP0OUT].
			10	Only CMP1 works. The positive input is connected to C1P, and the negative input to C1M. The output results are transferred to CMP_SR[CMP1OUT].
			11	Only CMP2 works. The positive input is connected to C2P, and the negative input to C2M. The output results are transferred to CMP_SR[CMP2OUT].
		11	00	CMP0/1 work simultaneously, as shown in Figure 33-16. The positive inputs are connected to C0P and C1PS respectively, and the negative inputs to C0M. The outputs results are transferred to CMP_SR[CMP0OUT] and CMP_SR[CMP1OUT] respectively.
			01	Only CMP0 works. The positive input is connected to C0P, and the negative input to C0M. The output results are transferred to CMP_SR[CMP0OUT].
			10	Only CMP1 works. The positive input is connected to C1PS, and the negative input to C0M. The output results are transferred to CMP_SR[CMP1OUT].
			11	Reserved
		CMP0/1/2 Rolling Speed Selection		
[2:1]	CMP0CSEL	00: Normal Speed 01: Fast Speed 10: Slow Speed		

		11: Low Speed
[0]	CMP0EN	CMP0/1/2 Enable 0: Disable 1: Enable

33.2.4 CMP_CR3 (CSR: 0x603)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMP5FSEL		CMP9FSEL		CMP3FSEL		CMP6FSEL			CMP0FSEL		
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11:10]	CMP5FSEL	CMP5 Filter Settings 00: Disable 01: 4 system clock cycles 10: 8 system clock cycles 11:16 system clock cycles
[9:8]	CMP9FSEL	CMP9 Filter Settings 00: Disable 01: 4 system clock cycles 10: 8 system clock cycles 11:16 system clock cycles
[7:6]	CMP3FSEL	CMP3 Filter Settings 00: Disable 01: 4 system clock cycles 10: 8 system clock cycles 11:16 system clock cycles
[5:3]	CMP6FSEL	CMP6/7/8 Filter Settings 000: 4 system clock cycles 001: 8 system clock cycles 010: 16 system clock cycles 011: 24 system clock cycles 100: 32 system clock cycles

		101: 64 system clock cycles 110: 96 system clock cycles 111: 128 system clock cycles
[2:0]	CMP0FSEL	CMP0/1/2 Filter Settings 000: 4 system clock cycles 001: 8 system clock cycles 010: 16 system clock cycles 011: 24 system clock cycles 100: 32 system clock cycles 101: 64 system clock cycles 110: 96 system clock cycles 111: 128 system clock cycles

33.2.5 CMP_SR (CSR: 0x604)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMP11OUT	CMP10OUT	CMP9OUT	CMP8OUT	CMP7OUT	CMP6OUT	CMP5OUT	CMP4OUT	CMP3OUT	CMP2OUT	CMP1OUT	CMP0OUT
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11]	CMP11OUT	CMP11 comparison result
[10]	CMP10OUT	CMP10 comparison result
[9]	CMP9OUT	CMP9 comparison result
[8]	CMP8OUT	CMP8 comparison result
[7]	CMP7OUT	CMP7 comparison result
[6]	CMP6OUT	CMP6 comparison result
[5]	CMP5OUT	CMP5 comparison result
[4]	CMP4OUT	CMP4 comparison result
[3]	CMP3OUT	CMP3 comparison result
[2]	CMP2OUT	CMP2 comparison result
[1]	CMP1OUT	CMP1 comparison result
[0]	CMP0OUT	CMP0 comparison result

33.2.6 CMP_IFR (CSR: 0x605)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMP11IF	CMP10IF	CMP9IF	CMP8IF	CMP7IF	CMP6IF	CMP5IF	CMP4IF	CMP3IF	CMP2IF	CMP1IF	CMP0IF
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0	rw0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11]	CMP11IF	CMP11 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[10]	CMP10IF	CMP10 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[9]	CMP9IF	CMP9 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[8]	CMP8IF	CMP8 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”.

		1: No effect
[7]	CMP7IF	CMP7 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[6]	CMP6IF	CMP6 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[5]	CMP5IF	CMP5 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[4]	CMP4IF	CMP4 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[3]	CMP3IF	CMP3 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to “0”. 1: No effect
[2]	CMP2IF	CMP2 Interrupt Flag Read:

		0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to "0". 1: No effect
[1]	CMP1IF	CMP1 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to "0". 1: No effect
[0]	CMP0IF	CMP0 Interrupt Flag Read: 0: No Interrupt Pending 1: Interrupt Pending Write: 0: This bit is cleared to "0". 1: No effect

33.2.7 CMP_SAMR (CSR: 0x606)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								CSOND				CSOFFD			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:4]	CSOND	CMPG1/CMPG2 Delayed Sampling Time When PWM module switches from OFF to ON or from ON to OFF, the power IC's turn-on/off affects input signal of the comparator. To avoid this interference, CMP_SAMR[CSOND] can be configured to delay the sampling of CMPG1 /CMPG2. Delayed sampling time = 32*CMP_SAMR[CSOND]*T  Note:

		CMP_SAMR[CSOND] must be greater than or equal to CMP_SAMR[CSOFFD]
[3:0]	CSOFFD	CMPG1/CMPG2 Advanced Sampling Time After CMP_SAMR[CSOND] is configured, sampling ends at the point defined by CMP_SAMR[CSOND] - CMP_SAMR[CSOFFD] after the back edge of PWM output, ensuring sampling interval enveloped by the PWM interval. Advanced sampling time = $32 * \text{CMP\_SAMR[CSOFFD]} * T$  Note: CMP_SAMR[CSOND] must be greater than or equal to CMP_SAMR[CSOFFD]

33.2.8 CMP_DBR (CSR: 0x607)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																DBGSEL2					DBGSEL1					RSV					
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-

Bit	Name	Description
[31:15]	RSV	Reserved
[14:10]	DBGSEL2	Debug Output Selection, connected to PB0 00000: Disable 00001: ADC1 Trigger Signal 00010: ADC2 Trigger Signal 00011: ADC3 Trigger Signal 00100: CMP0/1/2 Sampling Output during PWM ON 00101: CMP0/1/2 Sampling Output during PWM OFF 00110: CMP6/7/8 Sampling Output during PWM ON 00111: CMP6/7/8 Sampling Output during PWM OFF 01000: CMP0/1/2 Sampling Output during PWM ON/OFF 01001: CMP6/7/8 Sampling Output during PWM ON/OFF 01010: Reserved 01011: Reserved 01100: FOC Calculation in Progress 01101: FOC Current-loop Calculation in Progress 01110: FOC Calculation in Progress (Slave Motor) 01111: Reserved

		10000: DRVx_CNTR Direction (Master Motor) 10001: DRVx_CNTR Overflow Point (Master Motor) 10010: DRVx_CNTR Underflow Point (Master Motor) 10011: OMEGA Startup in Progress (Master Motor) 10100: HFI Status (Master Motor) 10101: Outer-loop Calculation in Progress (Master Motor) 10110: Reserved 10111: Reserved 11000: DRVx_CNTR Direction (Slave Motor) 11001: DRVx_CNTR Overflow Point (Slave Motor) 11010: DRVx_CNTR Underflow Point (Slave Motor) 11011: OMEGA Startup in Progress (Slave Motor) 11100: HFI Status (Slave Motor) 11101: Outer-loop Calculation in Progress (Slave Motor) 11110: Reserved 11111: Reserved
[9:5]	DBGSEL1	Debug Output Selection, connected to PA1 00000: Disable 00001: ADC1 Trigger Signal 00010: ADC2 Trigger Signal 00011: ADC3 Trigger Signal 00100: CMP0/1/2 Sampling Output during PWM ON 00101: CMP0/1/2 Sampling Output during PWM OFF 00110: CMP6/7/8 Sampling Output during PWM ON 00111: CMP6/7/8 Sampling Output during PWM OFF 01000: CMP0/1/2 Sampling Output during PWM ON/OFF 01001: CMP6/7/8 Sampling Output during PWM ON/OFF 01010: Reserved 01011: Reserved 01100: FOC Calculation in Progress 01101: FOC Current-loop Calculation in Progress 01110: FOC Calculation in Progress (Slave Motor) 01111: Reserved 10000: DRVx_CNTR Direction (Master Motor) 10001: DRVx_CNTR Overflow Point (Master Motor) 10010: DRVx_CNTR Underflow Point (Master Motor) 10011: OMEGA Startup in Progress (Master Motor) 10100: HFI Status (Master Motor) 10101: Outer-loop Calculation in Progress (Master Motor)

		10110: Reserved 10111: Reserved 11000: DRVx_CNTR Direction (Slave Motor) 11001: DRVx_CNTR Overflow Point (Slave Motor) 11010: DRVx_CNTR Underflow Point (Slave Motor) 11011: OMEGA Startup in Progress (Slave Motor) 11100: HFI Status (Slave Motor) 11101: Outer-loop Calculation in Progress (Slave Motor) 11110: Reserved 11111: Reserved
[4:0]	RSV	Reserved

33.2.9 CMP_CR4 (CSR: 0x608)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																				CMP11IM		CMP10IM		CMP9IM		CMP8IM		CMP7IM		CMP6IM	
																				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	

Bit	Name	Description
[31:12]	RSV	Reserved
[11:10]	CMP11IM	CMP11 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: The interrupt flag CMP_IFR[CMP11IF] is set to “1” upon falling edge, but no interrupt is generated.  Note: When an interrupt event occurs, if PFC_CR0[PFC_FM] is set as “0”, CMP11 forces PFC2 output (PWM2) low, while if PFC_CR0[PFC_FM] is set as “1”, CMP11 forces PFC1/PFC2 outputs (PWM1 and PWM2) low, but it does not clear PFC_CR0[PFCEN], PFC_CR0[IAC2EN] and PFC_CR0[PFCOE].
[9:8]	CMP10IM	CMP10 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge.

		11: The interrupt flag CMP_IFR[CMP10IF] is set to “1” upon both rising/falling edges, but no interrupt is generated.
[7:6]	CMP9IM	CMP9 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. If DRV2_CR[MOEMD] is not set as “0”, DRV2_CR[MOE] is cleared to “0”^[1]. 10: An interrupt is generated upon falling edge. If DRV2_CR[MOEMD] is not set as “0”, DRV2_CR[MOE] is cleared to “0”. 11: DRV2_CR[MOE] is cleared to “0” upon rising edge. The interrupt flag CMP_IFR[CMP9IF] is set to “1”, but no interrupt is generated^[2].  Note: > [1] See section 18.16.2.3 for MOE configurations > [2] When CMP9 is used for cycle-by-cycle current limiting, DRV2_CR[MOEMD] = 10/11 is set to 10/11
[5:4]	CMP8IM	CMP8 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: An interrupt is generated upon both rising/falling edges.
[3:2]	CMP7IM	CMP7 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: An interrupt is generated upon both rising/falling edges.
[1:0]	CMP6IM	CMP6 Interrupt Mode 00: No interrupt is generated. 01: An interrupt is generated upon rising edge. 10: An interrupt is generated upon falling edge. 11: An interrupt is generated upon both rising/falling edges.

33.2.10 CMP_CR5 (CSR: 0x609)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																							CMP9P10MFS	CMP10EN	CMP9MOD		CMP9EN	CMP9HYS	RSV	CMP6HYS	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	-	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	-	0	0

Bit	Name	Description
[31:9]	RSV	Reserved
[8]	CMP9P10MFS	Functions of C9P and C10M are switched to PC15. The output is used for bus current sampling (A0O output is connected to PC15) and then directly fed into the over-current comparator. 0: Disable 1: Enable. In this case, there is only one input for CMP9 positive side.
[7]	CMP10EN	CMP10 Enable 0: Disable 1: Enable
[6:5]	CMP9MOD	CMP9 Mode Selection Negative input connected to PC0 or DAC3 output 00: Single-comparator mode, where PC15 is connected to the positive input, as shown in Figure 33-6.
[4]	CMP9EN	CMP9 Enable 0: Disable 1: Enable
[3]	CMP9HYS	CMP9 Hysteresis 0: Disable 1: Enable
[2]	RSV	Reserved
[1:0]	CMP6HYS	CMP6/7/8 Hysteresis Voltage Selection 00: Disable 01: ±3mV 10: ±6mV 11: ±12mV

33.2.11 CMP_CR6 (CSR: 0x60A)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																		
RSV																				CMPSAM1SEL		RSV	HALL1EN	CMP6FS	CMP6MOD		CMP6SEL		CMP6CSEL		CMP6EN																		
																				r/w	r/w																												
																				-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r/w	r/w	-	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
																				-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:12]	RSV	Reserved
[11:10]	CMPSAM1SEL	Sampling Delay for CMP6, CMP7 and CMP8 during PWM ON/OFF 00: Sampling during PWM ON and OFF modes without time delay 01: Sampling during PWM OFF only, with time delay based on CMP_SAMR 10: Sampling during PWM ON only, with time delay based on CMP_SAMR 11: Sampling during PWM ON and OFF, with time delay based on CMP_SAMR
[9]	RSV	Reserved
[8]	HALL1EN	Hall1 Enable 0: Disable 1: Enable
[7]	CMP6FS	CMP7/CMP8 Function Switching 0: Disable 1: Enable. This bit works only when CMP_CR6[CMP6MOD] = 01.
[6:5]	CMP6MOD	CMPG2 Mode Setting 00: BEMF mode without internal virtual neutral point by the resistors, as shown in Figure 33-17 01: BEMF mode with internal virtual neutral point by the resistors, as shown in Figure 33-18 and Figure 33-19 10: Triple-differential-comparator mode, as shown in Figure 33-20 11: Dual-comparator mode, as shown in Figure 33-21
[4:3]	CMP6SEL	CMPG2 Pin Combination Selection It works with CMP_CR6[CMP6MOD]. Table 33-2 Function Description on Combination of CMPG2 Pins and CMP_CR6[CMP6MOD]

CMP6MOD		CMP6SEL
00	00	CMP6/7/8 work simultaneously, as shown in Figure 33-17. The negative inputs of these

		comparators are connected to C6M. The hardware compares the positive inputs C6P, C7P, and C8P with the common negative input C6M, and the output results are transferred to CMP_SR[CMP6OUT], CMP_SR[CMP7OUT] and CMP_SR[CMP8OUT] respectively.
	01	Only CMP6 works. The positive input is connected to C6P, and the negative input to C6M. The output results are transferred to CMP_SR[CMP6OUT].
	10	Only CMP7 works. The positive input is connected to C7P, and the negative input to C6M. The output results are transferred to CMP_SR[CMP7OUT]
	11	Only CMP8 works. The positive input is connected to C8P, and the negative input to C6M. The output results are transferred to CMP_SR[CMP8OUT].
	01	CMP6/7/8 work simultaneously, as shown in Figure 33-18 and Figure 33-19. The negative inputs of these comparators are connected to the center of built-in BEMF resistors. When CMP_CR6[CMP6FS] = 0, the hardware automatically compares the positive inputs C6P, C7P and C8P with C6M. When CMP_CR6[CMP6FS] = 1, the hardware automatically compares the positive inputs C6P, C7PS and C8PS with C6M. The output results are transferred to CMP_SR[CMP6OUT], CMP_SR[CMP7OUT] and CMP_SR[CMP8OUT] respectively.
	01	Only CMP6 works. The positive input is connected to C6P, and the negative input to the center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP6OUT].
	10	Only CMP7 works. When CMP_CR6[CMP6FS]= 0, the positive input is connected to C7P, and when CMP_CR6[CMP6FS] = 1, it is connected to C7PS. The negative input is connected to the

			center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP7OUT].
		11	Only CMP8 works. When CMP_CR6[CMP6FS] = 0, the positive input is connected to C8P, and when CMP_CR6[CMP6FS] = 1, it is connected to C8PS. The negative input is connected to the center of built-in BEMF resistors. The output results are transferred to CMP_SR[CMP8OUT].
	10	00	CMP6/7/8 work simultaneously, as shown in Figure 33-20. The positive inputs of these comparators are connected to C6P, C7P and C8P respectively, and the negative inputs are connected to C6M, C7M and C8M respectively. The output results are transferred to CMP_SR[CMP6OUT], CMP_SR[CMP7OUT] and CMP_SR[CMP8OUT] respectively.
		01	Only CMP6 works. The positive input is connected to C6P, and the negative input to C6M. The output results are transferred to CMP_SR[CMP6OUT].
		10	Only CMP7 works. The positive input is connected to C7P, and the negative input to C7M. The output results are transferred to CMP_SR[CMP7OUT].
		11	Only CMP8 works. The positive input is connected to C8P, and the negative input to C8M. The output results are transferred to CMP_SR[CMP8OUT].
	11	00	CMP6/7 work simultaneously, as shown in Figure 33-21. The positive inputs are connected to C6P and C7PS respectively, and the negative inputs to C6M. The outputs results are transferred to CMP_SR[CMP6OUT] and CMP_SR[CMP7OUT] respectively.
		01	Only CMP6 works. The positive input is connected to C6P, and the negative input to C6M. The output results are transferred to CMP_SR[CMP6OUT].

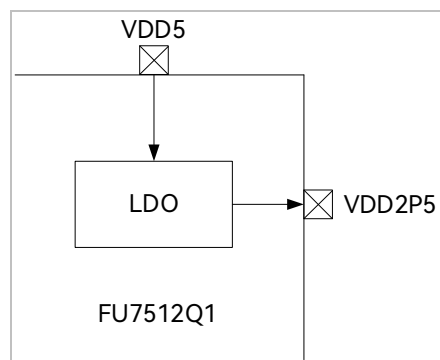
			10	Only CMP7 works. The positive input is connected to C7PS, and the negative input to C7M. The output results are transferred to CMP_SR[CMP7OUT].
			11	Reserved
[2:1]	CMP6CSEL	CMP6/7/8 Rolling Speed Selection 00: Normal Speed 01: Fast Speed 10: Slow Speed 11: Low Speed		
[0]	CMP6EN	CMP6/7/8 Enable 0: Disable 1: Enable		

34 Power Supply

34.1 LDO

34.1.1 FU7512Q1 LDO Module

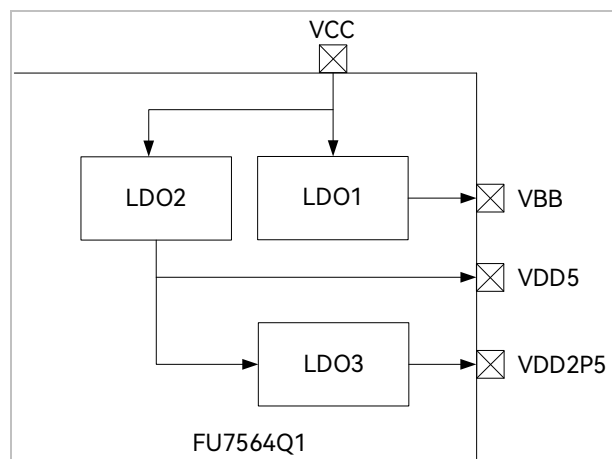
Figure 34-1 LDO Module of FU7512Q1



The input and output pins of the LDO module in FU7512Q1 are shown in Figure 34-1. The LDO module converts the input supply voltage to 2.5V (VDD2P5) to power internal circuitry of the chip.

34.1.2 FU7564Q1 LDO Module

Figure 34-2 LDO Module of FU7564Q1

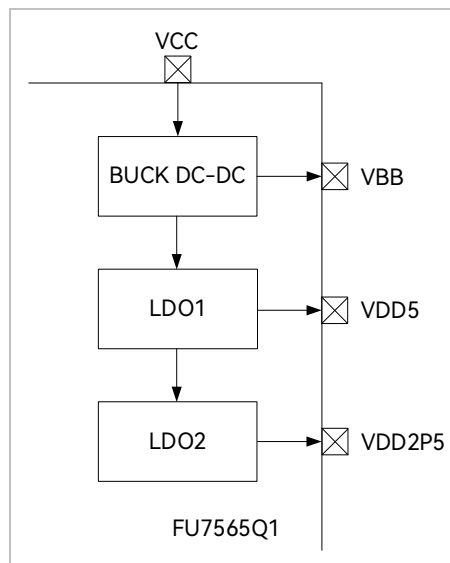


The input and output pins of the LDO modules in FU7564Q1 are shown in Figure 34-2. LDO1 and LDO2 convert the input supply voltage to 11V (VBB) and 5V (VDD5) respectively to power internal circuitry of the chip. LDO3 further steps down the output voltage of LDO2 to 2.5V (VDD2P5) to power internal circuitry of the chip.

34.1.3 FU7565Q1 LDO Module

The input and output pins of the LDO modules in FU7565Q1 are shown in Figure 34-3. LDO1 steps down the buck DC-DC converter output (12 V) to 5V (VDD5) to power internal circuitry of the chip; LDO2 further steps down the output voltage of LDO1 to 2.5V (VDD2P5) to power internal circuitry of the chip.

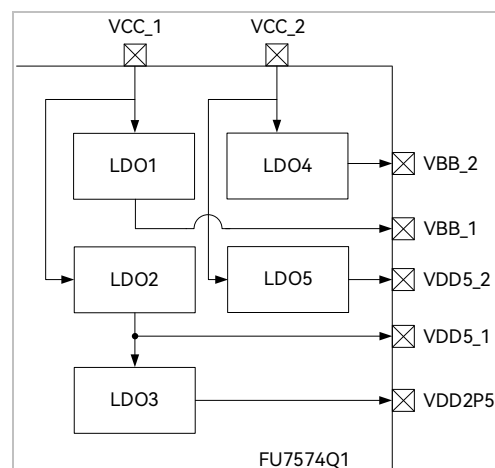
Figure 34-3 LDO Module of FU7565Q1



34.1.4 FU7574Q1 LDO Module

The input and output pins of the LDO modules in FU7574Q1 are shown in Figure 34-4. LDO1 and LDO4 step down the input supply voltage to 11V (VBB_1 and VBB_2); LDO2 and LDO5 step down the input supply voltage to 5V (VDD5_1 and VDD5_2) to power internal circuitry of the chip; LDO3 further steps down the output voltage of LDO2 to 2.5V (VDD2P5) to power internal circuitry of the chip.

Figure 34-4 LDO Module of FU7574Q1



34.2 Buck DC-DC Converter (FU7565Q1)

34.2.1 Buck DC-DC Converter Overview

FU7565Q1 integrates a Buck DC-DC converter that steps down the input supply voltage to 12V (VBB) for internal chip power. A 0.1 μ F capacitor must be connected between the SW pin and CP1_1, a 100 μ H inductor in series between SW and VBB, and a 1 μ F capacitor from VBB to ground.

This converter is controlled by fixed-frequency peak current combined with voltage feedback. Its key features include:

- > Slope compensation

Built-in slope compensation prevents subharmonic oscillation at high duty cycles.

- > Switching frequency and spread-spectrum control

An internal oscillator allows clock frequency configuration via VTLV_R[OSC2_FSEL] to meet different application needs. Spread-spectrum mode can be selected via VTHW_R[OSC2_SS] to reduce electromagnetic interference (EMI).

- > Soft-start

Integrated soft-start circuitry provides a typical start-up time of about 2ms.

- > Short-circuit protection

When a VBB short-circuit fault is detected, the system starts a timer. If the VBB voltage does not recover after 2048 μ s, the converter disables its output and enters hiccup mode. After 14336 μ s, the system automatically attempts to restart the converter. If the short-circuit fault persists, it re-enters hiccup mode until VBB returns to the normal operating range.

34.3 Charge Pump (FU7564Q1)

FU7564Q1 integrates a charge pump circuit that uses an external capacitor to generate a regulated output voltage $V_{CP} = V_{CC} + V_{BB}$. This circuit, which operates independently of the MOSFET's switching pulses, is mainly responsible for driving the gate of the high-side reverse-blocking MOSFET. By keeping VDH and VCC within the same voltage range, the charge pump ensures sufficient gate drive voltage for both the high-side reverse-blocking MOSFET and the upper high-side MOSFET.

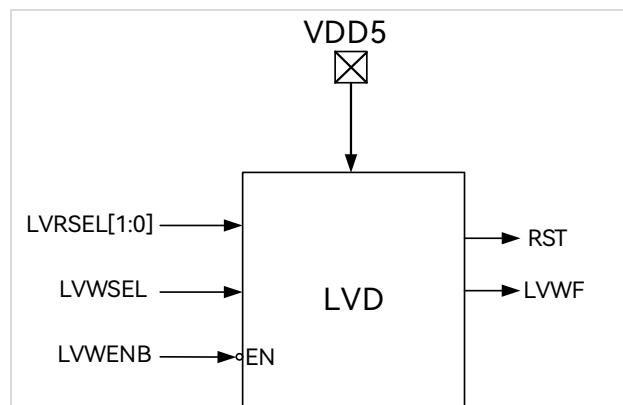
34.4 Low Voltage Detection (LVD)

34.4.1 LVD Introduction

The low voltage detection includes low voltage warning and low voltage reset.

34.4.2 LVD Operations

Figure 34-5 LVD Module

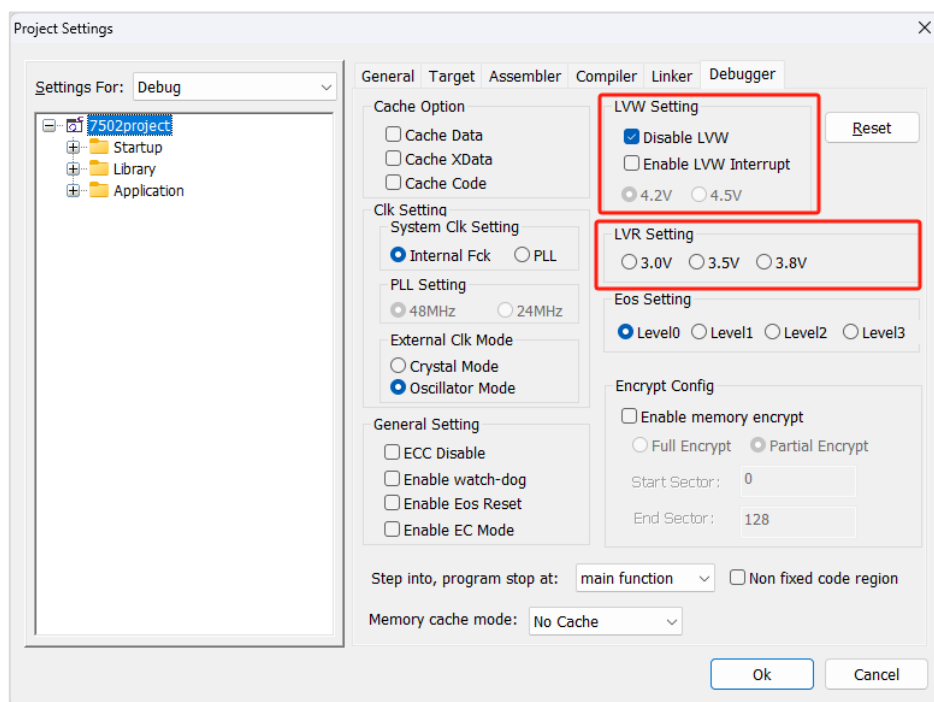


The operating instructions for LVD are as follows:

- > LV warning and LV reset are always enabled by default
- > 4.2/4.5V can be selected for LV warning threshold. When the interrupt feature is enabled, an interrupt is triggered if VDD5 voltage is lower than the LV warning threshold
- > 3.0/3.5/3.8V can be selected for the LV reset threshold. The chip resets when VDD5 voltage is lower than the LV reset voltage threshold. Low-voltage warning threshold, interrupt settings and low-voltage reset threshold are configured through the debug tool, as shown in Figure 34-6.

LVR Setting sets low-voltage reset threshold, Enable LVW Interrupt enables or disables low-voltage interrupt, and LVW Setting sets low-voltage warning threshold.

Figure 34-6 Configurations of LV Warning Threshold, LV Interrupt and LV Reset Threshold



34.5 LVD Registers

34.5.1 LVSR (CSR: 0x408)

[illegible]

Bit	Name	Description
[31:2]	RSV	Reserved
[1]	LVWF	VDD5 Low Voltage (LV) Flag This bit indicates whether the chip is in the low voltage state. 0: The chip is not in the LV warning state. 1: The chip is in the LV warning state.
[0]	LVWIF	VDD5 LV Interrupt Flag Read: 0: No interrupt pending

		1: Interrupt pending Write: 0: This bit is cleared to “0” 1: No effect  Note: This bit is not set to “1” by hardware when LVD interrupt is disabled

35 Flash

35.1 Flash Introduction

The chip provides 64kB on-chip Flash space and 8kB ECC space. It supports sector/page/chip erasure, sector/page/chip pre-programming, byte programming and so on. When the Flash is being programmed, the CPU pauses instruction fetching until the Flash programming is completed.

Main features:

- > 8k cells in total, each with 8B data space and 1B ECC space
- > 128 sectors in total, each with 64 cells that is 512B
- > 16 pages in total, each with 8 sectors that is 4kB
- > Last sector (0xFE00 ~ 0xFFFF) cannot be erased at any time
- > 120ms ~ 210ms for sector/page/chip erase
- > Operate Flash by store commands
- > ECC is provided to check the data and perform 1-bit error correction
- > Flash programming operations include:
 - >> Up to 8B for programming. ECC bits can be automatically or manually calculated.
 - >> Erase based on sectors
 - >> Flash maintenance mode based on sectors
 - >> Erase based on pages
 - >> Flash maintenance mode based on pages
 - >> Erase based on chips
 - >> Flash maintenance mode based on chips

35.2 Flash Operations

Flash shall be operated according to the following steps:

1. Unlock Flash memory: The Flash software programming feature is activated after “0x5A” and

“0x1F” are written to register FLA_KEY in sequence. If the sequence is incorrect or other values are written, Flash space is frozen until the next reset. After unlocking, any write to the FLA_CR register causes the FLA_KEY to be locked again

2. Preparations before programming: Stop the watchdog timer to prevent a timer reset
3. Configure programming mode: Configure FLA_CR[FLAEN] = 1 to enable programming and then set associated bits for Flash operations, see Table 35-1 for more details

Table 35-1 Flash Operations and Configurations

FLA_CR Configuration Bit	Flash Operations
FLAEN	Programming ECC bit by the 8 bytes of data. The ECC bit is calculated and programmed based on the 8-byte data.
FLAEN FLASIZE FLAECC	ECC Bits Programming. ECC bits are calculated and programmed based on the existing data in Flash.
FLAEN FLASIZE	Single-byte Data Programming
FLAEN FLAERS	Sector Erasure
FLAEN FLAPRE	Sector Pre-programming
FLAEN FLAPRE FLAMARGIN1	Sector Maintenance Mode
FLAEN FLAERS FLAPAGE	Page Erasure
FLAEN FLAPRE FLAPAGE	Page Pre-programming
FLAEN FLAPRE FLAPAGE FLAMARGIN1	Page Check Mode
FLAEN FLAERS FLACHIP	Chip Erasure
FLAEN FLAPRE FLACHIP	Chip Pre-programming
FLAEN FLAPRE FLACHIP FLAMARGIN1	Chip Maintenance Mode

**Note:**

- > During program execution, any modifications to the Flash memory change the CRC accordingly.
- > ECC can be accessed via the address starting at 0x01000000, where the ECC address is calculated as 0x01000000 plus the target Flash cell address.

35.3 ECC Verification

35.3.1 Introduction

The ECC verification module enhances data integrity in Flash memory by generating an 8-bit ECC checksum for each 64-bit data block. It can correct single-bit errors and detect double-bit errors.

The module also includes an error counter that accumulates ECC errors. Once the count exceeds the preset threshold, it generates an interrupt to signal a multiple-bit error event.

35.4 Flash Registers

35.4.1 FLA_CR (CSR: 0x4E1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																		FLAM0ERR	FLAERR	RSV			FLAMARGIN1	RSV	FLAECC	FLASIZE	FLACHIP	FLAPAGE	FLAPRE	FLAERS	FLAEN
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Bit	Name	Description
[31:14]	RSV	Reserved
[13]	FLAM0ERR	Flash Margin0 Error Flag 0: No Margin0 error pending 1: Margin0 error pending
[12]	FLAERR	Flash Programming/Pre-programming Error Flag 0: No flash programming/pre-programming error pending 1: Flash programming/pre-programming error pending
[11:9]	RSV	Reserved
[8]	FLAMARGIN1	Flash Margin1 Test Mode Enable 0: Disable 1: Enable
[7]	RSV	Reserved
[6]	FLAECC	Flash ECC Bytes Programming Enable 0: Disable 1: Enable

		Note: This bit works only when FLA_CR[FLAEN] = 1
[5]	FLASIZE	Flash Programming Data Byte Size 0: 8B 1: 1B Note: This bit works only when FLA_CR[FLAEN] = 1
[4]	FLACHIP	Flash Chip Operation Enable 0: Disable 1: Enable Note: This bit works only when FLA_CR[FLAEN] = 1
[3]	FLAPAGE	Flash Page Operation Enable 0: Disable 1: Enable Note: This bit works only when FLA_CR[FLAEN] = 1
[2]	FLAPRE	Flash Pre-programming Enable 0: Disable 1: Enable Note: This bit works only when FLA_CR[FLAEN] = 1
[1]	FLAERS	Flash Erasure Enable 0: Disable 1: Enable Note: This bit works only when FLA_CR[FLAEN] = 1
[0]	FLAEN	Flash Programming Enable 0: Disable 1: Enable

35.4.2 FLA_KEY (CSR: 0x4E0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																														FLAKSTA	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Description
[31:2]	RSV	Reserved
[1:0]	FLAKSTA	Read: Flash unlock status 00: Locked 01: 0x5A has been written, awaiting 0x1F 10: Frozen 11: Unlocked

35.4.3 FLA_ECSR (CSR: 0x4E2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV										LMERR_CEN	LERR_CEN	ERR_CNTR				ERR_ARR				MERR	MERR_IE	CMERR	CMERR_IE	CERR	CERR_IE	LMERR	LMERR_IE	LERR	LERR_IE		
-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw0	rw	r	r	rw0	rw	rw0	rw
-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:22]	RSV	Reserved
[21]	LMERR_CEN	Multiple-bit ECC Error Counting Enable during When Fetching Data from Flash 0: Disable 1: Enable
[20]	LERR_CEN	Single-bit ECC Error Counting Enable When Fetching Data from Flash 0: Disable 1: Enable
[19:15]	ERR_CNTR	ECC Error Trigger Count

[14:10]	ERR_ARR	Multiple ECC Error Interrupt Threshold This value sets the accumulated error count for the multiple ECC error interrupt.
[9]	MERR	ECC Accumulated Error Interrupt Enable Flag When the interrupt is enabled, ERR_CNTR counts the ECC errors. When the interrupt is disabled, ERR_CNTR is always 0. 0: Disable 1: Enable
[8]	MERR_IE	ECC Accumulated Error Interrupt Enable When the interrupt is enabled, ERR_CNTR counts the ECC errors. When the interrupt is disabled, ERR_CNTR is always 0. 0: Disable 1: Enable
[7]	CMERR	Multiple-bit ECC Error Interrupt Flag When Fetching Commands from Flash 0: No interrupt 1: Interrupt
[6]	CMERR_IE	Multiple-bit ECC Error Interrupt Enable When Fetching Commands from Flash 0: Disable 1: Enable
[5]	CERR	Single-bit ECC Error Interrupt Enable Flag When Fetching Commands from Flash 0: No interrupt 1: Interrupt
[4]	CERR_IE	Single-bit ECC Error Interrupt Enable When Fetching Commands from Flash 0: Disable 1: Enable
[3]	LMERR	Multiple-bit ECC Error Interrupt Enable Flag When Fetching Data from Flash 0: No interrupt 1: Interrupt
[2]	LMERR_IE	Multiple-bit ECC Error Interrupt Enable When Fetching Data from Flash 0: Disable 1: Enable
[1]	LERR	Single-bit ECC Error Interrupt Enable Flag When Fetching Data from Flash 0: No interrupt 1: Interrupt
[0]	LERR_IE	Single-bit ECC Error Interrupt Enable When Fetching Data from Flash 0: Disable 1: Enable

35.4.4 FLA_EEADR (CSR: 0x4E3)

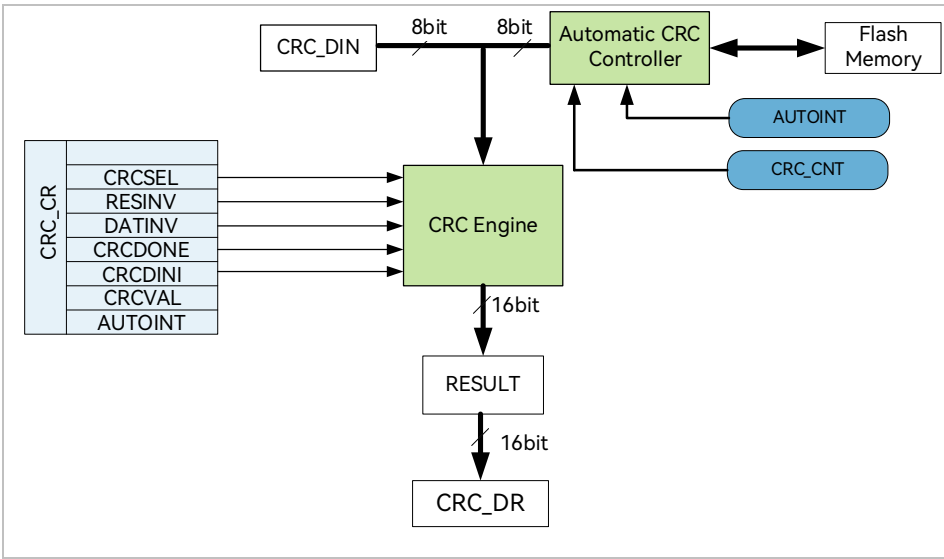
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																FLA_EEADR											RSV				
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-

位	名称	描述
[31:16]	RSV	Reserved
[15:3]	FLA_EEADR	ECC Error Address
[2:0]	RSV	Reserved

36 CRC

36.1 CRC Functional Block Diagram

Figure 36-1 CRC Functional Block Diagram



CRC module outputs the result of CRC calculation for any 8-bit data based on a fixed polynomial. As shown in Figure 36-1, CRC receives the 8-bit data from CRC_DIN and sends the 16-bit result to the internal register after the calculation is completed. The result can be indirectly accessed through CRC_DR register.

36.2 CRC16 Polynomials

The chip supports two kinds of CRC polynomials: $x^{16}+x^{15}+x^2+1$ (based on CRC16-CCITT-FALSE) and $x^{16}+x^{15}+x^2+1$ (based on CRC16).

Table 36-1 CRC Criteria and Polynomials

CRC Criteria	CRC Polynomial	Hexadecimal Representation
CRC16-CCITT-FALSE	$x^{16} + x^{12} + x^5 + 1$	0x1021
CRC16-MODBUS	$x^{16} + x^{15} + x^2 + 1$	0x8005

36.3 CRC16 Logic Diagram

The schematic diagram of CRC16 is shown in Figure 36-2. The chip implementation is based on parallel algorithm. For each input byte, MCU calculates the results within one system clock cycle.

Figure 36-2 CRC16-CCITT-FALSE Schematic Diagram

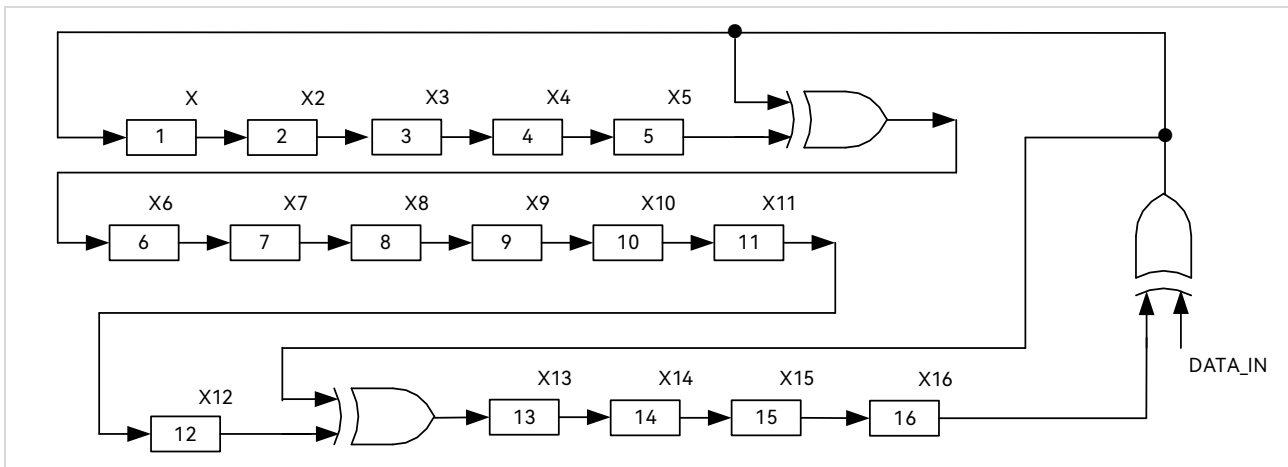
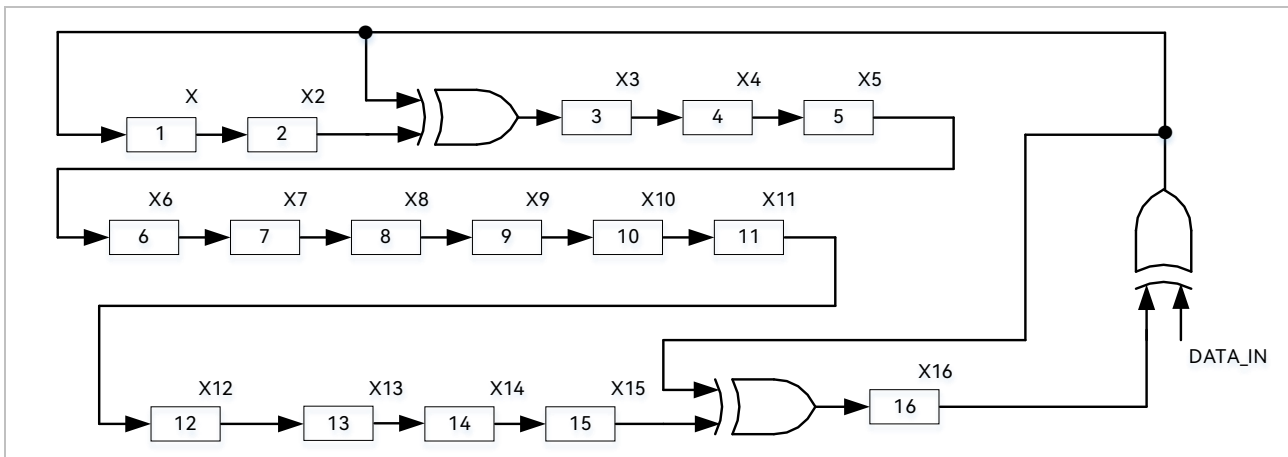


Figure 36-3 CRC16-MODBUS Schematic Diagram



36.4 CRC Operations

36.4.1 CRC Calculation of Single Byte

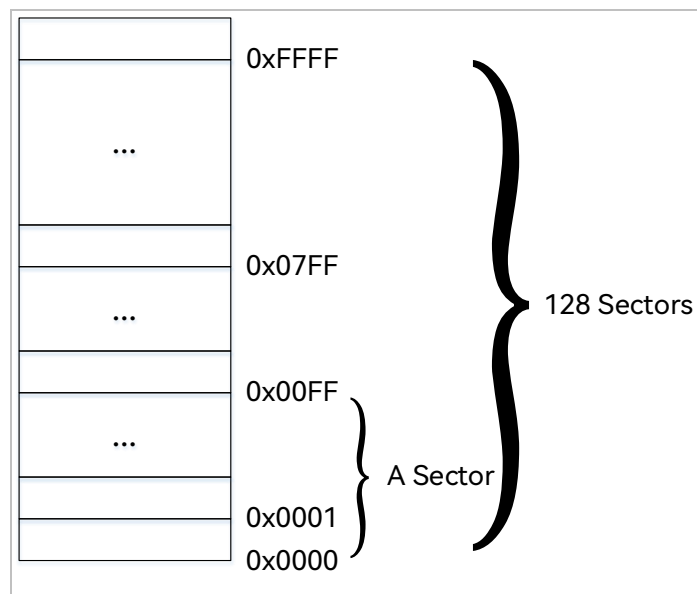
CRC of a single byte is calculated as follows:

1. Initialize CRC_DR with two options: Configure CRC_CR[CRCVAL] and set CRC_CR[CRCDINI] to "1", with an initial value of 0x0000 or 0xFFFF;
2. Write data to CRC_DIN, and the CRC calculation is completed in the next clock cycle;
3. Read CRC results: The software reads the result and outputs it to the register CRC_DR.

36.4.2 CRC Calculation of ROM Sector

1. Initialize CRC_DR in the same way as that of single-byte CRC calculation;
2. Configure CRC_BEG to define starting sector of the ROM to be calculated;
3. Configure CRC_CNT to set the offset from the starting sector to the ending sector;
4. Write “1” to CRC_CR[AUTOINT] and keep other bits unchanged. The calculation starts automatically;
5. Read CRC results when CRC_CR[CRCDONE] = 1.
6. As shown in Figure 36–4, ROM contains 64k bytes and is divided into 128 sectors, numbered from sector 0 to sector 127. Each sector contains 512 bytes. For CRC calculation of sectors, CRC_BEG (starting sector) can be any value falling between 0 and 127, including 0 and 127. CRC_CNT (total number of sectors to be calculated) can be any value between 0 and 127, including 0 and 127.

Figure 36–4 ROM Sectors



As CRC_BEG increases, CRC_CNT decreases accordingly and $\text{CRC\_BEG} + \text{CRC\_CNT} \leq 127$.

36.4.3 CRC Calculation of DMA

CRC of a continuous area of data of specified address via DMA is calculated as follows:

1. Initialize CRC_DR in the same way as that of single-byte CRC calculation;
2. Configure DMAx_CR to configure CRC mode and enable DMA;
3. Configure DMAx_BA to set origin data base address;
4. Configure DMAx_LEN to set the length of data;
5. Write “1” to DMAx_CR[DMABSY] and the calculation starts automatically;
6. Read the CRC results when DMAx_CR[DMABSY] = 0.

36.5 CRC Registers

36.5.1 CRC_DIN (CSR: 0x1D8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								CRC_DIN							
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	≧	≧	≧	≧	≧	≧	≧	≧
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	CRC_DIN	CRC Input Data Each time a data frame is written to this register, CRC module automatically calculates a new CRC result based on the existing CRC result, and overwrites the original one.  Note: It is a virtual register, so the written data is not saved. 0x00 is returned when the address is accessed.

36.5.2 CRC_CR (CSR: 0x1D9)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																								RESINV	DATINV	CRCSEL	CRCDONE	CRCDINI	CRCVAL	AUTOINT	RSV
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r/w	r/w	r/w	r/1	w/1	r/w	w/1	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	1	0	0	0	-

Bit	Name	Description
[31:8]	RSV	Reserved
[7]	RESINV	CRC Output Reversed 0: CRC output is normal. 1: CRC output is reversed.
[6]	DATINV	CRC Input Reversed 0: CRC input is normal. 1: CRC input is reversed.
[5]	CRCSEL	CRC Polynomial Selection 0: CRC16-CCITT-FALSE 1: CRC16
[4]	CRCDONE	CRC Sector Calculation Completed Flag During the calculation, this bit is automatically set to “0” and the software program stops. In other cases, this bit is automatically set to “1” by the hardware, so the software always returns “1” when reading this bit.
[3]	CRCDINI	CRC Result Initialization Trigger 0: No effect 1: CRC result initialization is triggered.
[2]	CRCVAL	CRC Result Initialization Selection 0: CRC result is initialized to 0x0000. 1: CRC result is initialized to 0xFFFF.
[1]	AUTOINT	CRC Sector Calculation Launch 0: No effect 1: Launch CRC Batch calculation See section CRC Calculation of ROM Sector.
[0]	RSV	Reserved

**Note:**

CRC_CR[AUTOINT] is set to “0” to perform single-byte CRC checksum.

36.5.3 CRC_DR (CSR: 0x1DA)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CRC_DR															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:16]	RSV	Reserved
[15:0]	CRC_DR	CRC Result Output

36.5.4 CRC_BEG (CSR: 0x1DB)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CRC_BEG															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description
[31:8]	RSV	Reserved
[7:0]	CRC_BEG	First ROM Sector Pending Automatic CRC Calculation Example: If CRC_BEG is set to “1”, CRC calculation starts from location $1 \times 256 = 256$, or rather from the first byte of sector 2.

36.5.5 CRC_CNT (CSR: 0x1DC)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																CRC_CNT															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	w	w	w	w	w	w	w	w
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

Bit	Name	Description

[31:8]	RSV	Reserved
[7:0]	CRC_CNT	Offset of Sector Pending Automatic CRC Calculation This bit defines the offset of ROM sector for CRC calculation and determines the last sector pending CRC calculation.

37 Sleep Mode

37.1 Introduction

The chip operates in three modes: normal mode, standby mode, and sleep mode. These modes are selected by setting PCON[IDLE] and PCON[STOP].

The following conditions shall be ensured when the chip is in sleep mode:

- > Configure CK_CR[DRV1CKEN] = 0 and CK_CR[DRV2CKEN] = 0;
- > Configure MIE[IRQ_EN] = 0;
- > Configure PCON[STOP] = 1;
- > Besides setting the above registers, a statement asm volatile ("WFI") shall be added. The statement is RISC-V defined instruction for sleep mode. When receiving the WFI instruction, the processor stops executing the instruction stream and enters sleep mode.

Operating states of the module under different power modes are summarized in the table below.

Table 37-1 Power Consumption Modes

Power Mode	Descriptions	Wakeup Source	Power Consumption and Performance
Normal	All modules work at full speed except for peripherals that are disabled	NA	High power consumption with best performance
Standby	CPU clock stops and other functional modules are either enabled or disabled depending on their control bit setting. The watchdog timer stops.	Any interrupt; Reset/Debug on external interrupt	Low power consumption with flexible performance
Sleep	Flash deep sleep. The analog fast clock circuit is disconnected and MCU software shall ensure that ADC, FOC, and driver modules are disabled before the chip enters the sleep mode. The watchdog timer is disabled.	External interrupt; RTC interrupt; Reset/Debug on external interrupt; Level changes on PA9 (for FU7512Q1); Low level input on LIN and level changes on MON_HVx (for FU7564Q1/FU7565Q1/FU7574Q1)	Extremely low power consumption with flexible performance

Power Mode	Descriptions	Wakeup Source	Power Consumption and Performance
	Low-power sleep mode (for FU7564Q1/FU7565Q1/FU7574Q1). The chip enters low-power sleep mode when SLPF_R [SLP_FORCE] = 1	Low level input on LIN and level changes on MON_HVx	Lowest power consumption with flexible performance

37.2 Low-power Sleep Mode (FU7564Q1/FU7565Q1/FU7574Q1)

The chip enters low-power sleep mode when SLPF_R[SLP_FORCE] = 1. In this mode, the VCC_x supply current reduces to the IVCCS quiescent level, and VDD5_x voltage drops to 0.

- > For FU7564Q1/FU7565Q1, the chip can exit low-power sleep mode only when the LIN input level is low or the MON_HV1 input level changes.
- > For FU7574Q1, the chip can exit low-power sleep mode only when either (the LIN input level is low and the MON_HV2 input level changes) or (both MON_HV1 and MON_HV2 input levels change).

Upon wake-up, the chip clears all existing fault conditions and resets all serial registers to their power-on defaults. This initialization sequence takes about 8ms. The chip then returns to normal operation where the general fault flags become valid. The 6N pre-driverx outputs are also enabled once VBB_x exceeds the UVLO release voltage V_{BBUVR} . Note that transient conditions during wake-up may affect the fault flags status and the initial values read from diagnostic and status registers. Setting SLPF_R[FAULT_CLR] = 1 clears the fault flags.

Please contact us for more details on low-power sleep mode.

37.3 Sleep Mode Registers

37.3.1 PCON(CSR: 0x4D2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV																STOP		IDLE													
																rw		rw													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Bit	Name	Description
[31:2]	RSV	Reserved
[1]	STOP	A write of “1” makes the chip enter the sleep mode. This bit is automatically cleared to “0” by hardware after wakeup
[0]	IDLE	A write of “1” makes the chip enter the standby mode. This bit is automatically cleared to “0” by hardware after wakeup

37.4 Low-power Sleep Mode Registers (FU7564Q1/FU7565Q1/FU7574Q1)

37.4.1 SLPF_R (0x02)

7	6	5	4	3	2	1	0
RSV			SLP_FORCE	REBOOT	VDS_CLR	FAULT_CLR	ANA_RDY
-	-	-	rw	w1	w1	w1	r
-	-	-	0	0	0	0	0

Bit	Name	Description
[7:5]	RSV	Reserved
[4]	SLP_FORCE	Writing “1” enters low-power sleep mode; the bit is automatically cleared to “0” by hardware upon wake-up
[3]	REBOOT	See descriptions in section SLPF_R (0x02) of chapter ME
[2]	VDS_CLR	See descriptions in section SLPF_R (0x02) of chapter ME
[1]	FAULT_CLR	Writing “1” clears the fault flag
[0]	ANA_RDY	See descriptions in section SLPF_R (0x02) of chapter ME

38 Code Protection

38.1 Introduction

The chip supports Flash space encryption to protect your software intellectual property and avoid unauthorized access. When Flash memory is encrypted, the data inside cannot be read, and data consistency can be evaluated by CRC module only.

38.2 Operating Instructions

Figure 38-1 Code Protection Configurations

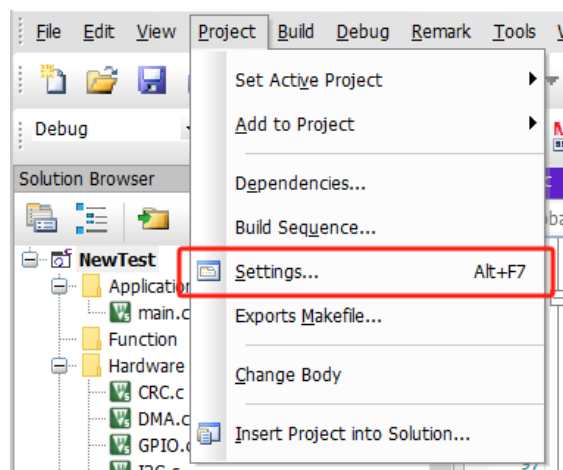
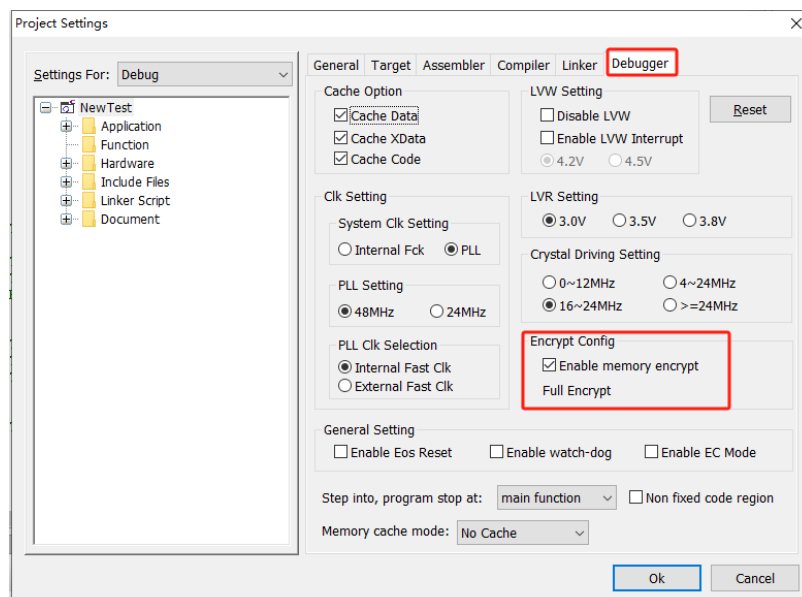


Figure 38-2 Full Code Protection Mode



Operation steps are as follows:

1. Start IDE, select Project -> Settings, and then choose Debugger tab to proceed with the setting, as shown in Figure 38-1;
2. Select the options as shown in Figure 38-2, and click OK. Then click Rebuild to compile the project and download it. Get the BIN file and program it to Flash.

39 Exception Handling

39.1 Trap Overview

In the RISC-V architecture, exceptions and interrupts are collectively referred to as traps, which are the core mechanisms for the processor to respond to internal errors or external events. Traps rely on a set of dedicated control and status registers (CSRs) that work together to capture exceptions, save context, jump to the handler, and return.

Traps in RISC-V fall into two categories:

- Synchronous exceptions: triggered by the execution of the current instruction (e.g., illegal instruction, ebreak)
- Asynchronous interrupts: triggered by external events (e.g., timer interrupts, external device interrupts, software interrupts) and can occur at any instruction boundary.

Both share the same handling mechanism but can be distinguished by the most significant bit of the MCAUSE register: 0 indicates an exception, 1 indicates an interrupt.

39.2 Exception Handling Flow

1. Trap triggered: The processor detects an exception or interrupt.
2. Context saving:
 - Read the cause code from MCAUSE.
 - Disable global interrupts.
3. Handler execution: The OS or firmware executes the corresponding logic based on the cause code.
4. Return: Use the mret instruction to resume execution of the program stopped by the exception and interrupt.

40 Revision History

Rev.	Description	Date	Prepared By
V0.1	Preliminary datasheet	2025/06/10	Eric Deng
V0.2	- Added descriptions on FU7564Q1 in section 1 System Introduction; - Added sections 2 Pin definitions ~ 5 Electrical Characteristics;	2025/10/31	Eric Deng
V0.3	- Added descriptions on FU7512Q1; - Added sections 6 Reset Control ~ 38 Code Protection; - Added ECC for Flash in section 1.1 Features, removed “QEP decoding” and “rotation/speed detection of step motor” from Timer6 and modified the number of ADC1 channels for FU7564Q1 from 10 to 12 and that of ADC2 channels from 6 to 8; - Modified FOC as 2*FOC, and added Charge Pump, MON, LIN Transceiver modules, AD1_3/11 channels and AD2_1/3 channels in Figure 1-2 Functional Block Diagram of FU7564Q1; - Added the registers SLPF_R(0x02), STAU_R(0x07), STAV_R(0x08) and STAW_R(0x09) in Table 1-6 6N Pre-driver Register Address Mapping, and modified the registers I2C_R(0x83) and LIN_R(0x85) as RSV; - Added “When VCC ≥ 12V, it delivers at least 30mA of additional load capability” to the descriptions on VBB and VDD5 pins in section 2.3 FU7564Q1 QFN56 Pins; - Modified the number of the ADC channels for FU7564Q1 in section 4 Ordering Information from 16 to 20; - Updated the minimum value of High-side Floating Offset Voltage for Phase U/V/W V_{SU}, V_{SV}, V_{SW} in Table 5-2 Absolute Maximum Ratings of FU7564Q1 from -0.3V to -10V; - Modified typical value of I_{VCC} Standby Current in Table 5 4 Global Electrical Characteristics of FU7564Q1 from 5mA to 8mA.	2025/12/19	Eric Deng
V0.4	- Added the test condition for “VCC to VSS Voltage” in Table 5-2 Absolute Maximum Ratings of FU7564Q1 and added the parameters “VCC to VSS Voltage (Spike Duration < 60) and VCC to VSS Voltage (Spike Duration < 500ms); - Modified the baud rate formula in section 11.4.4 UTx_BAUD (CSR: 0x0143/0x153) ($x = 1/2$); - Modified TIMx_CR0[TxINM] as TIMx_CR0[TxFE] in section 17 Timer3/4/7/8; - Modified the option “000/111: Invalid” for [2:0] CBA_MTSAM in section 18.16.2.13 DRVx_FCR7 (CSR: 0x54F/0x58F) ($x = 1/2$) as “000/111: Reserved”; - Modified “When CMP_CR0[CMP3IM] = 11, the OCP output is	2025/12/31	Eric Deng

Rev.	Description	Date	Prepared By
	generated on the raising edge of CMP3..." in section 33.1.1.1 Over-current Protection (OCP) of Master Motor as "When CMP_CR0[CMP3IM] = 01, the OCP output is generated on the raising edge of CMP3..."; 6. Modified "When CMP_CR4[CMP9IM] = 11, the OCP output is generated on the raising edge of CMP9..." in section 33.1.2.1 Over-current Protection (OCP) of Slave Motor as "When CMP_CR4[CMP9IM] = 01, the OCP output is generated on the raising edge of CMP9..."; 7. Modified PC13 as PB13 in section 33.1.3 CMP4; 8. Modified some descriptions.		
V1.0	1. Added descriptions about FU7574Q1; 2. Added CAN, ECC, LIN, PFC, PMSM, PRAM, XRAM, and XSFR, deleted LVDS, and modified "Adaptive Flux Observer" as "All-order Flux Observer" in chapter Abbreviations. 3. Added "System clock up to 48MHz", supplemented SPI description for FU7564Q1 with "supporting only 3-wire mode", and added "supporting 12V LIN applications" for FU7564Q1 LIN in section 1.1 Features. 4. Updated Figure 1-2 Functional Block Diagram of FU7564Q1 and added pin COM. 5. Renamed VSS (pin 16) of FU7564Q1 to COM_1, with description changed to "6N pre-driver1 ground"; updated VSS (pin 19) description to "MCU ground". 6. Standardized the following FU7564Q1 pin names: VDH/VBU/HU/VSU/VBV/HV/VSV/VBW/HW/VSW/LU/LV/LW/LSS/FAULTNS/CP1/CP2/VCP/COM to VDH1/VBU1/HU1/VSU1/VBV1/HV1/VSV1/VBW1/HW1/VSW1/LU1/LV1/LW1/LSS1/FAULTN1S/CP1/CP2/VCP/CP1_1/CP2_1/VCP_1/COM_1; 7. Added section 2.7 FU7512_64_74Q1 Functions and Pins Comparison. 8. Updated package drawings and dimensions for FU7512Q1 and FU7564Q1. 9. Added LIN transceiver, charge pump, and PFC in chapter 4 Ordering Information; changed "Frequency" to "System Clock". 10. Changed LIN pin voltage V_{LIN} minimum from $-0.3V$ to $-40V$ and added condition "LIN to VCC/VSS" in section 5.1.2 FU7564Q1 Absolute Maximum Ratings. 11. Deleted condition "PA_OE[6:9] = 1, PA[6:9] = 0" from I_{VCC} sleep current in section 5.2.2 FU7564Q1 Global Electrical Characteristics. 12. Changed PC[0:5] to PC[3:5] in Note [3] in section 5.3.1 FU7512Q1 GPIO Electrical Characteristics.	2026/07/17	Joe Luo

Rev.	Description	Date	Prepared By
	13. Renamed section 5.10 "OSC Electrical Characteristics" to "Clock Electrical Characteristics"; deleted the condition "PLL disabled" from the system clock frequency parameter and added condition "CCFG3[PLLFSEL] = 1/0". 14. Added section 7.5.2 MTVEC (CSR: 0x305) in section 7.5 Interrupt Registers. 15. Added section 13.7 LIN Transceiver (FU7564Q1/FU7574Q1). 16. Added the condition for periodic automatic bootstrap capacitor charging via charge pump VCP_x in section 18.2.2.2 Bootstrap Charging Management. 17. Updated the NFOCx_POWER calculation formula in section 18.7 Power Calculation: swapped NFOCx_POWK1 and NFOCx_POWK2 positions. 18. Updated the NFOCx_FGBASE calculation formula in section 18.14.2 FG Interrupt: changed the duplicate NFOCx_FBASE to BASE_FREQ, and added a description: "BASE_FREQ is the electrical frequency (in Hz) corresponding to the maximum motor speed." 19. Updated the Note description for [2] TRIG_MD in section 18.16.2.1 ME_CR (CSR: 0x500). 20. Changed "Dual-shunt 2-time sampling" to "Dual-shunt dual-ADC sampling" in section 18.16.2.6 DRVx_FCR0 (CSR: 0x548/0x588). 21. Renamed the following: UAVG to PFC_UAVG, UAC to PFC_UAC, IAC to PFC_IACx, IAC1 to PFC_IAC1, IAC2 to PFC_IAC2, and UCTHR to PFC_CR1[UCTHR]. 22. Changed description from "CMP0/7/8 PWM ON/OFF sampling signal output" to "CMP6/7/8 PWM ON/OFF sampling signal output" for bits [14:10] DBGSEL2 and [9:5] DBGSEL1 in section 33.2.8 CMP_DBR (CSR: 0x607). 23. Changed Flash total sectors from 256 to 128; changed cells per sector from 32 to 64; changed bytes per sector from 256 to 512. 24. Changed sectors per page from 16 to 8; changed last sector address range from 0xFF00–0xFFFF to 0xFE00–0xFFFF. 25. Deleted entries "FLAEN FLAECCMANUAL" and "FLAEN FLAECC FLAECCMANUAL" in Table 35-1 Flash Operations and Configurations; deleted "In cfg_unlock mode, single byte programming can be used to manually modify the ECC byte (ensure the lower 3 bits are 0)." in Note. 26. Changed bit [15] FLAERR to [12] and bit [12] FLAM0ERR to [13] in section 35.4.1 FLA_CR (CSR: 0x4E1). 27. Renamed 35.4.3 FLA_ECC_CR (CSR:0x4F0) to 35.4.3 FLA_ECSR		

Rev.	Description	Date	Prepared By
	(CSR: 0x4E2), and updated all register descriptions; renamed 35.4.4 FLA_ECC_SR (CSR: 0x4F1) to 35.4.4 FLA_EEADR (CSR: 0x4E3), and updated all register descriptions. 28. Added chapter 39 Exception Handling.		
V1.1	1. Added descriptions about registers I2C_R and DIS_R.	2026/07/17	Joe Luo
V2.0	1. Added descriptions about FU7565Q1. 2. Deleted PFC descriptions about FU7564Q1. 3. Deleted QEP2 descriptions about FU7512Q1 and FU7574Q1. 4. Modified built-in I ² C, ADC, and DAC to indicate they are for internal use only in section 1.1 Features. 5. Deleted 2k ME_RAM in section 1.4 Functional Block Diagram. 6. Changed QEP1A and QEP1B pin type from DB to DI, changed QEP0Z from DI to DB, and changed the capacitor between CP1 and CP2 from 1μF to 0.1μF in chapter 2 Pin Definitions. 7. Changed VCP1 and VCP1_x (CP1 Charge Pump Voltage) from 60V to 40V in sections 5.1.2 and 5.1.4 (Absolute Maximum Ratings for FU7564Q1 and FU7574Q1). 8. Added condition "SLPF_R[SLP_FORCE] = 1" to the I _{VCC} sleep current for FU7564Q1 in section 5.2.2. 9. Added condition "SLPF_R[SLP_FORCE] = 1" to the I _{VCC_1} sleep current for FU7574Q1 and changed the typical value from 60μA to 40μA in section 5.2.4. 10. Updated the Bootstrap OVP Threshold Voltage V _{BOVR} max./typ./min. from 150/160/170%VBB to 175/185/195%VBB and Bootstrap OVP Release Voltage V _{BOVF} max./typ./min. from 140/150/160%VBB to 165/175/185%VBB in sections 5.5.1.2 and 5.5.3.2. 11. Updated VHALF max/min values in section 5.7 Reference Voltage Electrical Characteristics: changed VREF/8 ± 0.2 to VREF/8 ± 0.1, while VREF/4 ± 0.12 remains unchanged. 12. Added condition "VCC = 12V" to the VBB voltage specification for FU7564Q1 LDO in section 5.12.2. 13. Added condition "VCC_x = 12V" to the VBB_x voltage specification for FU7574Q1 LDO in section 5.12.4. 14. Added Table 18-4 Logic Truth Values of FU7574Q1 Built-in Pre-driverx and Table 18-6 Filtering Time. 15. Updated Figure 18-2, changing HINV to HREV_EN and LINV to LREV_EN. 16. Updated the I _{VDH} calculation formula in section 18.2.4.1.5 MOSFET V _{DS} OVP. 17. Updated Figure 18-4 Block Diagram of FU7574Q1 6N Pre-driverx: changed the capacitor between CP1_x and CP2_x from 1μF to	2026/07/17	Joe Luo

Rev.	Description	Date	Prepared By
	0.1μF, and renamed "Charge Pump" to "Charge Pump & LDO". 18. Changed the range of NFOCx_FUWEI [15:0] from [0,64] to [0,32767] in section 18.16.23.3 NFOCx_FUWEI (0x3000021A/0x3001021A) (x=1/2). 19. Updated Table 26-1 Mapping between Output Codes and Temperature Levels and Table 26-2 Mapping between TSD Codes and Protection Temperatures. 20. Changed the reset value of TSD_ADJ from 0000 to 1101 in section 26.1.1 TSD_CR (CSR: 0x630). 21. Deleted the descriptions of dual-comparator and triple-comparator modes in section 33.1.2 CMP9. 22. Deleted Figure 33-6 Cycle-by-cycle Current Limiting Waveform (t2 - t1 = 5μs) when DRV1_CR[MOEMD]=11 and Figure 33-12 Cycle-by-cycle Current Limiting Waveform (t2 - t1 = 5μs) when DRV2_CR[MOEMD]=11. 23. Updated the descriptions for bits [2:1] CMP0CSEL and [2:1] CMP6CSEL: changed "10: Low Speed; 11: Slow Speed" to "10: Slow Speed; 11: Low Speed" in sections 33.2.3 CMP_CR2 (0xDA) and 33.2.11 CMP_CR6 (CSR: 0x60A).		
V2.1	1. Added "Flash endurance: 1000 erase cycles" in section 1.1 Features. 2. Added symbols to the Test Conditions column in section 5.5.3.1 6N Pre-driverx Electrical Parameters of FU7574Q1. 3. Added a cross-reference in section 16.2.2 Input Signal Filtering and Edge Detection. 4. Added descriptions for bit [8]: "0: Chip selected; 1: Chip not selected" in section 10.3.2 SPIx_SR (CSR: 0x181/0x191) (x = 1/2). 5. Changed the range to [0,32767] in section 18.16.21.18 NFOCx_LKARR (0x30000028/0x30010028) (x = 1/2). 6. Modified items 5, 7, and 27 of V1.0 in chapter 40 Revision History.	2026/07/20	Joe Luo



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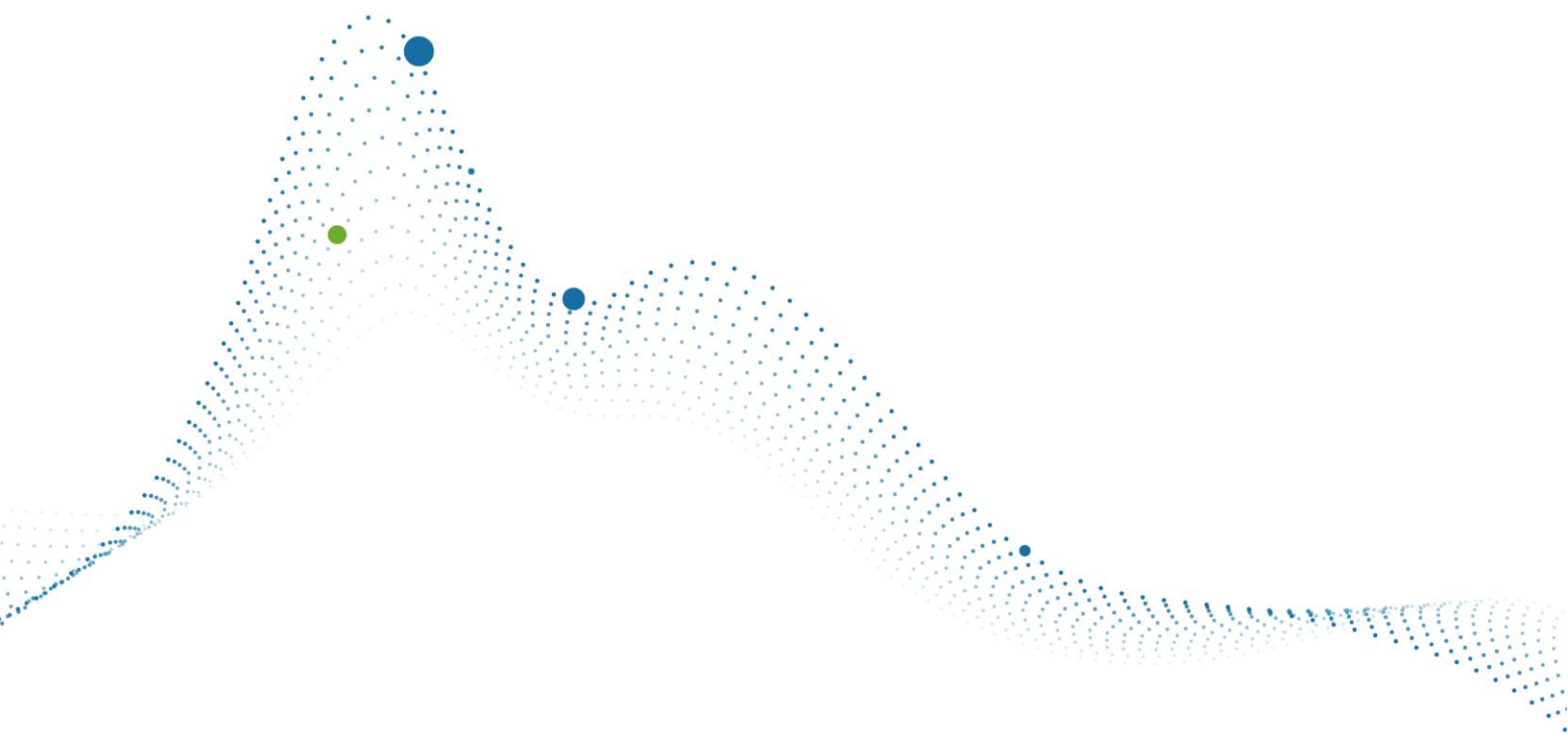
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