

INN040FQ012A

1. General Description

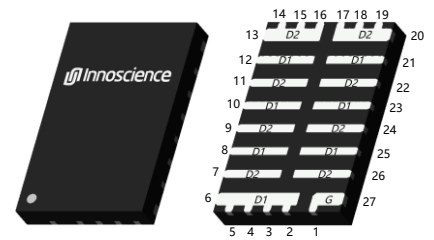
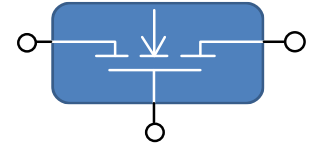
Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 6 mm x 4 mm package size.

2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

3. Applications

- High side load switch
- OVP protection in USB port
- Switch circuits in multiple power suppliers system



4. Key Performance Parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DD,max}$	40	V
$R_{D1D2(on),max}$ @ $V_G = 5\text{ V}$	1.2	m Ω
Q_G,typ @ $V_{DD} = 20\text{ V}$	60	nC
$I_{D,DC}$	100	A

5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
1,27	Gate	Driver Gate
2-6,8,10,12,21,23,25	Drain1	Power Drain1
7,9,11,13-20,22,24,26	Drain2	Power Drain2

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040FQ012A	FCQFN 6mm X 4mm	D18

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6. Maximum Ratings

at $T_J = 25\text{ °C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	40	V
V_{DG}	Drain-to-Gate Voltage	40	V
V_{GD}	Gate-to-Drain Voltage	6	V
I_D	Continuous Drain current	100	A
I_{DM}	Pulsed Drain Current (25 °C , $T_{Pulse} = 300\ \mu\text{s}$)	500	A
P_{tot}	Power dissipation ($T_{c, bottom} = 25\text{ °C}$)	105	W
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	°C

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
R _{θJC_top}	Thermal Resistance, Junction to Case (top)	14.26	°C/W	
R _{θJC_bot}	Thermal Resistance, Junction to Case (bottom)	0.95	°C/W	
R _{θJA}	Thermal Resistance, Junction to Ambient ¹	52.12	°C/W	
T _{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note 1: R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric Characteristics

 at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2S}	Drain1-to-Drain2 Breakdown Voltage	40			V	$V_{D2} = V_G = 0\text{ V}$, $I_{D1D2} = 500\text{ }\mu\text{A}$
BV_{D2D1S}	Drain2-to-Drain1 Breakdown Voltage	40			V	$V_{D1} = V_G = 0\text{ V}$, $I_{D2D1} = 500\text{ }\mu\text{A}$
I_{D1D2S}	Zero Gate Voltage Drain Current			50	μA	$V_{D2} = V_G = 0\text{ V}$, $V_{D1} = 40\text{ V}$
I_{D2D1S}	Zero Gate Voltage Drain Current			50	μA	$V_{D1} = V_G = 0\text{ V}$, $V_{D2} = 40\text{ V}$
I_{GDS}	Gate-to-Drain Leakage		0.5	5	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 5\text{ V}$
	Gate-to-Drain Leakage	10			μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = -5\text{ V}$
I_{GDS}	Gate-to-Drain Leakage		5	30	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 6\text{ V}$
	Gate-to-Drain Leakage	10			μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = -6\text{ V}$
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D1} = 0\text{ V}$, $V_{D2} = V_G$, $I_{D2D1} = 1\text{ mA}$
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D2} = 0\text{ V}$, $V_{D1} = V_G$, $I_{D1D2} = 1\text{ mA}$
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance		0.9	1.2	m Ω	$V_{D2} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D1D2} = 10\text{ A}$
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance		0.9	1.2	m Ω	$V_{D1} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D2D1} = 10\text{ A}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance		3.5		nF	V _G = 0 V, V _D = 20 V
C _{OSS}	Output Capacitance		1.6			
C _{RSS}	Reverse Transfer Capacitance		1.0			
R _G	Gate Resistance		8.7		Ω	f = 1 MHz
Q _G	Total Gate Charge		60		nC	V _D = 20 V, V _G = 5 V, I _D = 10 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D2D1} =20V)		6.2			V _{D1} = 0, V _{D2} = 20 V, I _{D2D1} = 10 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D1D2} =20V)		32			V _{D2} = 0, V _{D1} = 20 V, I _{D1D2} = 10 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D1D2} =20V)		6.2			V _{D2} = 0, V _{D1} = 20 V, I _{D1D2} = 10 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D2D1} =20V)		32			V _{D1} = 0, V _{D2} = 20 V, I _{D2D1} = 10 A
Q _{OSS}	Output Charge		45			V _G = 0 V, V _D = 20 V

9. Electric Characteristics Diagrams

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Note: In Charts, VD1D2 can be VD2D1 with same characteristic chart due to Bi-directional feature.

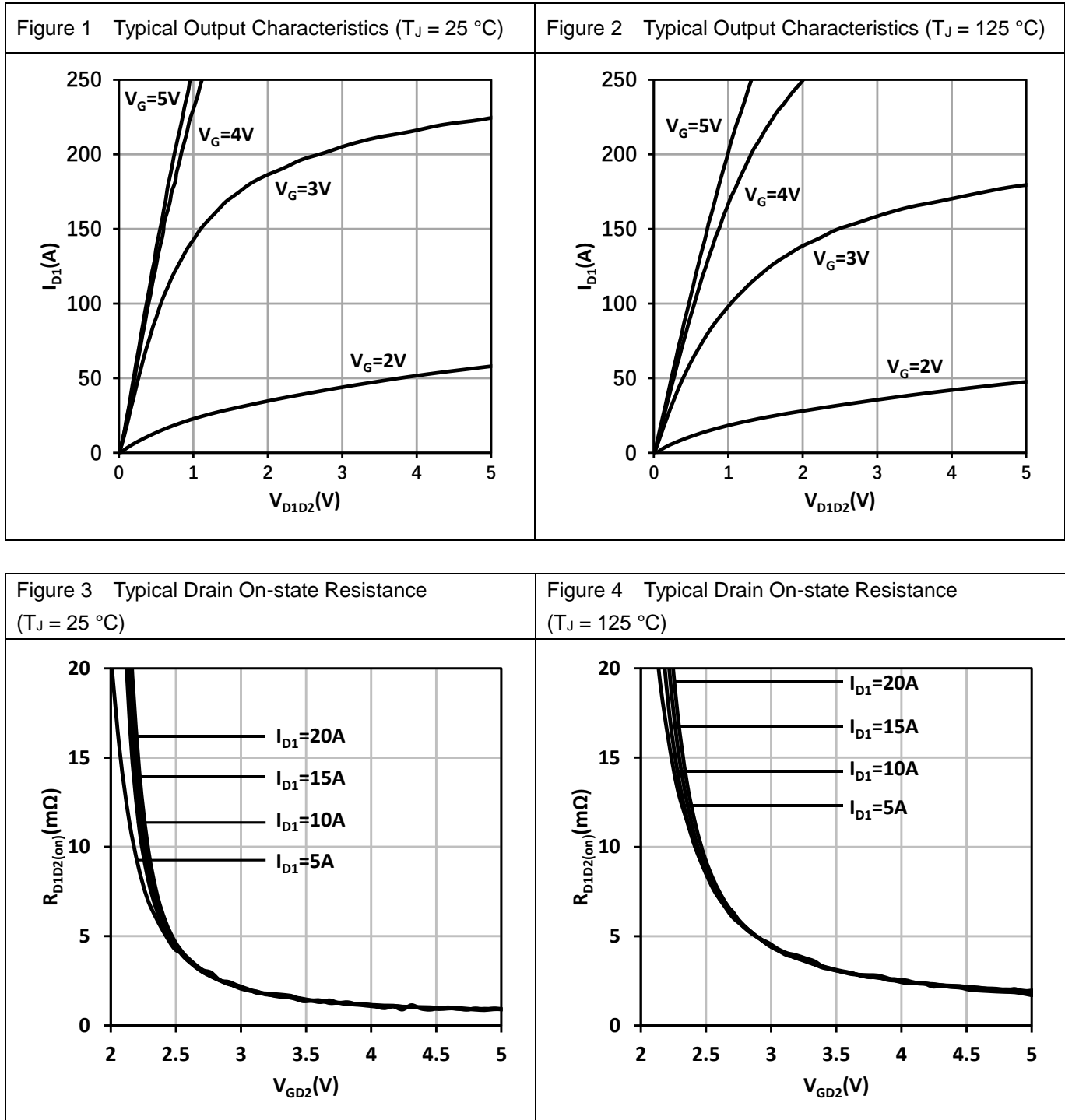


Figure 5 Typical On Resistance vs. Temperature

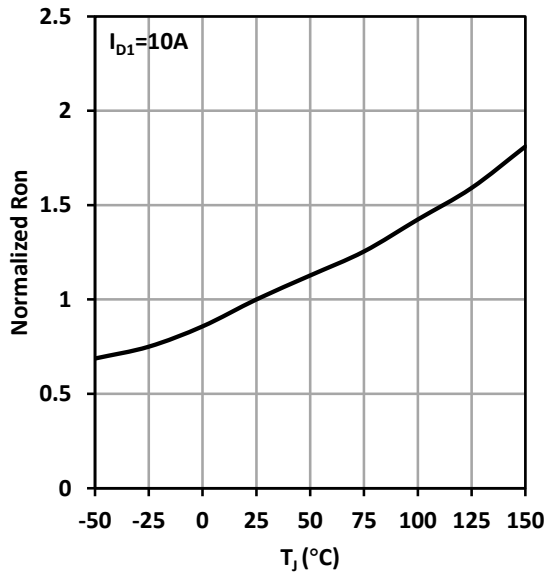


Figure 6 Typical Transfer Characteristics

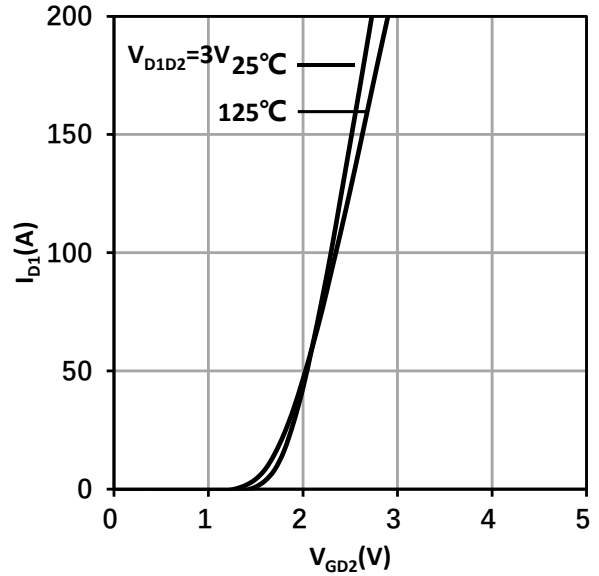


Figure 7 Typ. Reverse Drain1- Drain2 Characteristics (V_{GD2} ≤ 0V, T_J = 25 °C)

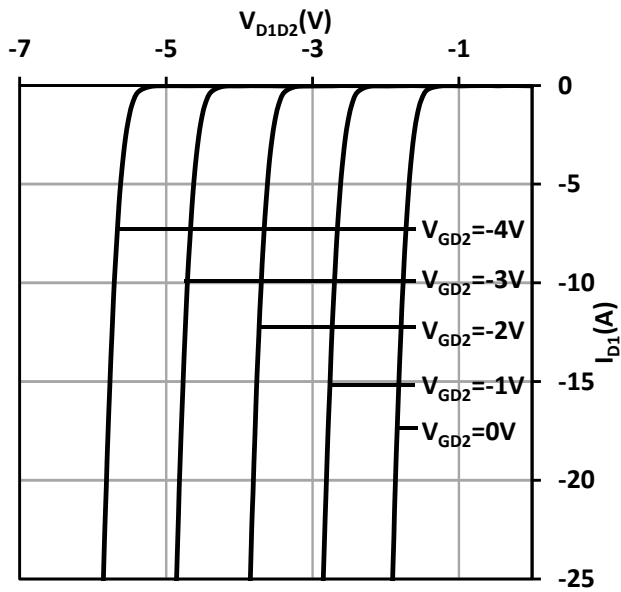


Figure 8 Typ. Reverse Drain1- Drain2 Characteristics (V_{GD2} ≥ 0V, T_J = 25 °C)

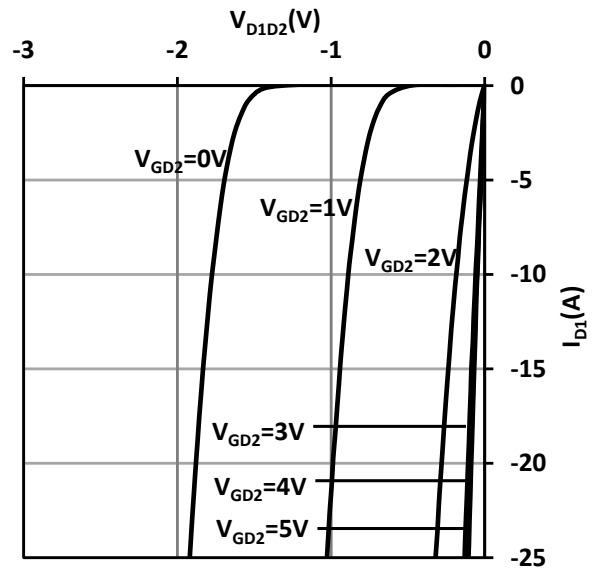


Figure 9 Typ. Reverse Drain1- Drain2 Characteristics ($V_{GD2} \leq 0V$, $T_J = 125^\circ C$)

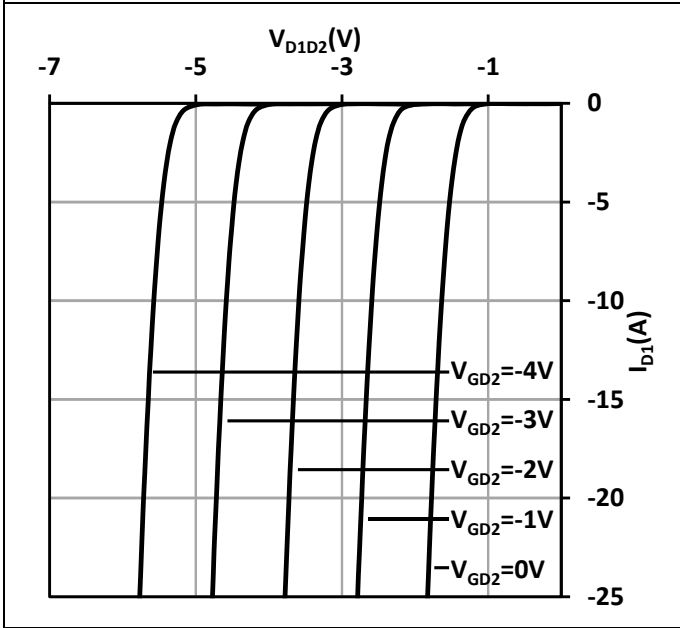


Figure 10 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \geq 0V$, $T_J = 125^\circ C$)

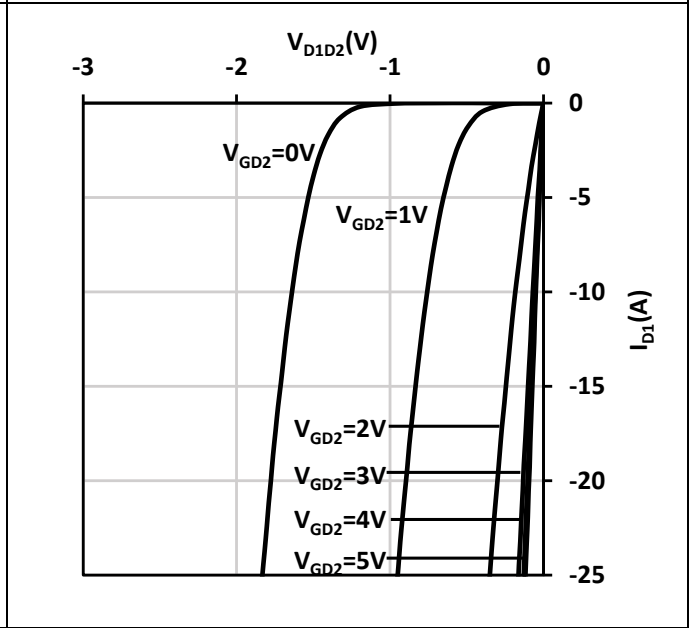


Figure 11 Typical Capacitances Characteristics

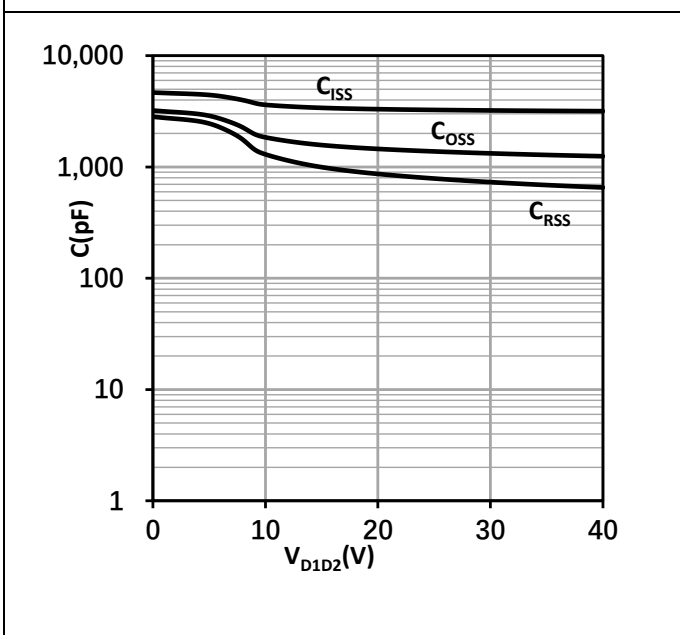


Figure 12 Typical Gate Charge

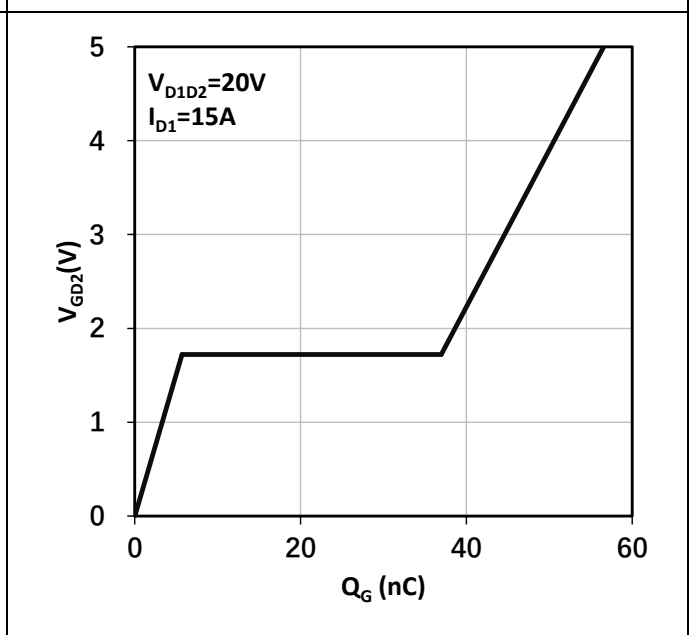


Figure 13 Normalized Threshold Voltage vs. Temp.

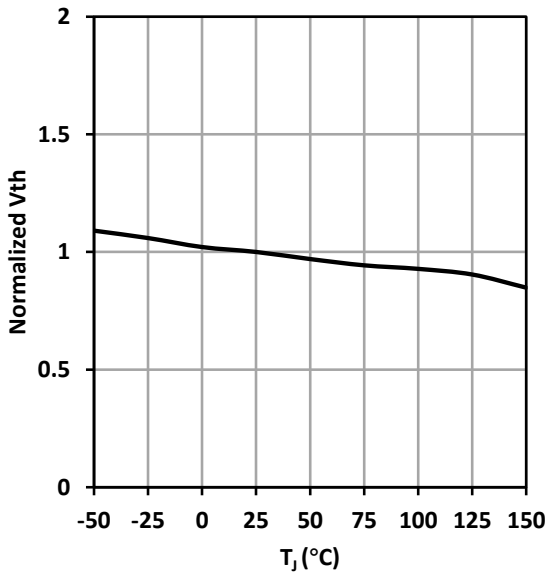


Figure 14 Output Charge

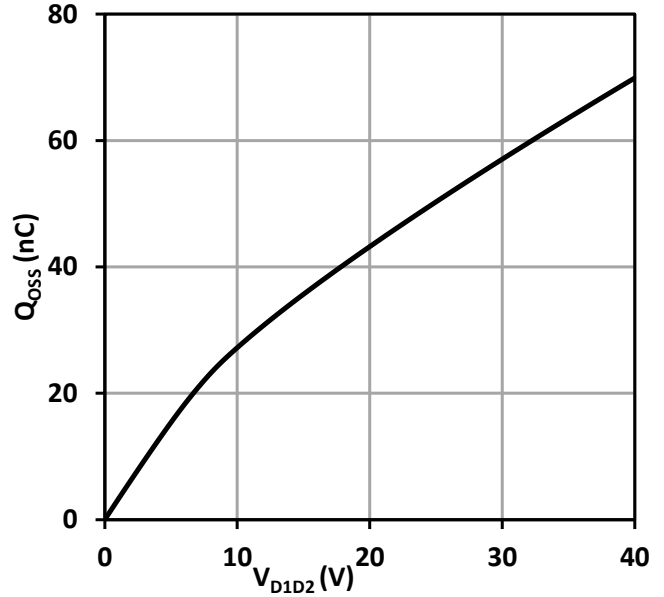


Figure 15 Output Capacitance Stored Energy

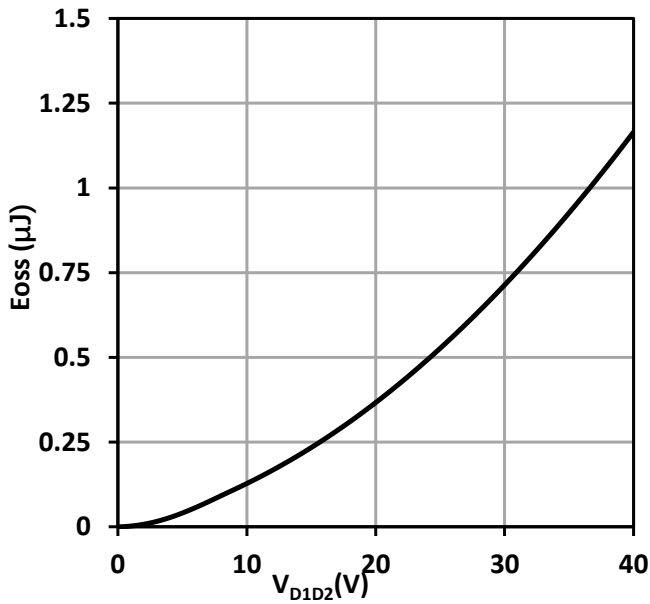


Figure 16 Power Dissipation

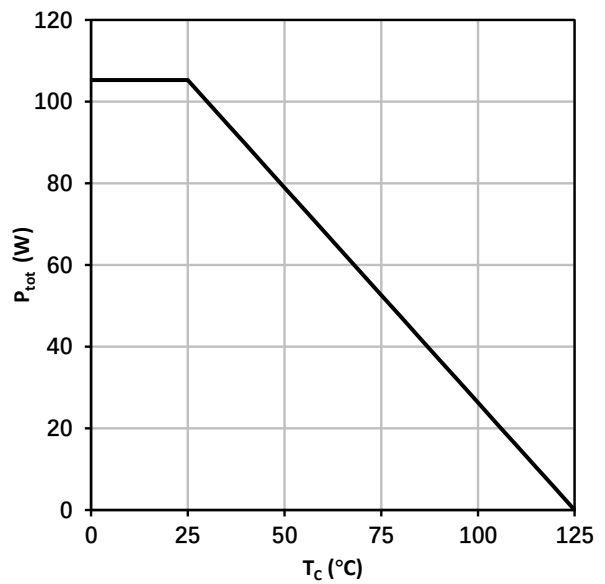


Figure 17 Safe Operating Area

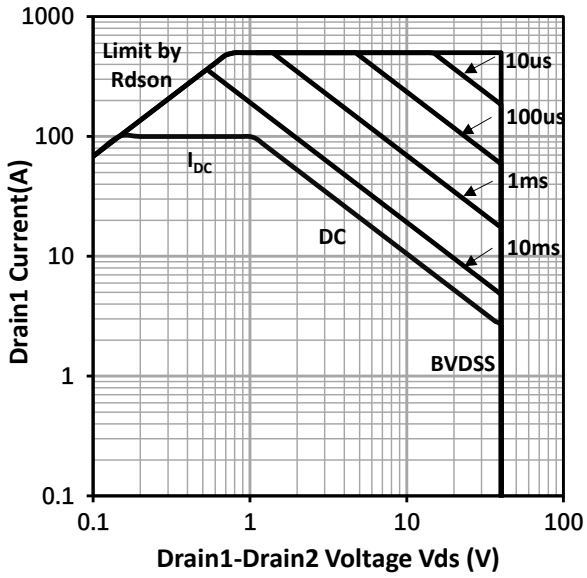
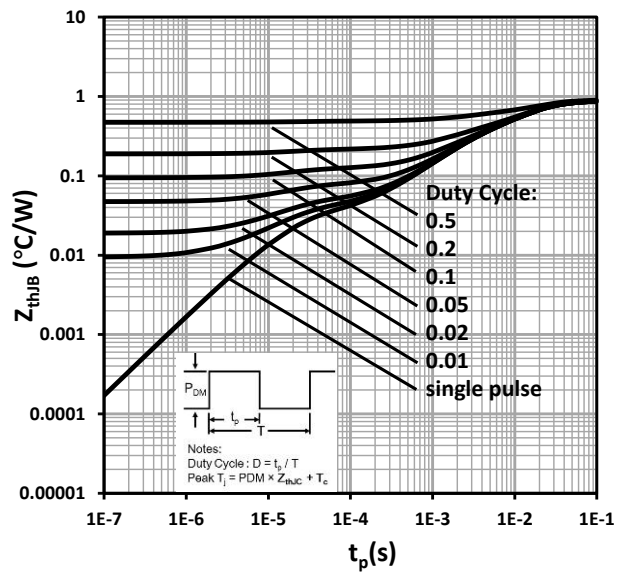
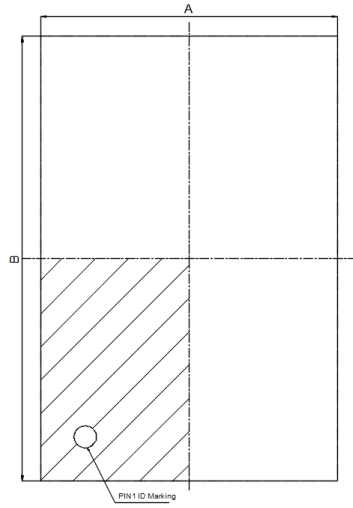


Figure 18 Max. Transient Thermal Impedance

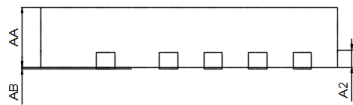


10. Package Outlines

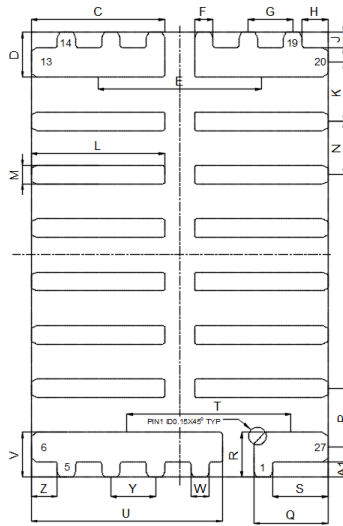
Package Reference



TOP VIEW



SIDE VIEW



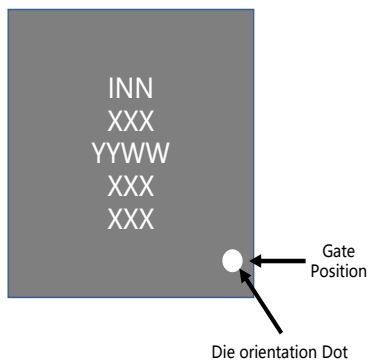
BOTTOM VIEW

NOTE:

- 1) ALL DIMENSION ARE IN MILLIMETERS.
- 2) BOTTOM VIEW IS FT TESTER SIDE VIEW.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) COMPLIES WITH JEDEC MO-220.
- 5) DRAWING IS NOT TO SCALE.

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.90	4.00	4.10	
B	5.90	6.00	6.10	
C	1.700	1.800	1.900	2X
D	0.505	0.605	0.705	2X
E	2.200 BASIC			7X
F	0.200	0.250	0.300	6X
G	0.600 BASIC			4X
H	0.350 REF			2X
J	0.205 REF			6X
K	0.795 BASIC			2X
L	1.700	1.800	1.900	12X
M	0.200	0.250	0.300	12X
N	0.720 BASIC			10X
P	0.795 BASIC			2X
Q	0.900	1.000	1.100	
R	0.505	0.605	0.705	
S	0.750 REF			
T	2.213 BASIC			
U	2.475	2.575	2.675	
V	0.505	0.605	0.705	
W	0.200	0.250	0.300	5X
Y	0.600 BASIC			3X
Z	0.350 REF			
A1	0.205 REF			6X
A2	0.203 REF			
AA	0.75	0.85	0.95	
AB	0	0.02	0.05	

Marking Reference:



Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot Code	XXX
Row 5		XXX

11. Reel Information

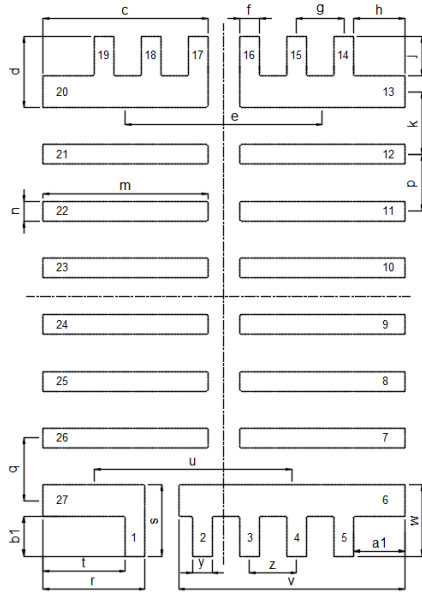
A ₀	4.30	+/- 0.1
B ₀	6.30	+/- 0.1
K ₀	1.10	+/- 0.1
F	5.50	+/- 0.1
P ₁	8.00	+/- 0.1
W	12.00	+/- 0.3

Unit: mm

Value & Tolerance				
A	B	C	D	t
Ø329±1	12.4 ^{+2.0} / _{-9.0}	Ø100±1	Ø13.3±0.3	2.0±0.3

12. Land Pattern

Recommended Land Pattern



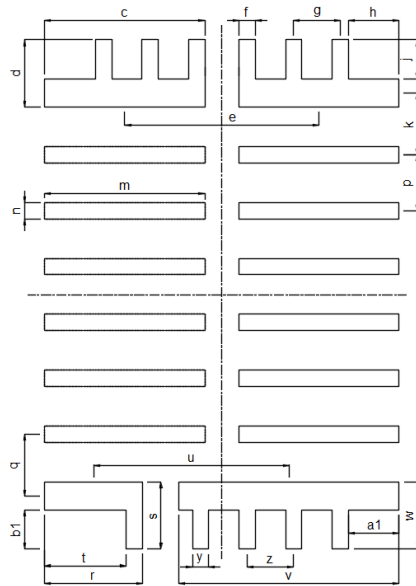
TOP VIEW

SYMBOL	MILLIMETER	
	NOM	NOTE
c	2.100	2X
d	0.905	2X
e	2.500	7X
f	0.250	6X
g	0.600	4X
h	0.650	2X
j	0.505	6X
k	0.795	2X
m	2.100	12X
n	0.250	12X
p	0.720	10X
q	0.795	2X
r	1.300	
s	0.905	
t	1.050	
u	2.513	
v	2.875	
w	0.905	
y	0.250	5X
z	0.600	3X
a1	0.650	
b1	0.505	6X

NOTE:

- 1) LAND PATTERN IS SOLDER MASK DEFINED.
- 2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

Recommended Stencil Drawing



TOP VIEW

SYMBOL	MILLIMETER	
	NOM	NOTE
c	2.060	2X
d	0.865	2X
e	2.500	7X
f	0.210	6X
g	0.600	4X
h	0.650	2X
j	0.505	6X
k	0.795	2X
m	2.060	12X
n	0.210	12X
p	0.720	10X
q	0.795	2X
r	1.260	
s	0.865	
t	1.050	
u	2.513	
v	2.835	
w	0.865	
y	0.210	5X
z	0.600	3X
a1	0.650	
b1	0.505	6X

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-06-15	Datasheet Version 1.0 Release
1.1	2023-08-14	<ol style="list-style-type: none">1. Updated format and corrected typos2. Added P_{tot} in Maximum Ratings3. Corrected description 'D' to 'D1', 'S' to 'D2' in Electric Characteristics Diagrams4. Updated Note in Electric Characteristics Diagrams

Important Notice

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