# INN650N240A

## 1. General description

**650V GaN-on-Silicon Enhancement-mode Power Transistor Bare Die**

## 2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

## 3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion
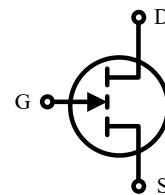
## 4. Key performance parameters

**Table 1        Key performance parameters at $T_j$ = 25 °C**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS,max}$ | 650 | V |
| $R_{DS(on),max}$ @ $V_{GS}$ = 6 V | 240 | mΩ |
| $Q_{G,typ}$ @ $V_{DS}$ = 400 V | 2 | nC |
| $I_{D,pulse}$ | 18 | A |
| $Q_{OSS}$ @ $V_{DS}$ = 400 V | 21 | nC |
| $Q_{rr}$ @ $V_{DS}$ = 400 V | 0 | nC |

## 5. Pin information

**Table 2        Pin information**

| Gate | Drain | Source |
|---|---|---|
| G | D | S1~S4 |

**Table 3        Ordering information**

| Type/Ordering Code | Product Code |
|---|---|
| INN650N240A | INN650N240A |

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## 6. Maximum ratings

at $T_j$ = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

**Table 4      Maximum ratings**

| Parameter | Symbol | Values | Unit | Note/Test Condition |
|---|---|---|---|---|
| Drain source voltage | $V_{DS, max}$ | 650 | V | $V_{GS}$ = 0 V; $T_j$ = -55 °C to 150 °C |
| Drain source voltage transient [1] | $V_{DS, transient}$ | 800 | V | $V_{GS}$ = 0 V |
| Drain source voltage, pulsed [2] | $V_{DS, pulse}$ | 750 | V | $T_j$ = 25 °C; total time < 10 h<br>$T_j$ = 125 °C; total time < 1 h |
| Continuous current, drain source[3] | $I_D$ | 10 | A | $T_c$ = 25 °C |
| Pulsed current, drain source [4] | $I_{D, pulse}$ | 18 | A | $T_c$ = 25 °C; $V_{GS}$ = 6 V; $t_{PULSE}$ = 300 µs |
| Pulsed current, drain source [4] | $I_{D, pulse}$ | 10 | A | $T_c$ = 125 °C; $V_{GS}$ = 6 V; $t_{PULSE}$ = 300 µs |
| Gate source voltage, continuous [5] | $V_{GS}$ | -1.4 to +7 | V | $T_j$ = -55 °C to 150 °C |
| Gate source voltage, pulsed | $V_{GS, pulse}$ | -20 to +10 | V | $T_j$ = -55 °C to 150 °C; $t_{PULSE}$ = 50 ns, f = 100 kHz; open drain |
| Operating temperature | $T_j$ | -55 to +150 | ˚C | |
| Storage temperature | $T_{stg}$ | -55 to +150 | ˚C | |

1. $V_{DS, transient}$ is intended for non-repetitive events, $t_{PULSE}$ < 200 µs.

2. $V_{DS, pulse}$ is intended for repetitive pulse, $t_{PULSE}$ < 100 ns.

3. Limited by maximum temperature allowed with the parts assembled in DFN 5X6 package.

4. Limit was extracted from characterization test, not measured during production.

5. The minimum $V_{GS}$ is clamped by ESD protection circuit, as shown in Figure 10.

## 7. Electric characteristics[1]

at $T_j$ = 25 °C, unless specified otherwise

**Table 5**      **Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note/Test Condition |
|-----------|--------|--------|------|------|------|---------------------|
| | | Min. | Typ. | Max. | | |
| Gate threshold voltage | $V_{GS(th)}$ | 1.2 | 1.7 | 2.5 | V | $I_D$ = 11 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C |
| | | - | 1.7 | - | | $I_D$ = 11 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C |
| Drain-source leakage current | $I_{DSS}$ | - | 0.4 | 20 | µA | $V_{DS}$ = 650 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C |
| | | - | 5 | - | | $V_{DS}$ = 650 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 50 | - | µA | $V_{GS}$ = 6 V; $V_{DS}$ = 0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 165 | 240 | mΩ | $V_{GS}$ = 6 V; $I_D$ = 3 A; $T_j$ = 25 °C |
| | | - | 360 | - | mΩ | $V_{GS}$ = 6 V; $I_D$ = 3 A; $T_j$ = 150 °C |
| Gate resistance | $R_G$ | - | 5 | - | Ω | f = 5 MHz; open drain |

**Table 6**      **Dynamic characteristics**

| Parameter | Symbol | Values | | | Unit | Note/Test Condition |
|-----------|--------|--------|------|------|------|---------------------|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 79 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 100 kHz |
| Output capacitance | $C_{oss}$ | - | 25 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 100 kHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 0.2 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 400 V; f = 100 kHz |
| Effective output capacitance, energy related [2] | $C_{o(er)}$ | - | 36 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 0 to 400 V |
| Effective output capacitance, time related [3] | $C_{o(tr)}$ | - | 52 | - | pF | $V_{GS}$ = 0 V; $V_{DS}$ = 0 to 400 V |
| Output charge | $Q_{OSS}$ | - | 21 | - | nC | $V_{GS}$ = 0 V; $V_{DS}$ = 0 to 400 V |
| Turn-on delay time | $t_{d(on)}$ | - | 2 | - | nS | $V_{DS}$ = 400 V; $I_D$ = 6 A; L = 318 µH; $V_{GS}$ = 6 V; $R_{on}$ = 10 Ω; $R_{off}$ = 2 Ω; See Figure 22 |
| Turn-off delay time | $t_{d(off)}$ | - | 4 | - | nS | |
| Rise time | $t_r$ | - | 5 | - | nS | |
| Fall time | $t_f$ | - | 6 | - | nS | |

1. The electrical characteristics parameters were tested with the parts assembled in DFN 5X6 package.

2. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V.

3. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V.

**Table 7        Gate charge characteristics**

| Parameter | Symbol | Values | | | Unit | Note/Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate charge | $Q_G$ | - | 2 | - | nC | $V_{GS}$ = 0 to 6 V; $V_{DS}$ = 400 V; $I_D$ = 3 A |
| Gate-source charge | $Q_{GS}$ | - | 0.2 | - | nC | |
| Gate-drain charge | $Q_{GD}$ | - | 0.7 | - | nC | |
| Gate Plateau Voltage | $V_{Plat}$ | - | 2.5 | - | V | $V_{DS}$ = 400 V; $I_D$ = 3 A |

**Table 8        Reverse conduction characteristics**

| Parameter | Symbol | Values | | | Unit | Note/Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Source-Drain reverse voltage | $V_{SD}$ | - | 2.6 | - | V | $V_{GS}$ = 0 V; $I_S$ = 3 A |
| Pulsed current, reverse | $I_{S, pulse}$ | - | - | 18 | A | $V_{GS}$ = 6 V; $t_{PULSE}$ = 300 µs |
| Reverse recovery charge | $Q_{rr}$ | - | 0 | - | nC | $I_S$ = 3 A; $V_{DS}$ = 400 V |
| Reverse recovery time | $t_{rr}$ | - | 0 | - | ns | |
| Peak reverse recovery current | $I_{rrm}$ | - | 0 | - | A | |

## 8. Electric characteristics diagrams[1]

at $T_j$ = 25 °C, unless specified otherwise

| Figure 1    Typ. output characteristics | Figure 2    Typ. output characteristics |
|---|---|
|  |  |
| $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$ = 25 °C | $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$ = 125 °C |

| Figure 3    Typ. Drain-source on-state resistance | Figure 4    Typ. Drain-source on-state resistance |
|---|---|
|  |  |
| $R_{DS(on)}$ = f($I_{DS}$,$V_{GS}$); $T_j$ = 25 °C | $R_{DS(on)}$ = f($I_{DS}$,$V_{GS}$); $T_j$ = 125 °C |
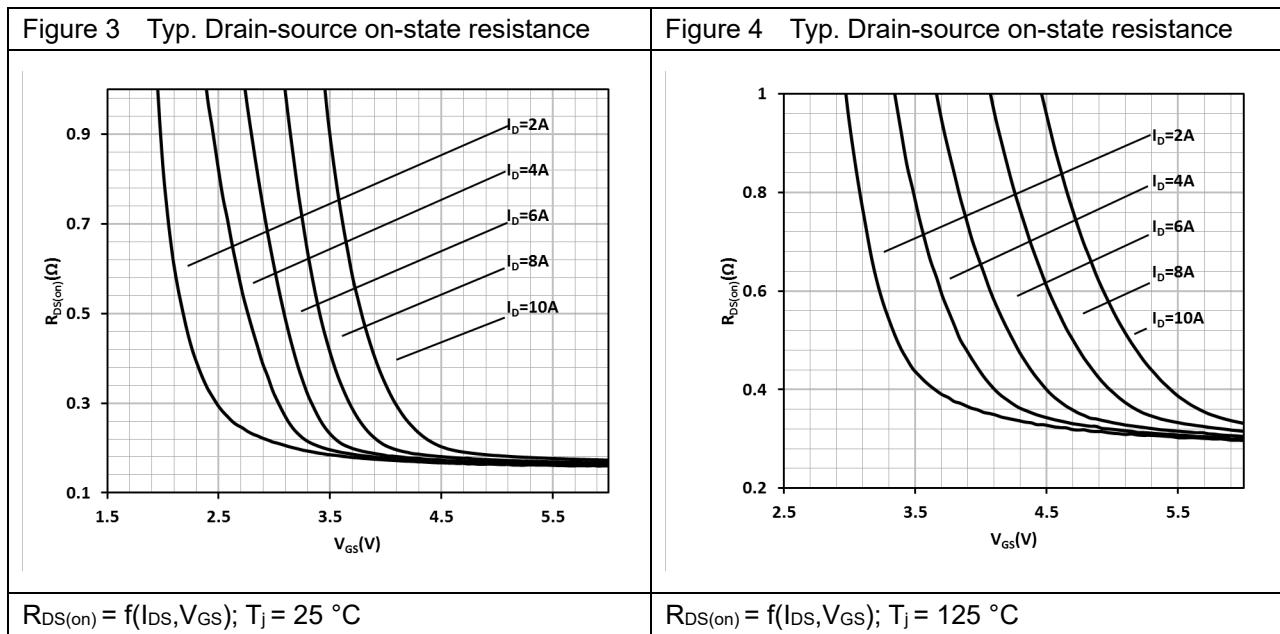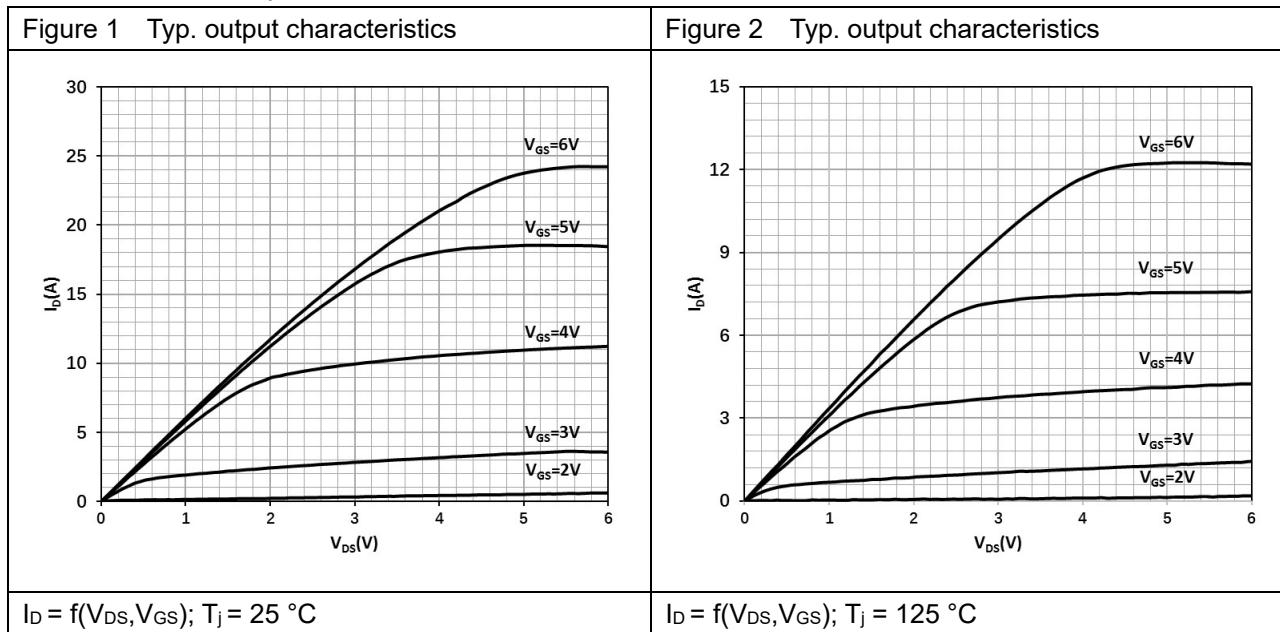
1. The typical electrical characteristic curves were measured with the parts assembled in DFN 5X6 package.

| Figure 5 Typ. channel reverse characteristics | Figure 6 Typ. channel reverse characteristics |
|---|---|
|  |  |
| $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$= 25 °C | $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$ = 125 °C |

| Figure 7 Typ. channel reverse characteristics | Figure 8 Typ. channel reverse characteristics |
|---|---|
|  |  |
| $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$ = 25 °C | $I_D$ = f($V_{DS}$,$V_{GS}$); $T_j$ = 125 °C |
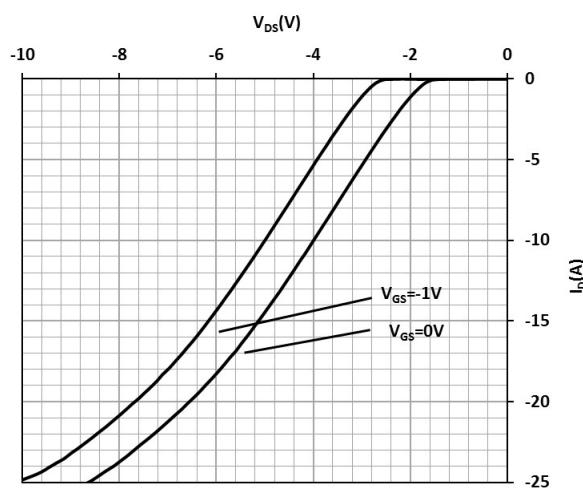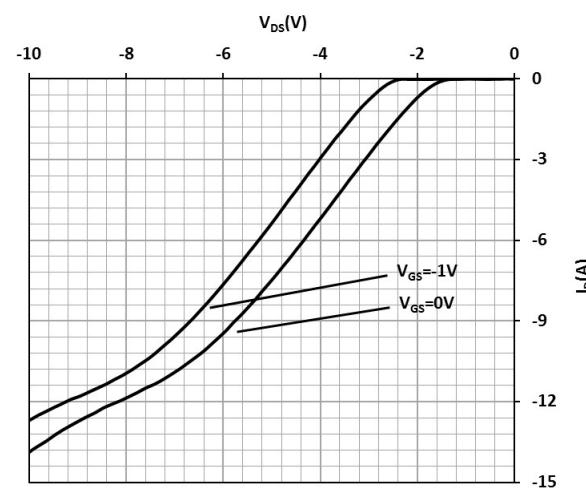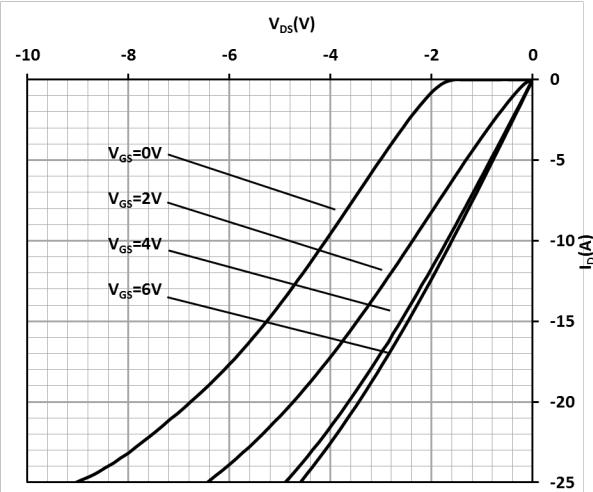
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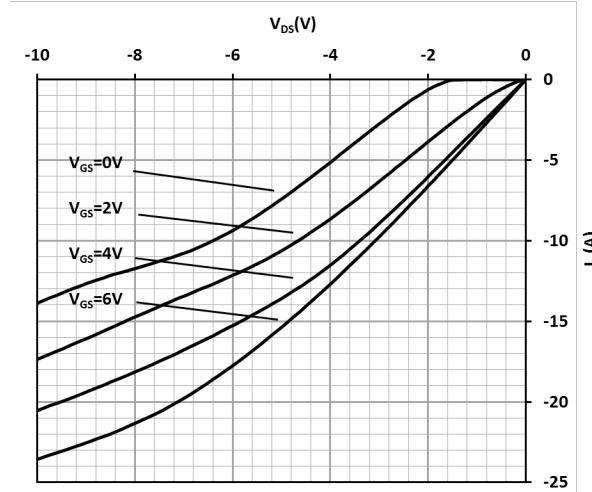
| Figure 9 Typ. transfer characteristics | Figure 10 Typ. Gate-to-Source leakage |
|---|---|
|  |  |
| $I_D = f(V_{GS})$; $V_{DS}$= 3 V | $I_G = f(V_{GS})$; $I_G$ reverse turn on by ESD unit |

| Figure 11 Drain-source leakage characteristics |
|---|
|  |
| $I_{DSS} = f(V_{DS})$; $V_{GS}$ = 0 V |

| Figure 12 | Gate threshold voltage |
|---|---|
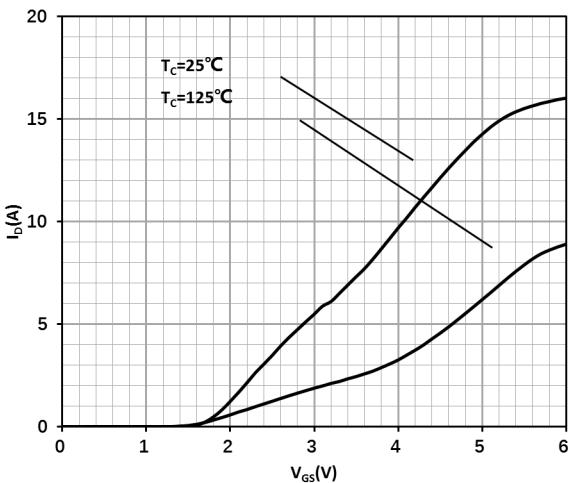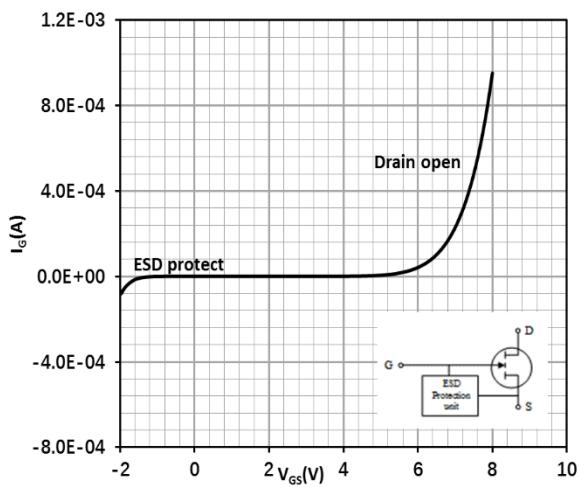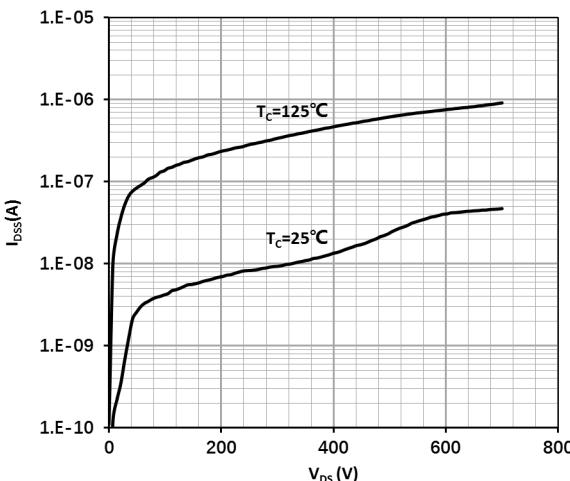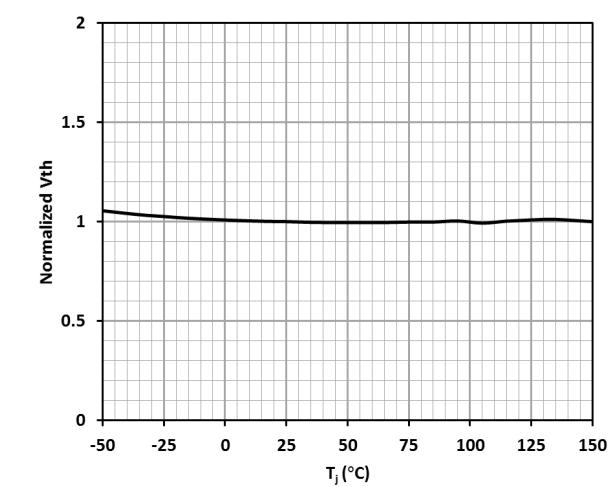


$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 11$ mA

| Figure 13 | Drain-source on-state resistance |
|---|---|
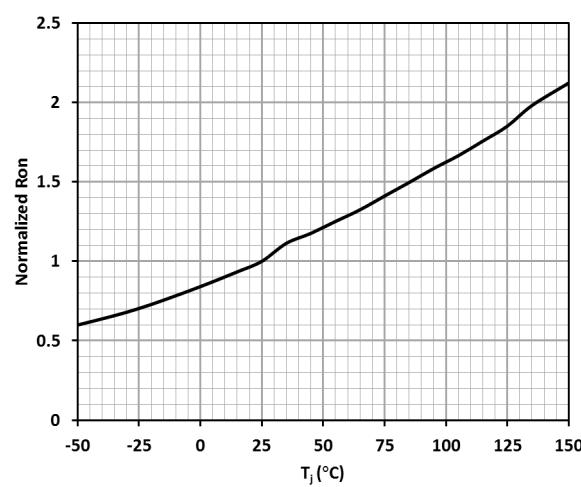


$R_{DS(on)} = f(T_j)$; $I_D = 3$ A; $V_{GS} = 6$V

| Figure 14 | Power dissipation |
|---|---|
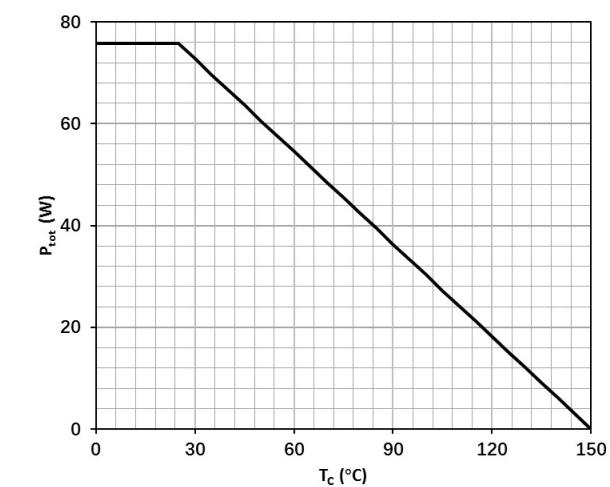


$P_{tot} = f(T_C)$

| Figure 15 | Max.transient thermal impedance |
|---|---|



$Z_{thJC} = f(t_P, D)$

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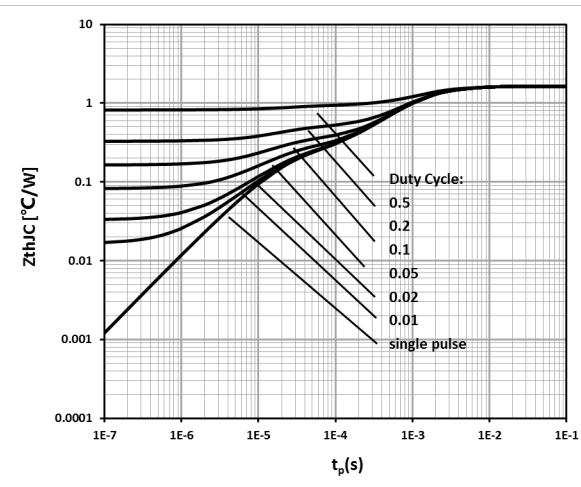
| Figure 16   Safe operating area | Figure 17   Safe operating area |
|---|---|
|  |  |
| $I_D = f(V_{DS})$; $T_C$ = 25 °C | $I_D = f(V_{DS})$; $T_C$ = 125 °C |

| Figure 18   Typ. gate charge | Figure 19   Typ. capacitances |
|---|---|
|  |  |
| $V_{GS} = f(Q_G)$; $V_{DCLINK}$ = 400 V; $I_D$ = 3 A | $C_{XSS} = f(V_{DS})$; Freq. = 100 kHz |
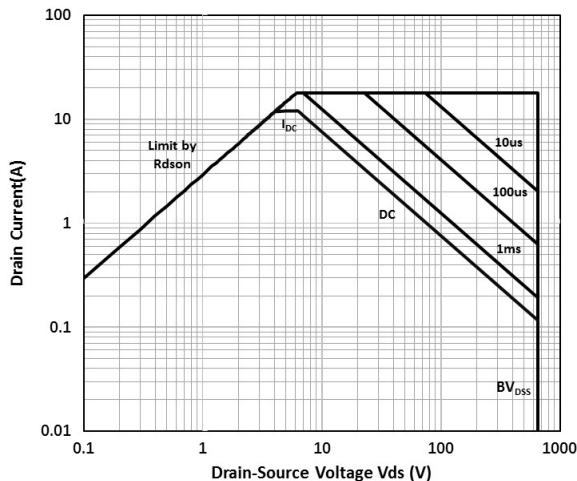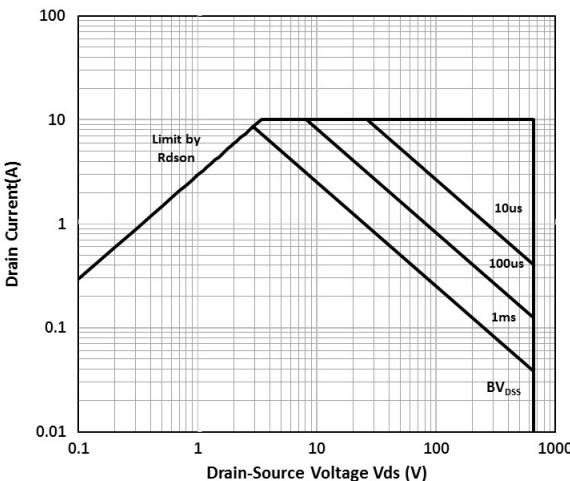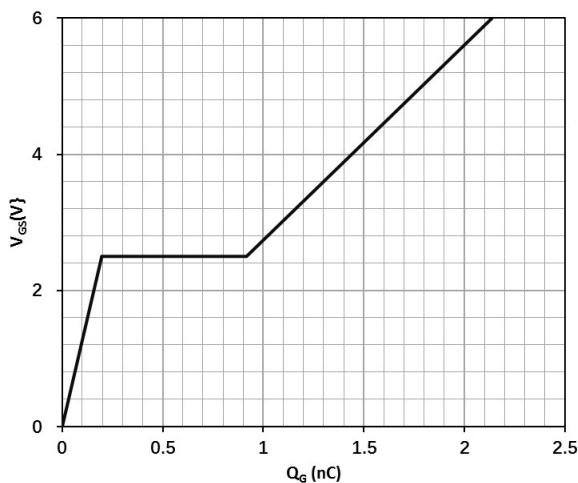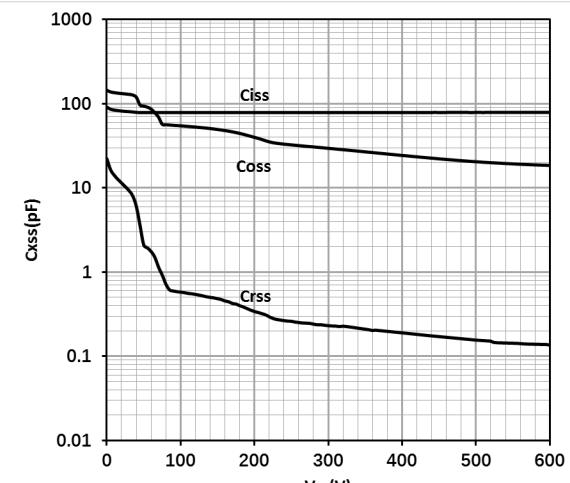
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| Figure 20    Typ. output charge | Figure 21    Typ. $C_{OSS}$ stored Energy |
|---|---|
|  |  |
| $Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz | $E_{OSS} = f(V_{DS})$; Freq. = 100 kHz |

| Figure 22    Typ.Switching times with inductive load | Figure 23    Typ.Switching times waveform |
|---|---|
|  |  |
| $V_{DS}$ = 400 V, $I_D$ = 6 A, L = 318 µH, $V_{GS}$ = 6 V, $R_{on}$ = 10 Ω, $R_{off}$ = 2 Ω | |
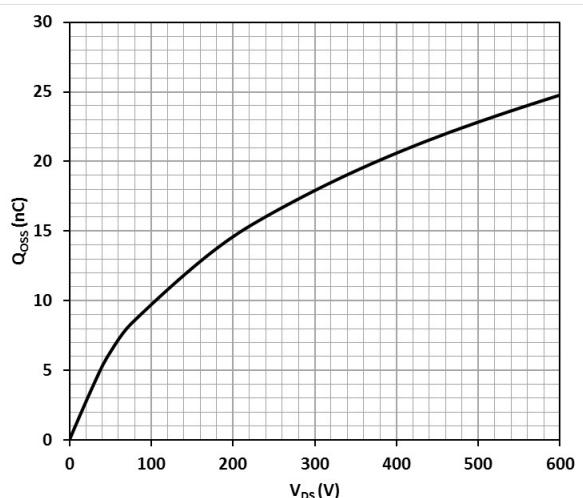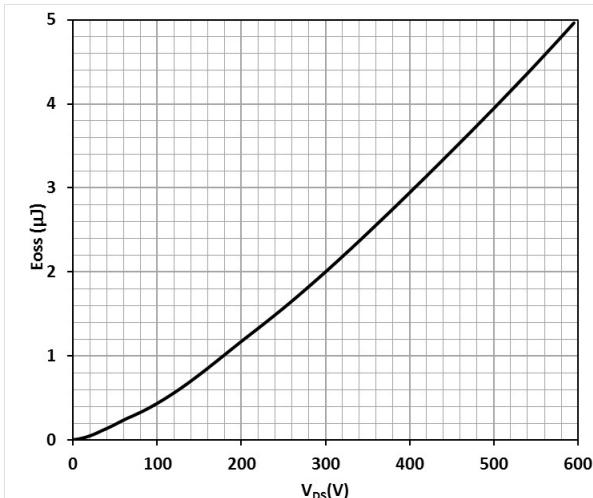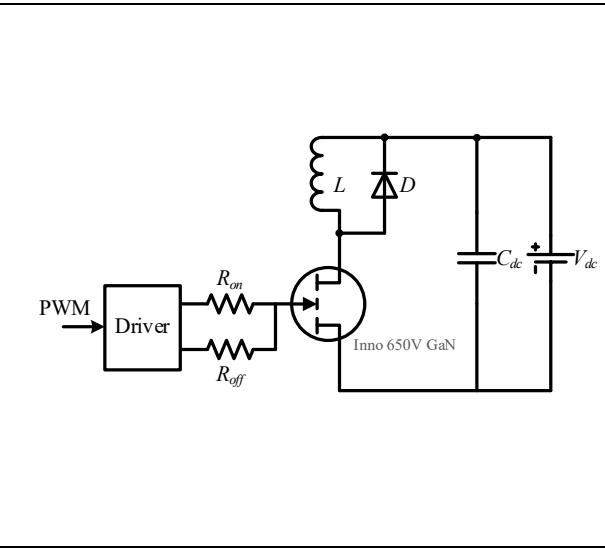
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## 9. Chip drawing

Unit: um

| | G | S1 | S2 | S3 | S4 | D |

Dimensions shown: 65, 64.5, 69, 69, 69, 76, 80, 145, 145, 515, 515, 515, 703.5, 1147.5, 2430, 1570, 145, 313, 67, 56.5, 2810
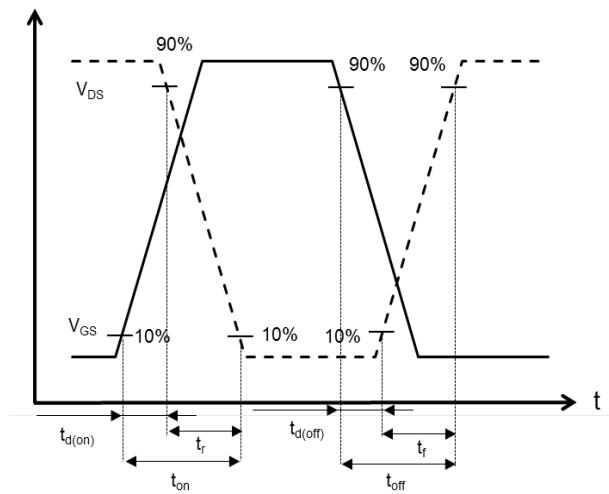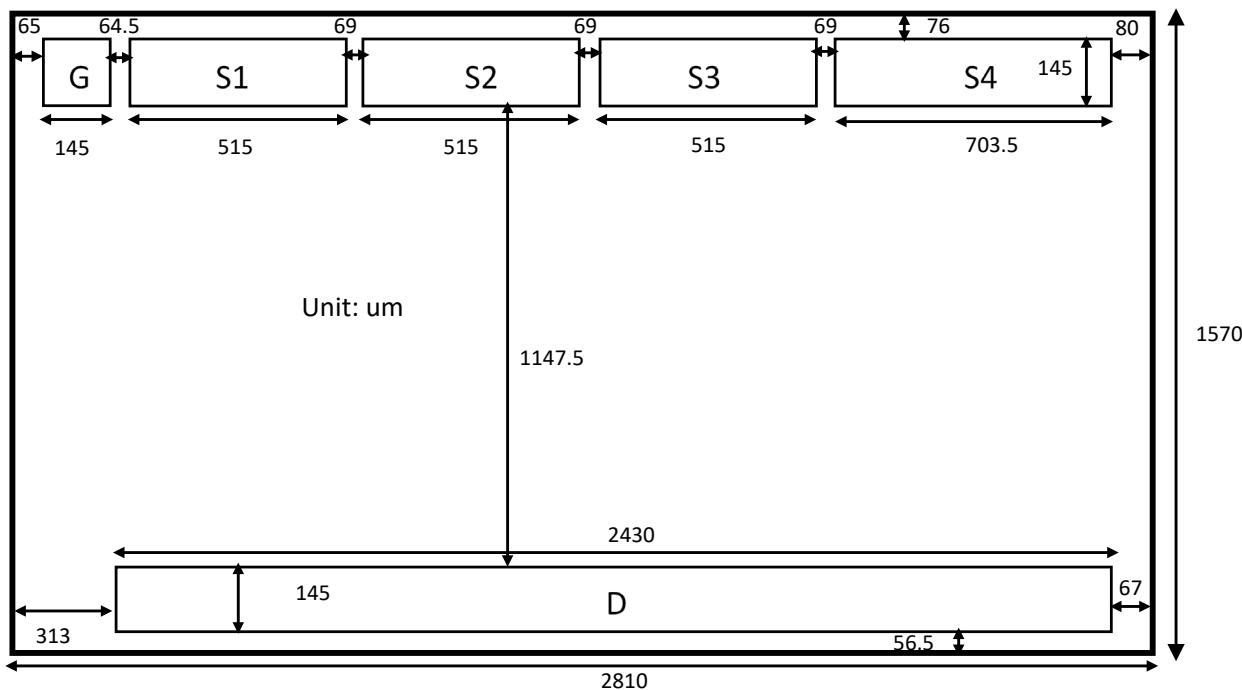
## Wafer features

| Physical Characteristics | | Unit |
|---|---|---|
| Wafer Size | 8 | inches |
| Wafer Thickness | 1150 | μm |
| Die Size (with S/L) | 2.89 x 1.65 | mm$^2$ |
| Scribe Street Width | 80 | μm |
| Metal thickness | 3.5 | μm |
| Top Metallization | Al-Cu | |
| Gate Pad Size | 145x145 | μm$^2$ |
| Source Pad Size | S1:515 x 145<br>S2:515 x 145<br>S3:515 x 145<br>S4:703.5 x 145 | μm$^2$ |
| Drain Pad Size | 2430 x 145 | μm$^2$ |
| Backside | Silicon | |

**Note:** All the pad size refers to PI top opening size, actual size at PI bottom (top metal exposure) is about 4~8 μm shorter than top opening.

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## 10. Revision history

**Major changes since the last revision**

| Revision | Date | Description of changes |
|----------|------|------------------------|
| 1.0 | 2021-10-26 | 1.0 version release |
| 1.2 | 2022-04-09 | 1. Optimize parameter descriptions.<br>2. Delete $E_{on}/E_{off}/E_{oss}$ from Electric characteristics. |

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