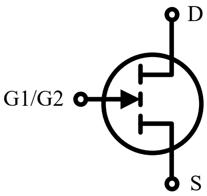
INN650N600A

1. General description

650V GaN-on-Silicon Enhancement-mode Power Transistor Bare Die

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



3. Applications

- DCM/BCM PFC
- AHB/LLC/QR Flyback/ACF DCDC converter
- LED driver
- Fast battery charger
- Standard adaptor

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	600	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	0.7	nC
$I_{D,pulse}$	6	A
Q_{OSS} @ V_{DS} = 400 V	7.3	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Source
G1,G2	D	S

Table 3 Ordering information

Type/Ordering Code	Product Code
INN650N600A	INN650N600A

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	650	V	V_{GS} = 0 V, T_j = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS,transient}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS,pulse}$	750	V	T_j = 25 °C; total time < 10 h T_j = 125 °C; total time < 1 h
Continuous current, drain source[3]	I_D	3.3	A	T_c = 25 °C
Pulsed current, drain source [4]	$I_{D,pulse}$	6	A	T_c = 25 °C; V_G = 6 V; t_{PULSE} = 10 µs
Pulsed current, drain source [4]	$I_{D,pulse}$	3.3	A	T_c = 125 °C; V_G = 6 V; t_{PULSE} = 10 µs
Gate source voltage, continuous [5]	V_{GS}	-1.4 to +7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1 $V_{DS,transient}$ is intended for non-repetitive events, t_{PULSE} < 200 µs

2 $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns

3 Limited by maximum temperature allowed with the parts assembled in DFN 5X6 package

4 Limit was extracted from characterization test, not measured during production

5 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Electric characteristics[1]

at T_j = 25 °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 3.8 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 3.8 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.15	8	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	1.5	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	15	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	470	600	mΩ	V_{GS} = 6 V; I_D = 1.4 A; T_j = 25 °C
		-	1020	-	mΩ	V_{GS} = 6 V; I_D = 1.4 A; T_j = 150 °C
Gate resistance-G1[2]	R_{G1}	-	13	-	Ω	f = 5 MHz; open drain
Gate resistance-G2[2]	R_{G2}	-	14	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	30	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	9	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer Capacitance	C_{rss}	-	0.1	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related[3]	$C_{o(er)}$	-	12.7	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related[4]	$C_{o(tr)}$	-	18.3	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	7.3	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	0.6	-	nS	V_{DS} = 400 V; I_D = 2.8 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 22
Turn-off delay time	$t_{d(off)}$	-	10.6	-	nS	
Rise time	t_r	-	3.7	-	nS	
Fall time	t_f	-	9.8	-	nS	
Output Capacitance Stored Energy	E_{oss}	-	1.0	-	μJ	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz

1 The electrical characteristics parameters were tested with the parts assembled in DFN 5X6 package

2 Refer to chip drawing section, device owns different R_G while bonding from different gate pad

3 $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

4 $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	0.7	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 1.4 A
Gate-source charge	Q_{GS}	-	0.1	-	nC	
Gate-drain charge	Q_{GD}	-	0.3	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.4	-	V	V_{DS} = 400 V; I_D= 1.4 A

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.7	-	V	V_{GS} = 0 V; I_S = 1.4 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	6	A	V_{GS} = 6 V; t_{PULSE} = 10 µs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S = 1.4 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

8. Electric characteristics diagrams[1]

at T_j = 25 °C, unless specified otherwise

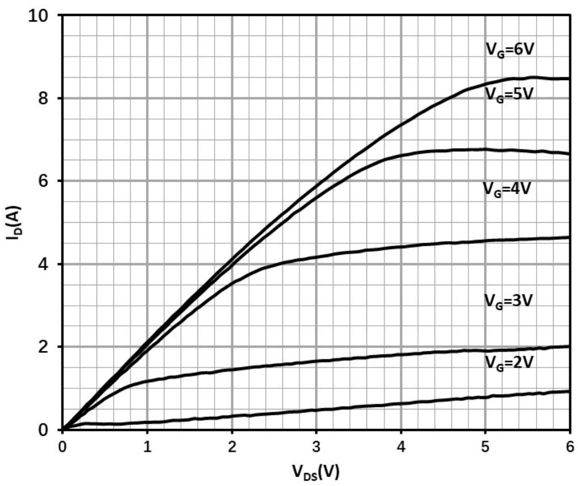
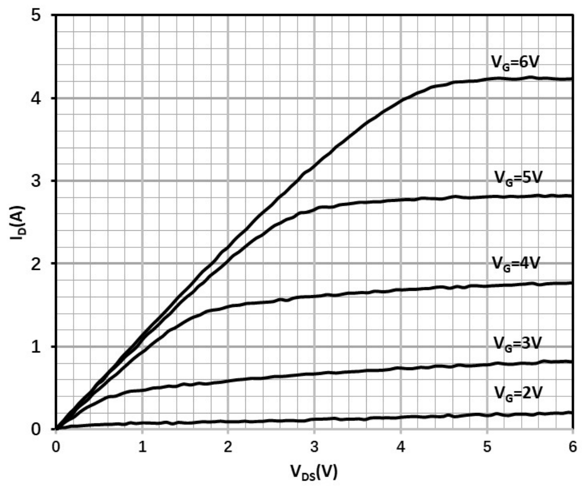
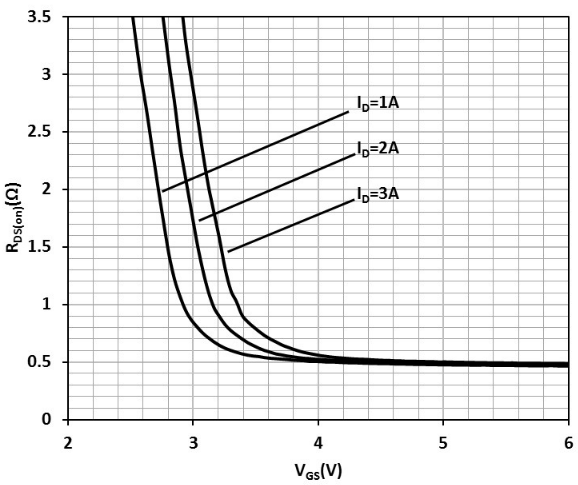
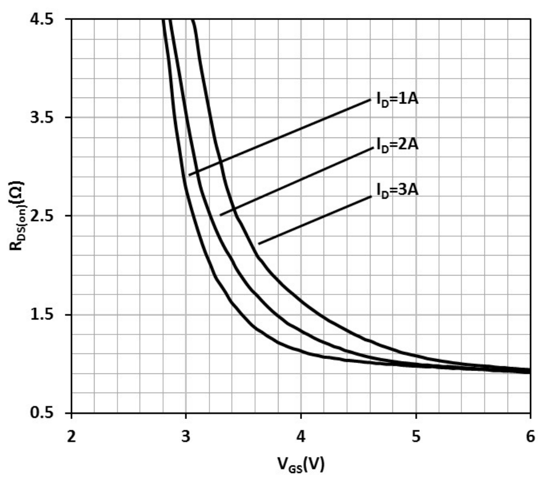
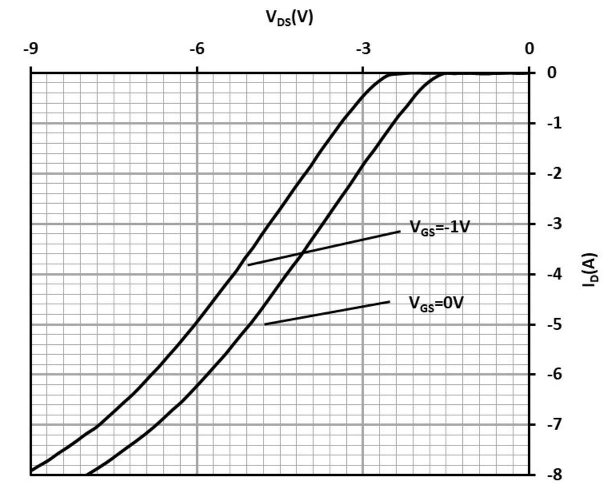
Figure 1 Typ. output characteristics	Figure 2 Typ. output characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance	Figure 4 Typ. Drain-source on-state resistance
	
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C	$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

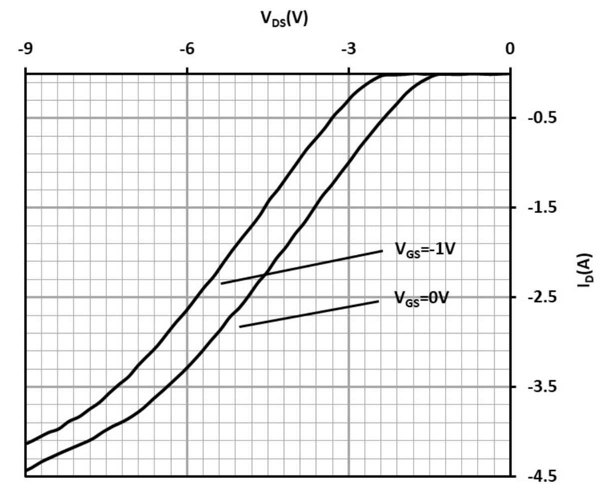
1 The typical electrical characteristic curves were measured with the parts assembled in DFN 5X6 package.

Figure 5 Typ. channel reverse characteristics



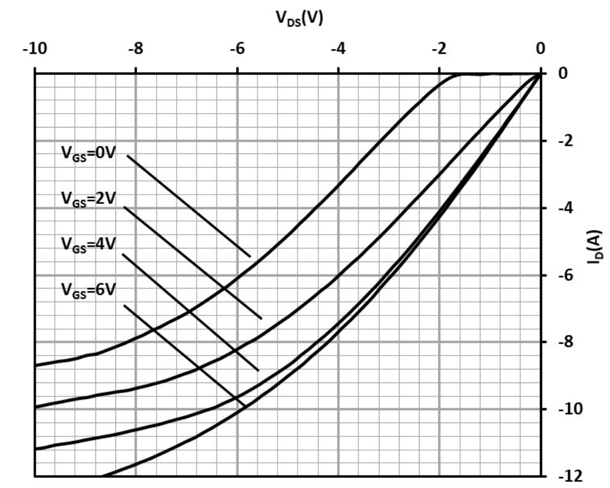
$I_D = f(V_{DS},V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



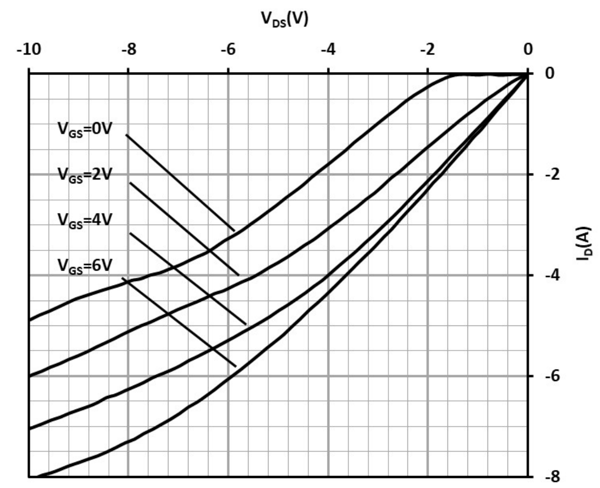
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



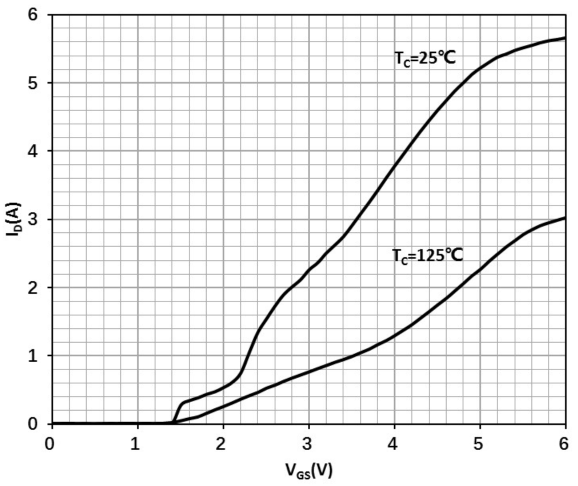
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



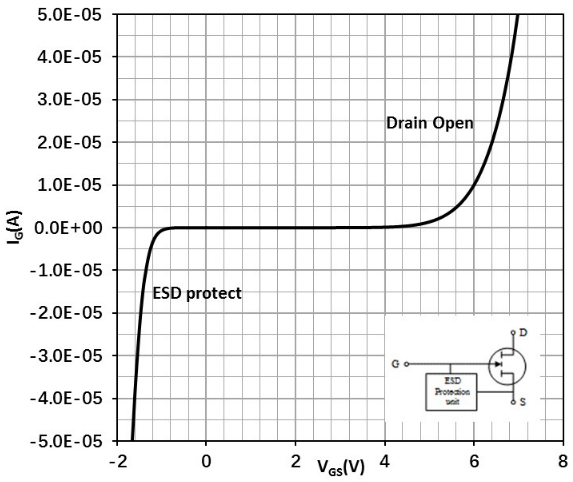
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



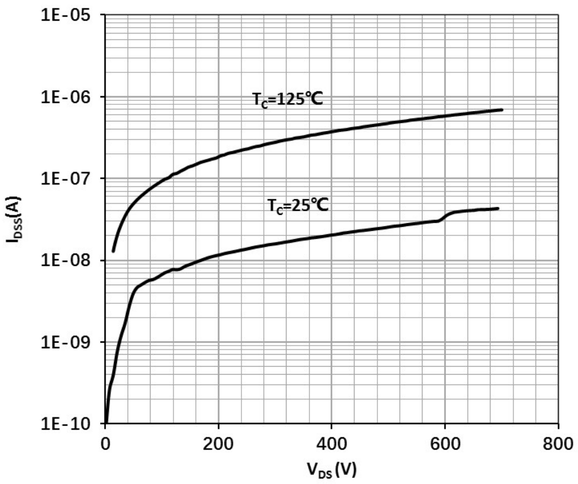
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



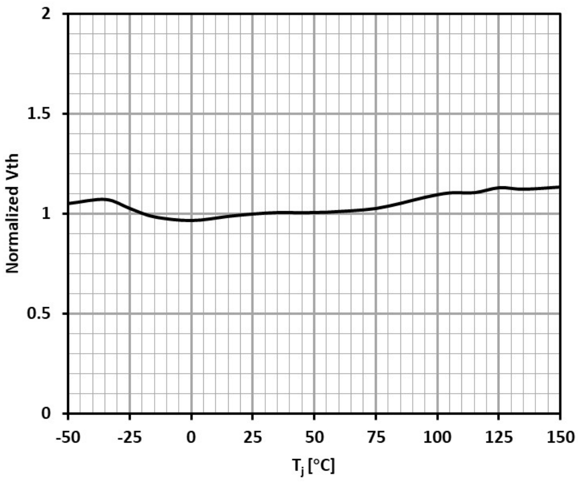
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



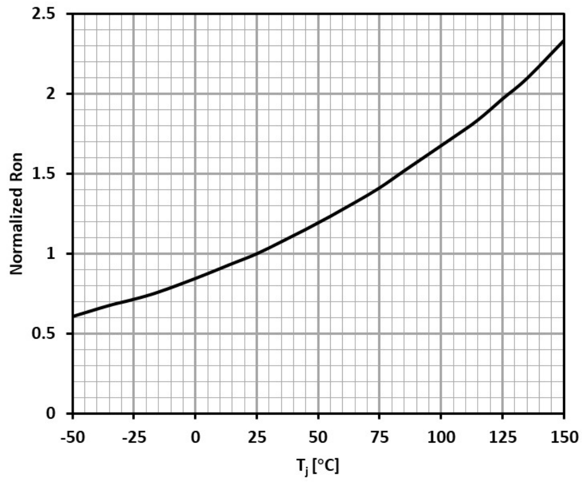
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



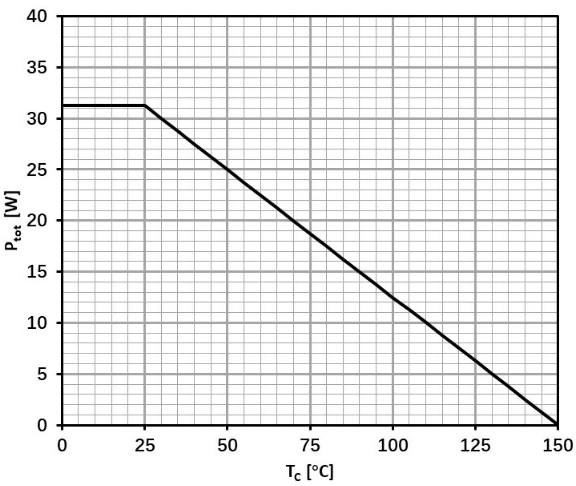
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 3.8$ mA

Figure 13 Drain-source on-state resistance



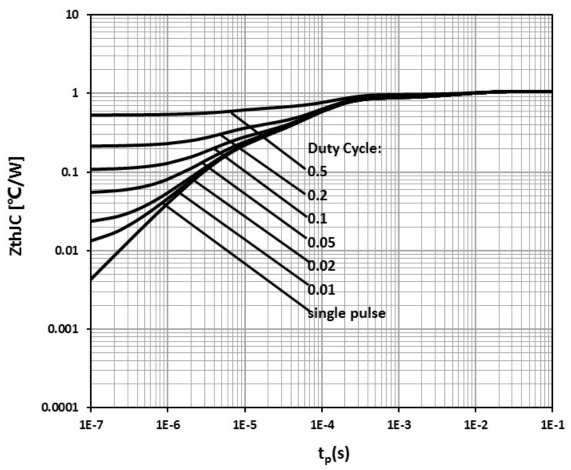
$R_{DS(on)} = f(T_j)$; $I_D = 1.4$ A; V_{GS}=6V

Figure 14 Power dissipation



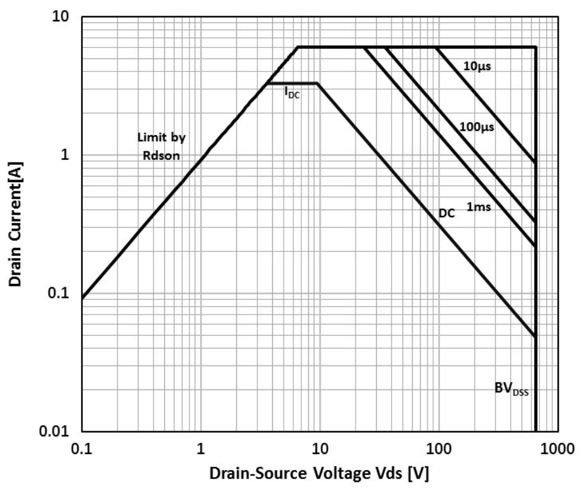
$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



$Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



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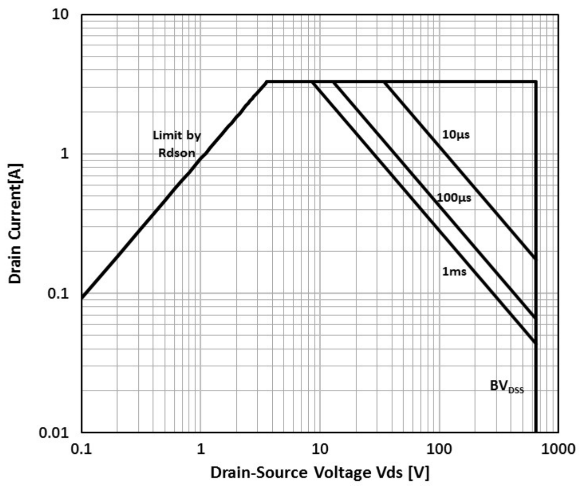
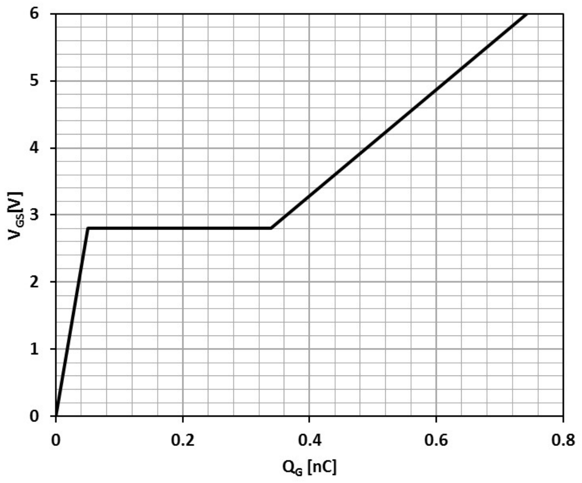
$I_D = f(V_{DS})$; T_C = 25 °C

Figure 17 Safe operating area



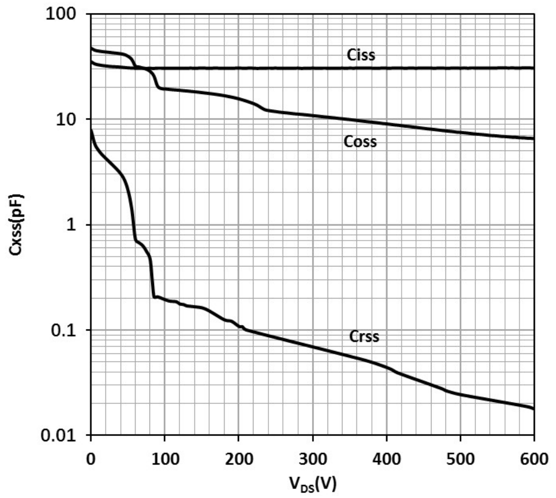
$I_D = f(V_{DS})$; T_C = 125 °C

Figure 18 Typ. gate charge



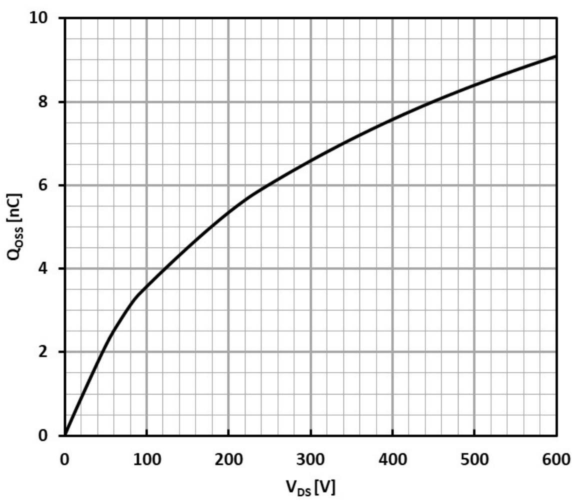
$V_{GS} = f(Q_G)$; V_{DCLINK} = 400 V; I_D = 1.4 A

Figure 19 Typ. capacitances



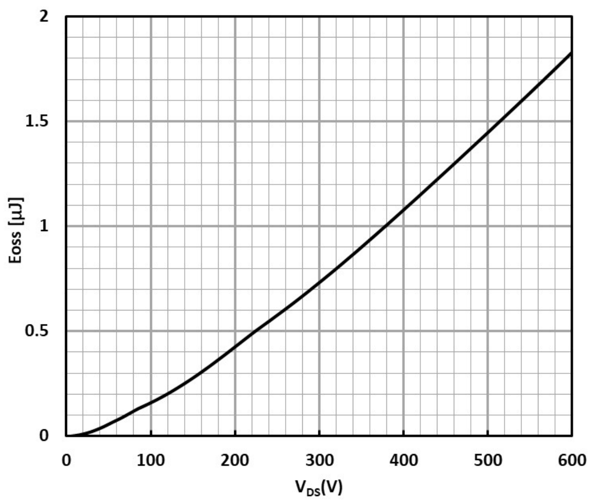
$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 20 Typ. output charge



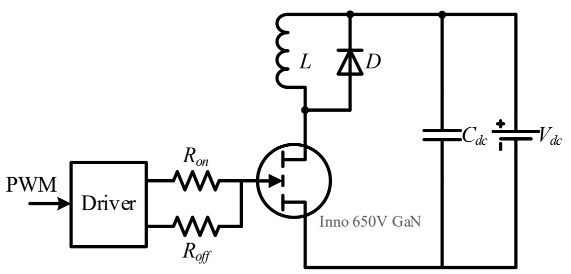
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 21 Typ. C_{OSS} stored Energy



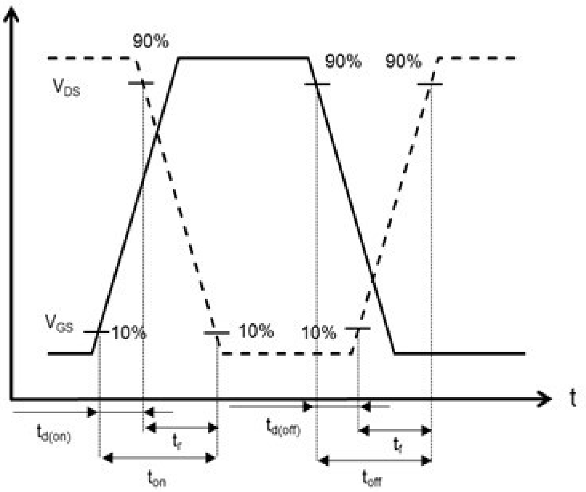
$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load

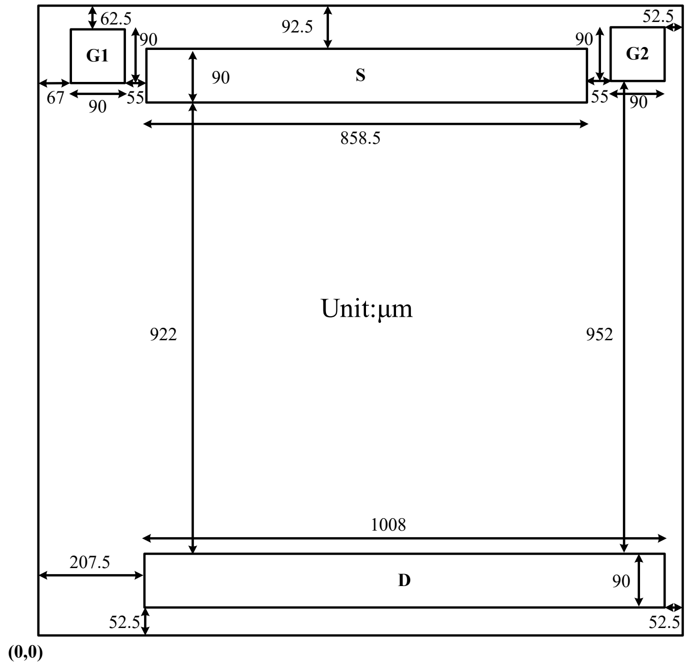


$V_{DS} = 400$ V, $I_D = 2.8$ A, L = 318 μH, $V_{GS} = 6$ V,
$R_{on} = 10\ \Omega$, $R_{off} = 2\ \Omega$

Figure 23 Typ.Switching times waveform



9. Chip drawing



Wafer features

Physical Characteristics		Unit
Wafer Size	8	inches
Wafer Thickness	1150	μm
Die Size (with S/L)	1.35 x 1.33	mm^2
Scribe Street Width	80	μm
Top Metal Materials	Al-Cu	
Top Metal thickness	3.5	μm
Passivation Materials	SiN,SiO_2	
Passivation Thickness	2.1	μm
PI Materials	Polymide	
PI Thickness	10	μm
Gate Pad Size	G1: 90 x 90 G2: 90 x 90	$μm^2$
Source Pad Size	858.5 x 90	$μm^2$
Drain Pad Size	1008 x 90	$μm^2$
TGV	No	
Backside	Silicon	

Note: All the pad size refers to PI top opening size, actual size at PI bottom (top metal exposure) is about 4~8 μm shorter than top opening.

10. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-05-11	1.0 version release

Important Notice