

KTH5701 EVB Manual

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1 Introduction

The KTH5701_EVB board is designed for performance evaluation and testing of the CONNTEK KTH5701 3D Hall magnetic sensor. It supports both SPI and I²C communication interfaces. This document describes how to use the board in detail.

2 Hardware Overview

The KTH5701_EVB hardware includes the 3D Hall sensor, decoupling capacitors, I²C pull-up resistors, and pin-header connectors.

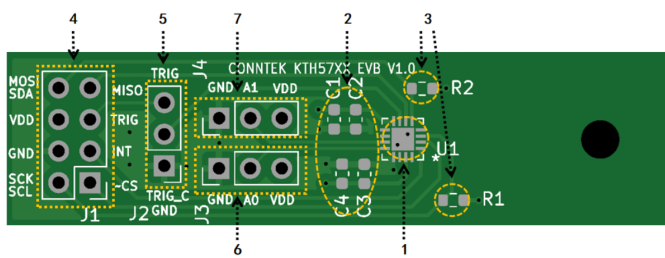


Figure 1 Board Top View

The component descriptions on the board are listed below.

Table 1 Board Component Function List

No.	Ref.	Component	Description
1	U1	KTH5701	3D Hall magnetic sensor IC
2	C1, C2, C3, C4	Decoupling capacitors	Power filtering; C1/C4 are 10 μ F, C2/C3 are 100 nF
3	R1, R2	Pull-up resistors	I ² C bus (SDA/SCL) pull-up resistors, 4.7 k Ω
4	J1	2 \times 4 header	Main signal connector for SPI/I ² C, power, and interrupt signals
5	J2	1 \times 3 header	Jumper to connect TRIG to J1 or GND
6	J3	1 \times 3 header	I ² C address pin A0 configuration, selectable between GND and VDD
7	J4	1 \times 3 header	I ² C address pin A1 configuration, selectable between GND and VDD

3 Schematic

The figure below shows the complete schematic of the KTH5701_EVB board.

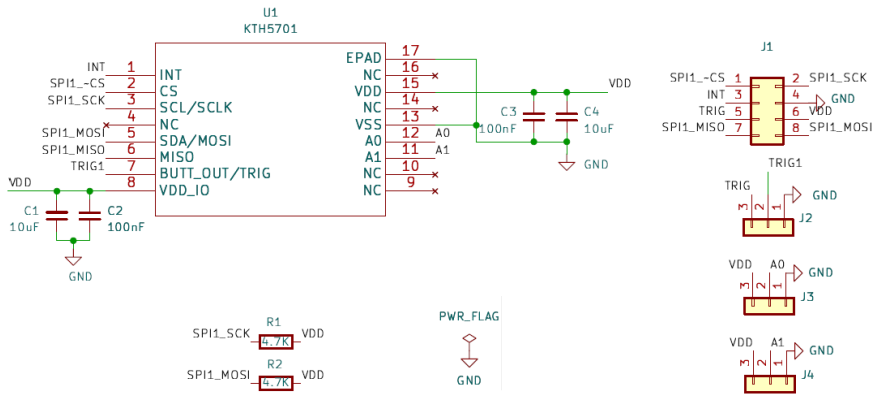


Figure 2 KTH5701_EVB Schematic

4 Mechanical Dimensions

The figure below shows the EVB dimensions. The overall board size is 54.2 mm × 14 mm, and the sensor is placed 20.5 mm from the board edge.

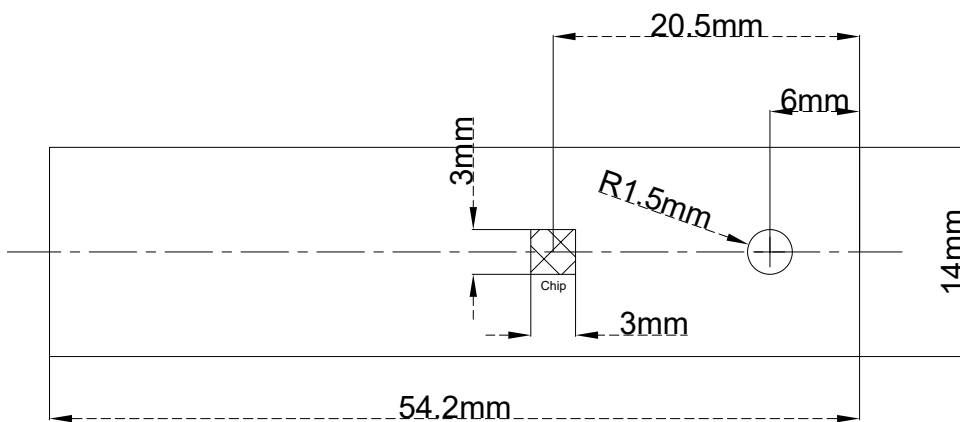


Figure 3 Board Mechanical Drawing

5 Connector Pin Definitions

5.1 J1 Main Signal Connector

J1 is a 2×4 header (2.54 mm pitch) for the main communication and power signals of KTH5701. Each pin function is marked on the PCB silkscreen.

Table 2 J1 Pin Definitions

Pin	PCB Label	Function Description
J1.1	MOSI/SDA	SPI master-out/slave-in signal, multiplexed with I ² C data
J1.2	MISO	SPI master-in/slave-out signal
J1.3	VDD	Sensor supply voltage (2.8V~5.5V)
J1.4	TRIG	Single measurement trigger input, active high; multiplexed with BUTT_OUT button-detection function (configured via J2)
J1.5	GND	Sensor ground
J1.6	INT	Interrupt output signal
J1.7	SCK/SCL	SPI clock signal, multiplexed with I ² C clock
J1.8	~CS	SPI chip select signal (active low)

5.2 J2 TRIG Jumper

J2 is a 1×3 header used to configure the TRIG pin connection of KTH5701.

Table 3 J2 Jumper Definitions

Jumper Position	Function Description
Pin1–Pin2	Connects TRIG to J1 for external host control
Pin2–Pin3	Connects TRIG to GND

5.3 J3/J4 I²C Address Jumpers

J3 and J4 are 1×3 headers used to configure the I²C slave address pins A0 and A1 of KTH5701.

Table 4 J3 (A0) / J4 (A1) Jumper Configuration

Connector	Jumper Position	Function Description
J3 (A0)	Pin1–Pin2	A0 connected to VDD (A0 = 1)
	Pin2–Pin3	A0 connected to GND (A0 = 0)
J4 (A1)	Pin1–Pin2	A1 connected to VDD (A1 = 1)
	Pin2–Pin3	A1 connected to GND (A1 = 0)

I²C address calculation: The 7-bit I²C slave address of KTH5701 is determined by A0 and A1 pin levels. J3 (A0) and J4 (A1) provide four configurable slave addresses. Refer to the KTH5701 datasheet for the exact address values.

6 Functional Description

6.1 I²C Communication

6.1.1 Connection

Connect VDD and GND on J1 to the power supply (2.8V~5.5V), and connect SDA (J1.1) and SCL (J1.7) to the host controller. The board integrates 4.7 k Ω I²C pull-up resistors R1 and R2.

6.1.2 Address Configuration

Set jumper levels on J3 and J4 to configure the I²C slave address A0 and A1.

6.1.3 Procedure

1. Set J3 (A0) and J4 (A1) jumper levels to determine the I²C slave address
2. Connect J1 VDD, GND, SDA (J1.1), and SCL (J1.7) to the host controller
3. After power-up, perform register read/write operations on KTH5701 through I²C

Note: In I²C mode, J1.2 (MISO) and J1.8 (\sim CS) are not used.

6.2 SPI Communication

6.2.1 Connection

Connect VDD and GND on J1 to the power supply (2.8V~5.5V), and connect MOSI (J1.1), MISO (J1.2), SCK (J1.7), and \sim CS (J1.8) to the host controller.

6.2.2 Procedure

1. Connect J1 VDD, GND, MOSI (J1.1), MISO (J1.2), SCK (J1.7), and \sim CS (J1.8) to the host controller
2. After power-up, perform register read/write operations on KTH5701 through SPI
3. \sim CS is active low; the host should pull \sim CS low before communication

Important: SPI and I²C share J1.1 (SDA/MOSI) and J1.7 (SCL/SCK). Only one communication interface can be used at a time. Verify wiring before switching modes.

7 FAQ

Q1: Communication fails after power-up.

- Check whether VDD and GND are correctly connected, and confirm supply voltage is within 2.8V~5.5V
- In I²C mode, verify that J3 (A0)/J4 (A1) address settings match the host side
- In SPI mode, verify that ~CS is correctly driven low
- Confirm signal wiring: SDA/MOSI on J1.1 and SCL/SCK on J1.7

Q2: I²C communication is unstable.

- Confirm R1 and R2 pull-up resistors are populated (4.7 k Ω)
- Check for I²C address conflicts on the bus
- Lower the I²C clock speed for testing