KTH7112 Series

16-bit High-Speed High-Precision On-Axis Magnetic Encoder Programmable Multi-Interface Angle Sensor with ABZ/UVW/PWM/SPI/SSI Outputs

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1 Product Information

1.1 Features

The KTH7112 is a high-performance magnetic encoder with the following key features:

- 16-bit high-resolution absolute angle output
- On-axis application supported, with post-calibration INL error less than $\pm 0.1^\circ$
- Supports both single-pole and multi-pole magnetic sources
- Ultra-low latency with a data update rate of 1 μs
- SPI communication interface with data rates up to 10 Mbps
- SSI interface supporting up to 5 Mbps for angle output
- Programmable ABZ incremental output with 4 to 16384 steps per revolution
- Programmable UVW output for 1 to 32 pole pairs
- 12-bit PWM angle output, frequency adjustable, supports calibration status indication
- Built-in MTP (Multi-Time Programmable) memory for parameter storage
- Operating voltage: from 3.3 V to 5 V
- Operating temperature range: -40°C to 125°C
- Package: QFN3x3-16L

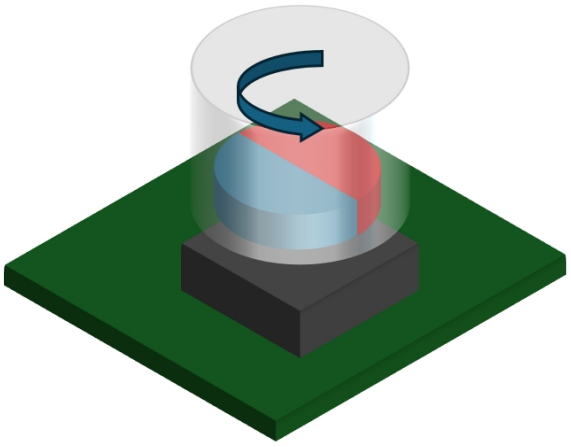

Figure 1: On-axis Configuration Example

1.2 Typical Applications

- Absolute angular position detection
- Brushless DC motor control

- Closed-loop stepper motor control systems
- Platform automatic door systems in rail transportation

1.3 General Description

The KTH7112 is a high-speed, high-precision magnetic encoder equipped with an advanced automatic nonlinearity calibration (ANLC) engine.

Users can initiate the calibration either by register configuration or via external pin trigger. The internal controller automatically measures nonlinear errors and calculates the compensation parameters. The calibration results are stored in internal MTP (Multi-Time Programmable) memory.

This calibration mechanism requires no external computation and can significantly enhance the linearity of angle measurement, achieving absolute accuracy better than $\pm 0.1^\circ$.

The encoder supports multiple interface modes to suit various applications:

- **SPI Interface:** A 3-wire SPI bus (CPOL=1, CPHA=1) is provided for reading 16-bit angle data, accessing internal registers, and configuring parameters. Data transmission includes an 8-bit CRC for error checking. This SPI interface does not support multiple CS lines; instead, multiple SDA lines can be connected to a microcontroller for data access.
- **ABZ Incremental Output:** Programmable ABZ quadrature signal output with resolutions up to 16384 steps/rev. It supports absolute position initialization upon power-up by emitting a sequence of AB pulses.
- **SSI Interface:** Supports two-wire synchronous serial communication with up to 5 Mbps data rate for absolute angle output.
- **PWM Output:** Offers a PWM signal with adjustable frequency (120 Hz to 3.8 kHz), and uses pulse width modulation to indicate angle or calibration status.
- **UVW Commutation Signal:** Programmable commutation outputs for 1 to 32 pole-pair configurations, ideal for BLDC applications.

These interface modes provide flexible and robust integration options for a wide range of system designs.

2 System Overview

2.1 System Architecture

The KTH7112 integrates Hall sensors, analog front-end, analog-to-digital converters, and a digital signal chain to perform angle measurement and output digital signals.

The Hall sensors detect magnetic fields and generate analog voltages. These are converted into two orthogonal digital signals via ADCs. The

angle is calculated using an arctangent (ATAN) module, producing a 16-bit angle value. The angle is then processed through zero offset, rotation direction setting, and filtering.

Filtered angle data can be output directly via SPI or SSI interfaces. Alternatively, the angle can be converted into PWM signals based on duty cycle.

To enhance refresh rate, the filtered angle passes through an interpolator and is then output to the ABZ encoder module, which converts angle into quadrature incremental signals.

All system parameters are stored in non-volatile multi-time programmable (MTP) memory. Parameters can be configured via the SPI interface.

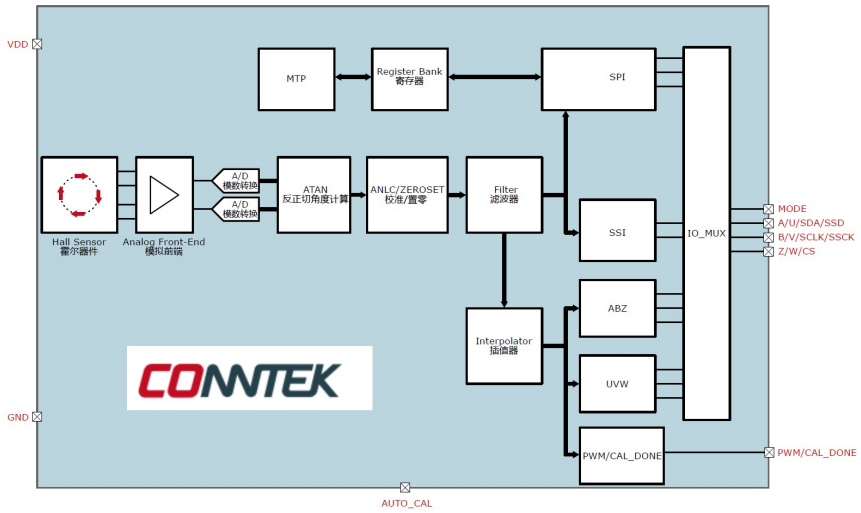

Figure 2: Functional Block Diagram

2.2 Recommended Application Circuit

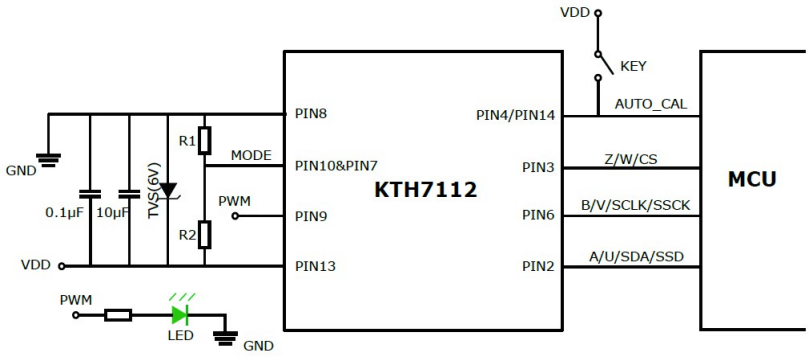

Figure 3: Recommended Application Circuit

- R1 and R2 are 5.1 kΩ pull-up resistors. Soldering R1 only enables 3-wire SPI. Soldering R2 only enables ABZ/UVW/SSI output.
- AUTO_CAL pin can be externally triggered.
- PWM output can be connected to an LED to indicate calibration completion.

- PIN7 and PIN10 are both MODE pins and must be connected together with pull-up/pull-down resistors.
- PIN4 and PIN14 are both AUTO_CAL pins. Either one can be used or neither needs to be connected.

2.3 Pin Definition

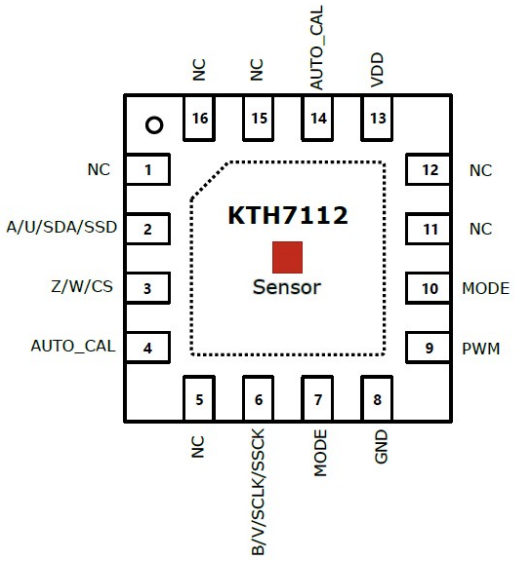

Figure 4: QFN-16L Package Pinout

Pin	Name	Function
1	NC	No connection, IO must be floating
2	A/U/SDA/SSD	Function defined by MODE and IO_MUX
3	Z/W/CS	Function defined by MODE and IO_MUX
4	AUTO_CAL	External calibration trigger interface, active high
5	NC	No connection, IO must be floating
6	B/V/SCLK/SSCK	Function defined by MODE and IO_MUX
7	MODE	Interface output control
8	GND	Ground
9	PWM	Duty cycle output
10	MODE	Interface output control
11–12	NC	No connection, IO must be floating
13	VDD	Power supply
14	AUTO_CAL	External calibration trigger interface, active high
15–16	NC	No connection, IO must be floating
17	T-PAD	Thermal pad, connect to GND

Table 1: Pin Functions of KTH7112

2.4 Interface Output Selection

The interface output of KTH7112 is jointly controlled by PIN2 and the IO_MUX register (detailed in Chapter 4, register address 0x10). It can output 3-wire SPI, ABZ, UVW, SSI, with specific specifications as follows:

PIN and Register	State	State	State	State
PIN10:MODE	Low level	High level	High level	High level
IO_MUX[2:0]	Any	0	1	2
PIN2	SDA	A	U	SSD
PIN6	SCLK	B	V	SSCK
PIN3	CS	Z	W	Z

Table 2: Interface Output Selection

The output status of KTH7112's output interfaces PIN2, PIN6, PIN3 is jointly determined by the input status of PIN2 MODE and the IO_MUX register. When MODE input is low, PIN2, PIN6, PIN3 are 3-wire SPI interfaces. When MODE input is high, if the IO_MUX register is set to 0, it is ABZ output (default value); if the IO_MUX register is set to 1, it is UVW output; if the IO_MUX register is set to 2, it is SSD output.

2.5 16-bit Binary Angle Encoding

The angle is represented using a 16-bit binary value ranging from 0 to 65535, which corresponds to 0° to 360°.

$$\text{Angle (degrees)} = \frac{\text{Binary Value} \times 360}{2^{16}}$$

All angle outputs in this datasheet use this encoding format unless otherwise specified.

3 Key Parameters

Parameter	Min	Typ	Max
Supply Voltage	3.0 V	3.3 V	5.0 V
Magnetic Field Strength	30 mT	60 mT	150 mT
Operating Current	—	16 mA	—
Start-up Time	—	20 ms	—
Data Latency	—	1 μs	—
Output Noise (1 sigma)	—	0.015°	—
Integral Nonlinearity	—	$\pm 0.1^\circ$	—
Maximum Rotational Speed	—	—	120000 rpm
ESD Protection (HBM)	—	± 5 kV	—

Table 3: Key Electrical and Performance Parameters @ 3.3 V Supply

4 Magnet Installation Guide

4.1 On-Axis Magnet Installation

Parameter	Description	Min	Typ	Max	Unit
D_{mag}	Diameter of radially magnetized magnet	—	10	30	mm
T_{mag}	Recommended magnet thickness	—	2.5	5	mm
B_{pk}	Magnetic field at chip location	30	—	150	mT
A_G	Air gap	—	1.0	5.0	mm
R_S	Rotational speed	—	—	120	krpm
Δ_{disp}	Installation offset tolerance	—	0	1.0	mm
TC_{mag1}	NdFeB magnet temperature coefficient	—	−0.120	—	%/°C
TC_{mag2}	SmCo magnet temperature coefficient	—	−0.035	—	%/°C

Table 4: On-Axis Magnet Installation Recommendations

- Recommended magnetic materials: NdFeB or SmCo.

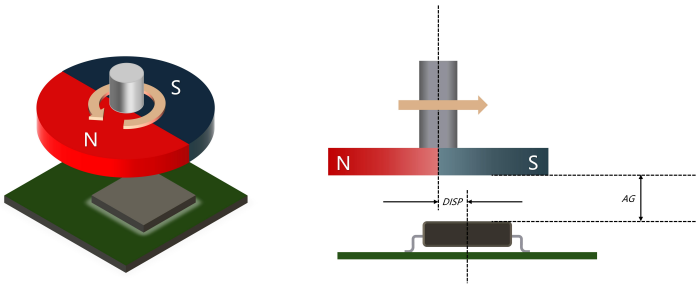

Figure 5: Recommended Chip Placement for On-Axis Magnet

5 Register Configuration

5.1 Register Map

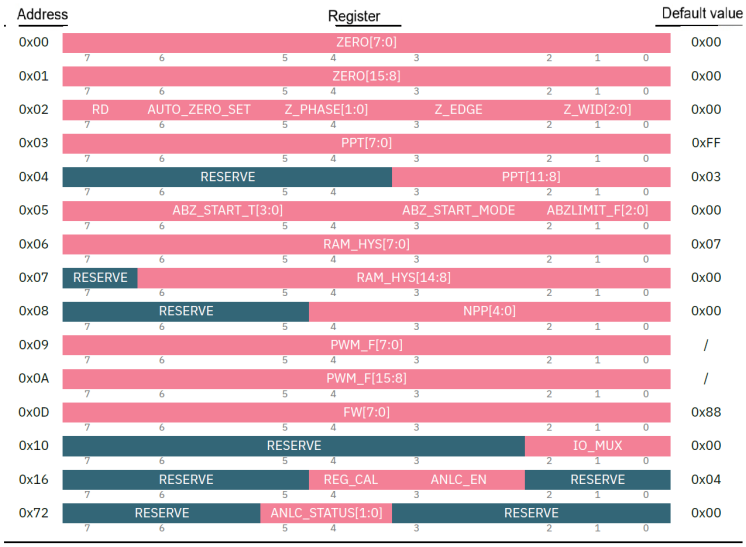

Figure 6: Detailed Register Bit Field Layout

5.2 Register Description

Symbol	Default (dec)	Description
ZERO[15:0]	0	Zero angle offset setting
RD	1	Rotation direction: 1 for CW
AUTO_ZERO_SET	0	Set to 1 to force output angle to zero
Z_PHASE[1:0]	0	Z signal phase for ABZ
Z_EDGE	0	0: rising edge of Z at zero angle, 1: falling edge
Z_WID[2:0]	0	Z signal width in LSBs
PPT[11:0]	1023	ABZ resolution, default 1024 lines (4096 steps/rev)
ABZ_START_T[3:0]	2	ABZ output delay, default 20ms
ABZ_START_MODE	0	1: absolute ABZ startup mode
ABZLIMIT_F[2:0]	0	ABZ max frequency limit, default 16MHz
RAM_HYS[14:0]	7	Hysteresis configuration for angle output
NPP[4:0]	0	UVW pole pair count, default 1
PWM_F	—	PWM output frequency (factory calibrated to 1kHz)
FW[7:0]	136	Filter depth control
IO_MUX	0	0: ABZ, 1: UVW, 2: SSI output
REG_CAL	0	Set to 1 to initiate self-calibration
ANLC_EN	1	Enable calibration effect on angle output
ANLC_STATUS[1:0]	0	0: Not started
RESERVE	0	Reserved, do not modify

Table 5: Register Parameter Descriptions

6 SPI Interface

KTH7112 employs a three-wire SPI communication protocol, operating in Mode 3 (CPOL $= 1$, CPHA $= 1$). This serial interface allows reading the absolute angle, accessing internal registers, and programming the MTP (Multiple-Time Programmable) memory. The maximum supported SPI communication speed is 10 Mbps.

6.1 SPI Timing

The SPI timing diagram is shown in Figure 7. All timing parameters are measured under a load condition of 20 pF.

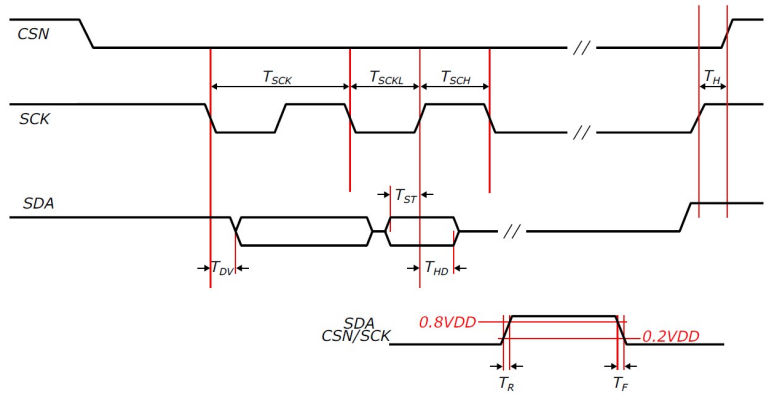

Figure 7: SPI Timing Diagram

Table 6: SPI Timing Parameters (20 pF Load)

Symbol	Description	Min (ns)	Typ (ns)	Max (ns)
T_{SCK}	SCK clock period	100	—	—
T_{SCKL}	SCK low-level period	50	—	—
T_{SCKH}	SCK high-level period	50	—	—
T_H	SCK rising edge to CSN rising edge interval	120	—	—
T_R	Digital signal rise time	—	10	—
T_F	Digital signal fall time	—	10	—
T_{DV}	MISO data valid time	—	—	50
T_{ST}	MOSI data setup time	50	—	—
T_{HD}	MOSI data hold time	50	—	—

These parameters are crucial for defining the SPI communication timing requirements. Adhering to these specifications in hardware and firmware design is essential to ensure reliable data transfer between the KTH7112 product's microcontroller and peripheral devices.

6.2 Reading Absolute Angle via SPI

The steps for reading the angle are as follows:

1. Send command: 8-bit $(0x00)$
2. Receive data: 16-bit data + 8-bit CRC
3. The number of SCLKs sent for reading the angle can be adjusted according to your needs. For example, sending an 8-bit angle reading command, or only sending 8 SCLKs to read the high 8 bits of the angle, is also supported by the chip.
4. The interval between two SPI communications needs to be greater than 150 ns
5. CRC check adopts CRC-8/ITU standard:
   - Polynomial: $x^8 + x^2 + x + 1$ $(0x07)$
   - Initial value: $0x00$
   - Result XOR value: $0x55$

Figure 8: SPI Read Angle Sequence

6.3 Register Access Control

KTH7112 implements a locking mechanism for write access to its registers to ensure safe operation.

- Upon power-up, registers are locked and cannot be modified.
- Send 32-bit unlock key: `0x20240101`
- Send 32-bit lock key: `0x20241231` to re-enable protection
- Register and angle read operations are always allowed

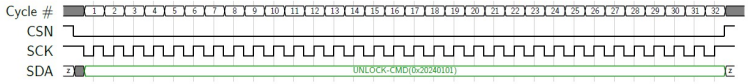

Figure 9: Unlocking Registers via SPI

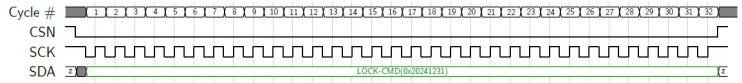

Figure 10: Locking Registers via SPI

6.4 Reading Registers

The operation steps for reading registers:

1. Send command: 8-bit $0x11$ + 8-bit register address
2. Receive data: 8-bit register value + 8-bit CRC
3. The high 16 bits are the read command input sent to the chip, and the low 16 bits are the returned register value and CRC check code
4. The interval between two SPI communications needs to be greater than 150 ns

Figure 11: Register Read Operation via SPI

6.5 Writing Registers

The operation steps for writing registers:

1. First, you need to send the unlock code (32'h20240101)
2. Send command: 8-bit $0x33$ + 8-bit register address + 8-bit write value
3. Receive data: 8-bit register value (New feature: returns the value written to the register in the same frame)
4. The 24th SCLK high-level duration must be greater than 100 ns

Important timing requirements:

- The interval between two SPI communications needs to be greater than 150 ns
- After the register write command, you must wait at least 100 ns before reading the return value

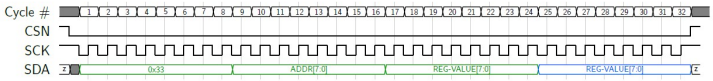

Figure 12: Register Write Operation via SPI

6.6 Writing Registers to MTP

All register writes are volatile unless explicitly saved to MTP (non-volatile memory). Use the following steps to burn MTP:

1. Ensure register access is unlocked
2. Send 24-bit MTP burn command: `0x2255AA`
3. Wait at least 400 ms before any further SPI operation

Important precautions:

- MTP write is irreversible
- Validate all parameters before writing
- Do not power off during programming
- Use only verified and tested firmware for MTP operations

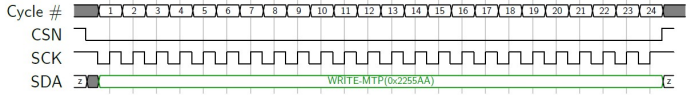

Figure 13: Writing Registers to MTP via SPI

7 SSI Interface

KTH7112 supports the SSI (Synchronous Serial Interface) protocol for absolute angle readout.

The device functions as an **SSI slave** and exclusively supports **angle data transmission only**. **Register read or write operations are not supported via SSI**. The transmitted data is **MSB-first**, meaning the most significant bit of the angle data is sent first.

7.1 Timing Diagram

The standard SSI interface uses two signal lines:

- **SSCK**: Clock input from the master
- **SSD**: Serial data output from the sensor

The timing relationship between SSCK and SSD is shown in Figure 14.

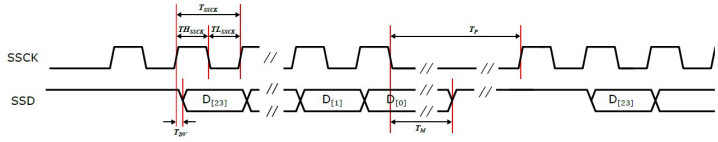

Figure 14: SSI Timing Diagram

7.2 Timing Parameters

The electrical timing requirements for SSI communication are shown in Table 7. These values ensure proper synchronization between the host controller and the KTH7112 device.

Table 7: SSI Timing Parameters

Symbol	Description	Min	Max	Unit
t_{DV}	SSD data valid delay	—	15	ns
T_{SSCK}	SSCK clock period	0.2	10	μs
T_{LSSCK}	SSCK low level duration	0.1	5	μs
T_{HSSCK}	SSCK high level duration	0.1	5	μs
T_M	Monoflop timeout	10	—	μs
T_P	Inter-frame pause time	16	—	μs

7.3 Data Frame Format

Each SSI data frame consists of:

- 16-bit absolute angle value
- 8-bit CRC code using the CRC-8/ITU standard

Data is shifted out synchronously on the falling edge of SSCK, with MSB transmitted first.

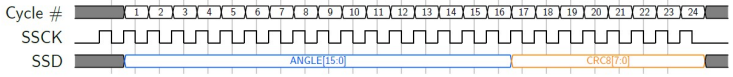

Figure 15: Standard SSI Angle Read Sequence

8 ABZ Interface

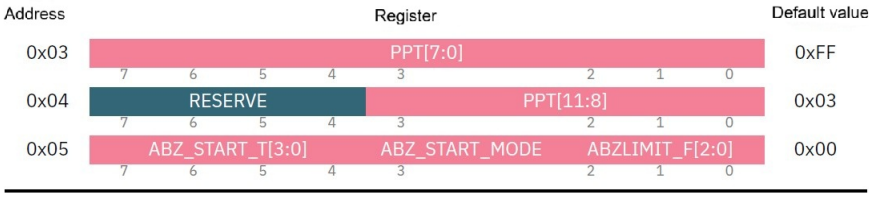

Figure 16: ABZ Output Related Register Settings

KTH7112 provides angular position output through the incremental ABZ interface. The interface is configured for 14-bit resolution, corresponding to 16384 steps per revolution, or 4096 pulse periods (PPT) per revolution on the AB signals.

The phase difference between signals A and B indicates the direction of rotation. In clockwise rotation, signal A leads and signal B follows. In counterclockwise rotation, signal B leads and signal A follows. During power-on, all three ABZ signals are held high.

When the magnet above the center of the chip (viewed from top) rotates counterclockwise (CCW), the rising edge of signal B leads that of signal A by $1/4$ cycle. Conversely, during clockwise (CW) rotation, the rising edge of signal A leads that of signal B by $1/4$ cycle. The phase relationship between A and B reverses as the rotation direction changes.

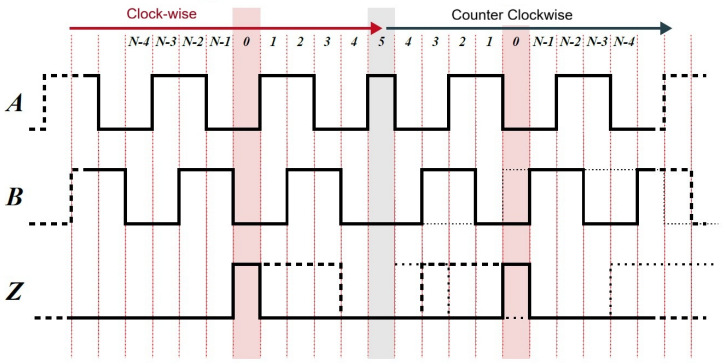

Figure 17: ABZ Output Timing Diagram

8.1 ABZ Output Resolution

The ABZ incremental interface of KTH7112 can support any integer resolution up to 4096 pulse periods per revolution. Users can program the internal MTP field `PPT[13:0]` to set a custom resolution. Common values are shown below:

Table 8: ABZ Resolution vs. PPT Settings

PPT(11:0)	Pulse/Rev (PPT)	Steps/Rev
0	1	4
1	2	8
2	3	12
⋮	⋮	⋮
4093	4094	16376
4094	4095	16380
4095	4096	16384

8.2 ABZ Output Frequency Limiting

The maximum AB edge output frequency is 16 MHz. This can be reduced by configuring the `ABZLIMIT` parameter, as shown below:

Table 9: ABZ Frequency Limit Settings

ABZLIMIT	Max Edge Frequency
0	16 MHz
1	8 MHz
2	4 MHz
3	2 MHz
4	1 MHz

8.3 ABZ Startup Mode

KTH7112 supports two ABZ startup modes, selectable via the `ABZ_START_MODE` register:

- **Normal startup** (`ABZ_START_MODE` $= 0$): ABZ signals output incremental pulses immediately after power-on.
- **Absolute startup** (`ABZ_START_MODE` $= 1$): ABZ outputs a burst of pulses indicating the absolute position at startup.

In absolute startup mode, one clock after `ABZ_EN` is enabled, the device captures the current angle as an absolute position. It then outputs a series of AB pulses to represent this angle.

$$\text{Pulse Count} = \left(\frac{\min(\text{Angle}, 65536 - \text{Angle})}{65536} \right) \times \text{PPT}$$

For example, if the angle is $90°$ (16384 in count) and PPT $= 511$, then AB outputs 128 pulses. If the angle is greater than $180°$, the AB output is reversed, counting down from $360°$.

8.4 ABZ Startup Delay

The ABZ startup delay can be configured using the `ABZ_START_T[3:0]` register. Typical settings are:

Table 10: ABZ Startup Delay Settings

ABZ_START_T[3:0]	Delay Time
1	10 ms
2	20 ms (default)
3	30 ms
4	40 ms
5	50 ms
6	75 ms
7	100 ms

This setting helps prevent false ABZ signals during system power-up instability.

9 UVW Output

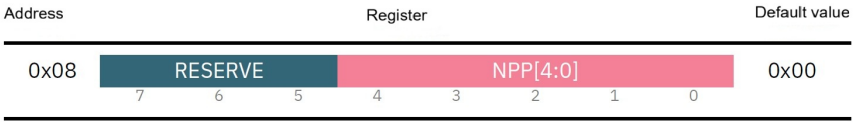

Figure 18: UVW Output Register Configuration

UVW output signals simulate three Hall switches used for commutation in three-phase motors. As shown in Figure 19, the three logic signals have 50% duty cycle and 120° phase difference.

If the motor has more pole pairs than the target magnet, KTH7112 can divide one electrical rotation into multiple commutation steps to generate multiple UVW periods.

The parameter register `0x7` uses `NPP[4:0]` to configure the simulated pole-pair number and UVW switching step angle.

Table 11 describes the NPP configuration:

For example, with a four-pole (two pole-pair) motor, the UVW commutation step is 30° per state, as shown in Figure 20.

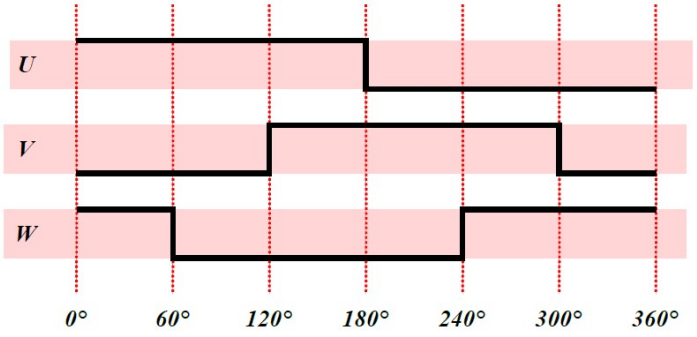

Figure 19: UVW Output for One Pole Pair

Table 11: UVW Pole-Pair Configuration: NPP[4:0]

NPP(4:0)	Pole Pairs	States Per Turn
00000	1	6
00001	2	12
00010	3	18
00011	4	24
00100	5	30
00101	6	36
00110	7	42
00111	8	48
⋮	⋮	⋮
11110	31	186
11111	32	192

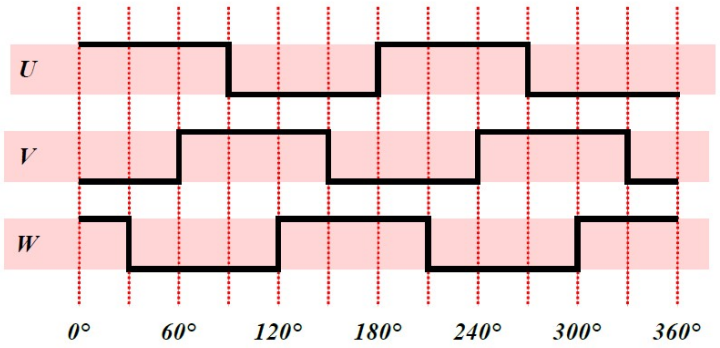

Figure 20: UVW Output for Two Pole Pairs

9.1 UVW Startup Delay

The startup timing of UVW output is the same as ABZ output. It is controlled by the `abz_start_t[3:0]` parameter. This ensures UVW outputs are enabled only after the system becomes stable during power-up.

9.2 UVW and Z Signal Phase Relationship

The UVW signals are phase-aligned with the Z signal edge. This alignment ensures proper commutation synchronization with the electrical zero reference position.

10 PWM Absolute Output

KTH7112 provides a single-wire PWM absolute angle output mode. PWM is the default output function on pin 9, as shown in Figure 21.

Address	Register	Default value
0x09	PWM_F[7:0] (7 6 5 4 3 2 1 0)	/
0x0A	PWM_F[15:8] (7 6 5 4 3 2 1 0)	/

Figure 21: PWM Register Diagram

10.1 PWM Frequency Setting

The PWM output frequency is controlled by the 16-bit parameter `pwm_f`. The relationship between frequency and `pwm_f` is given by:

$$\text{PWM(Hz)} = \frac{(120.284 - 3846.0)}{65536.0} \cdot \text{pwm\_f} + 3846.0$$

Typical settings:

- `pwm_f` = 0: Output frequency is 3846 Hz
- `pwm_f` = 65535: Output frequency is 120.284 Hz

The required frequency accuracy is $\pm 5\%$.

10.2 PWM Resolution and Angle Calculation

The PWM signal duty cycle is proportional to the magnetic angle. The output resolution is 12 bits.

- When duty cycle is $\frac{32}{4096+64}$, the angle is $0°$
- When duty cycle is $\frac{4096+32}{4096+64}$, the angle is $360°$

The formula to calculate angle from duty cycle is:

$$\text{Ang} = \frac{360}{4096}\left(\frac{(4096+64)\cdot t_{\text{ON}}}{t_{\text{ON}} + t_{\text{OFF}}} - 32\right)$$

where:

- t_{ON}: PWM high level time - t_{OFF}: PWM low level time

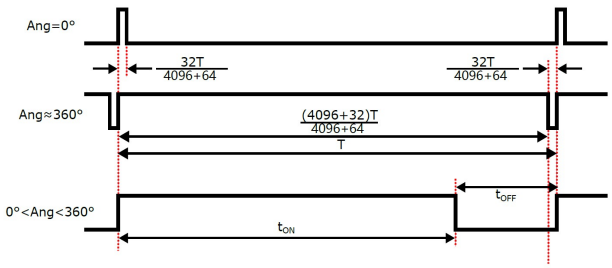

Figure 22: PWM Output Timing Diagram

10.3 PWM Status Indication During Non-Linear Calibration

During automatic nonlinear calibration, the PWM output indicates calibration status:

- 3.8 Hz with 50% duty cycle: calibration in progress
- Constant high level: calibration successful
- Constant low level: calibration failed

After calibration, when the `auto_cal` signal is pulled low, PWM returns to normal angle output mode.

10.4 PWM Startup Delay

The PWM output is also affected by the `abz_start_t[3:0]` parameter. This ensures that PWM signals start only after system stabilization upon power-up.

11 Automatic Nonlinearity Calibration

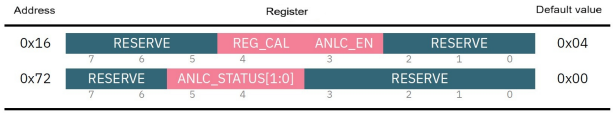

Figure 23: Registers related to ANLC (Auto Nonlinearity Calibration)

KTH7112 includes an automatic nonlinearity calibration (ANLC) function. It effectively compensates for nonlinearity errors that occur due to installation offsets or imperfect magnetic field distribution, improving angle measurement accuracy.

11.1 Calibration Principle

During calibration, the system collects angle error data at 16 evenly spaced points within one full rotation. Using these points, the chip calculates correction parameters and applies real-time output compensation.

During the calibration process, the PWM output flashes at 3.8 Hz with a 50% duty cycle to indicate that calibration is in progress. Once calibration is complete, the PWM output returns to normal operation.

11.2 Calibration Status

The register `ANLC_STATUS[1:0]` reflects the current calibration state:

11.3 Calibration Methods

KTH7112 supports two ways to trigger ANLC:

Table 12: Calibration Status via ANLC_STATUS[1:0]

Value	Description
0	Calibration not started
1	Calibration in progress
2	Calibration failed
3	Calibration completed

1. **Register-triggered:** Set REG_CAL to 1 to start nonlinearity calibration.
2. **Pin-triggered:** Pull the AUTO_CAL pin high and hold for a period. The system will automatically determine whether to perform zero position setting or ANLC based on the angle behavior.

11.4 Calibration Guidelines

To ensure optimal calibration results:

1. Keep the magnetic field stable and avoid movement between the magnet and sensor.
2. Maintain a constant rotation speed during calibration. A recommended speed is 100 to 1000 rpm. Too high or too low speed may affect the result.
3. Perform calibration under actual application conditions to capture real-world error.
4. For off-axis installations, configure GAINTRIM parameters before ANLC.
5. After calibration, parameters are automatically written to MTP and will be retained after power-off.

12 System Operation Settings

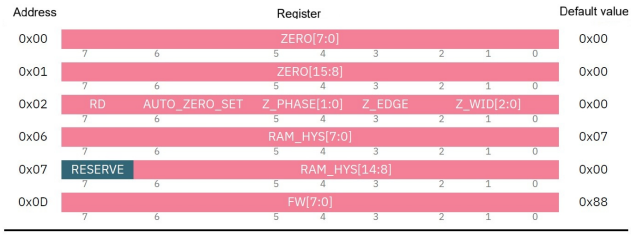

Figure 24: System Operation Related Registers

12.1 Rotation Direction

The rotation direction is configured via the RD bit in register 0x02. It determines whether clockwise or counter-clockwise rotation increases the output angle.

- When `RD = 1` (default): Viewed from above the chip, clockwise rotation increases the output angle.
- When `RD = 0`: Counter-clockwise rotation increases the output angle.

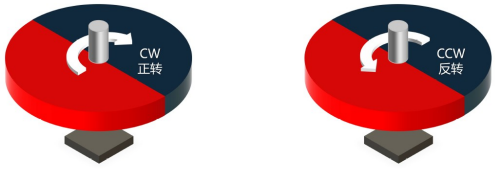

Figure 25: Rotation Direction and Angle Output Relationship

12.2 Zero Position Setting

The chip supports both automatic and manual zero alignment.

12.2.1 Automatic Zero Setting

Method 1: Register Triggered Setting `AUTO_ZERO_SET = 1` will trigger zero alignment. The chip executes:

1. Calculate:

$$\texttt{zero\_set\_angle} = \begin{cases} \texttt{ZERO} - \texttt{angle}, & \texttt{if RD = 1} \\ \texttt{ZERO} + \texttt{angle}, & \texttt{if RD = 0} \end{cases}$$

2. Write result to `ZERO[15:0]` register.
3. Write to MTP.
4. `AUTO_ZERO_SET` bit clears automatically.

Method 2: Pin Triggered Pulling `AUTO_CAL` pin high for more than 2 s will trigger zero setting:

- The chip captures the current angle as zero.
- Writes it to MTP memory.

12.2.2 Manual Zero Position Setting

Manual zero setting is implemented by directly writing to the `ZERO[15:0]` register.

- Register range: 0 to 65535, representing $0°$ to $360°$
- Written value takes effect immediately and affects all output interfaces
- Value is volatile and will be lost on power-off unless saved via MTP programming

The effect of the ZERO value on angle output is as follows:

- If `RD = 0`:

$$\text{Angle}_{\text{out}} = \text{Angle}_{\text{raw}} - \text{ZERO}$$

- If `RD = 1`:

$$\text{Angle}_{\text{out}} = \text{Angle}_{\text{raw}} + \text{ZERO} - 65536$$

Table 13: Comparison of Zero Setting Methods

Method	Advantages	Disadvantages
Register-based ZERO setting	Simple operation, automatic saving, no communication required	Requires SPI access
AUTO_CAL pin based setting	No communication, easy to use	Requires additional control pin
Manual ZERO register setting	High accuracy, flexible setting	Must be saved via SPI, more complex

The `ZERO[15:0]` register defines the zero position and applies to all output types with 16-bit resolution.

ZERO Value Calculation

- If `RD = 1`:

$$\texttt{ZERO} = 2^{16} - \left(\frac{\text{Desired Angle}}{360^\circ} \times 2^{16}\right) + 1$$

- If `RD = 0`:

$$\texttt{ZERO} = \left(\frac{\text{Desired Angle}}{360^\circ} \times 2^{16}\right)$$

Example If RD = 1 and SPI outputs 16384 (i.e., 90°), set `ZERO = 49152`, output becomes 0° If RD = 0 and SPI outputs 16384, set `ZERO = 16384`, output becomes 0°

12.3 Hysteresis

Hysteresis refers to the introduction of lag effects on output signals to prevent false switching and improve the system's anti-interference capability. Lag means that the output signal must exceed a specific threshold before it can change its state. This lag effect can effectively reduce noise and other interference effects on the output signal. When the input signal changes, the output signal will not immediately follow the change, but needs to exceed a threshold before changing state. This threshold setting makes the system insensitive to small amplitude noise and interference, thereby improving the stability and accuracy of the system.

The hysteresis function is effective for all output interfaces.

Hysteresis parameters can be configured through the `RAM_HYS[14:0]` register, $1\,\text{LSB} = \frac{360^\circ}{32768} \approx 0.01099^\circ$. The default value is 7, which is approximately 0.07693°. By introducing output hysteresis, errors can be reduced and the anti-interference capability of the system can be improved. This is very important for applications that require high precision and stability, especially in noisy environments or situations with interference.

Table 14: Hysteresis Parameter Configuration Table

RAM_HYS[14:0]	Hysteresis Angle (°)	Description
0	0	No hysteresis
1	0.01099	Minimum hysteresis
2	0.02197	
4	0.04395	
7	0.07693	Default
8	0.08789	
16	0.17578	
32	0.35156	
64	0.70313	
128	1.40625	Maximum hysteresis

The hysteresis angle is calculated as:

$$\text{Hysteresis Angle} = \frac{\texttt{RAM\_HYS} \times 360^\circ}{32768}$$

12.4 Digital Filter

The depth of the digital filter affects both noise immunity and system dynamic response. It is configured by the `FW[7:0]` register.

- Higher filter level → higher effective resolution
- Lower filter level → faster response
- Default value: `0x88`

Table 15: Effective Resolution vs. Filter Depth

FW[7:0]	Filter Level	Effective Resolution (bit)
0x00	0	9.5
0x11	1	10
0x33	3	11
0x77	7	12
0x88	8	13
0xAA	10	14
0xFF	15	15

13 Product Selection Guide

Table 16: Product Selection Table

Model	Noise (1 sigma)	Output Interface	Time Constant τ (ms)	Operating Magnetic Field	Application
KTH7112	0.015°	SPI, SSI, PWM, ABZ	0.51	30–150 mT	Industrial Automation

14 Ordering Information

Table 17: Ordering Information

Model	Package Type	Operating Temperature	Application	Number of Pins	CRC Check
KTH7112-QN16	QFN3×3-16L	−40°C to 125°C	Industrial Automation	16	No

15 QFN-16L Package Information

15.1 Package Drawing

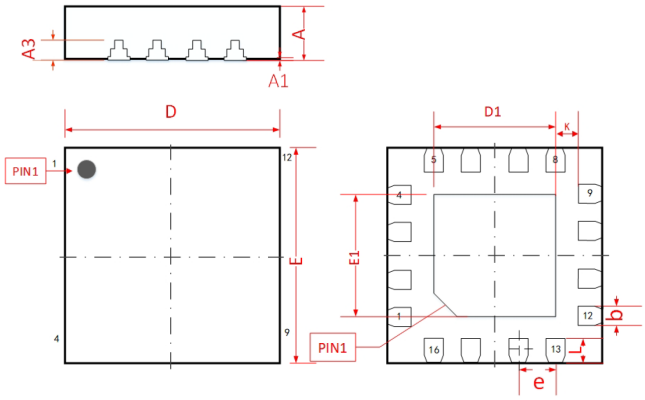

Figure 26: QFN-16L Mechanical Drawing

15.2 Mechanical Dimensions

Table 18: QFN-16L Package Dimensions (Unit: mm)

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
D		3.00 BSC	
E		3.00 BSC	
D1	1.50	1.65	1.80
E1	1.50	1.65	1.80
k		0.385 BSC	
b	0.18	0.24	0.30
e		0.50 BSC	
L	0.19	0.29	0.39

—

16 QFN-16L Tape and Reel Information

16.1 Package Drawing

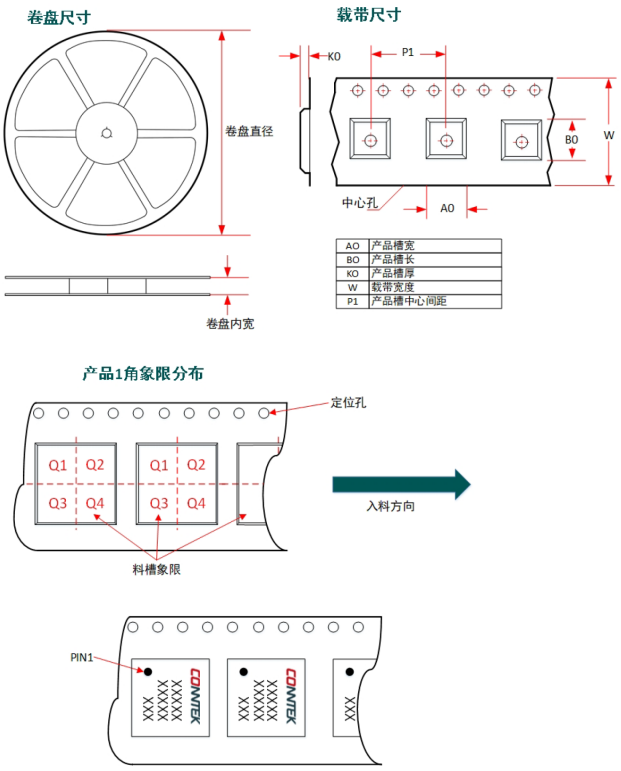

Figure 27: QFN-16L Tape and Reel Mechanical Drawing

16.2 Tape Dimensions

Table 19: Carrier Tape and Reel Parameters

Package Type	Pins	SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Direction
QFN3×3-16L	16	5000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1

—

17 Reflow Soldering Temperature Profile

The recommended reflow soldering profile is shown below. It follows a standard ramp-soak-peak process.

17.1 Profile Parameters

- Preheat stage: $150°C \pm 10°C$ for 90 ± 30 seconds
- Ramp-up slope: $2–5°C/s$

- Peak temperature: $255°C \pm 10°C$ for 10 ± 1 seconds
- Cooling rate: $2–5°C/s$

17.2 Temperature Curve

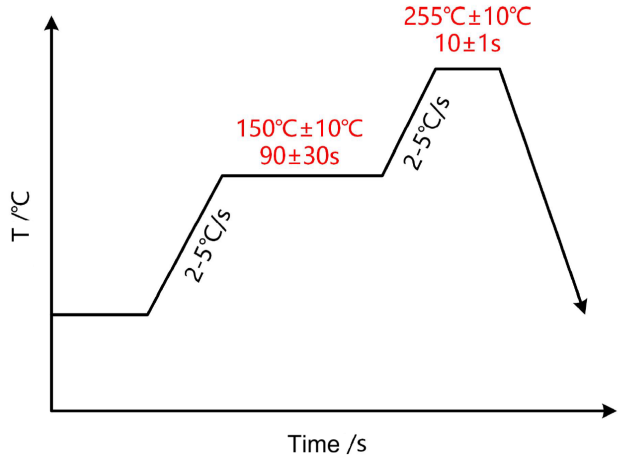

Figure 28: Reflow Soldering Temperature Curve