KTH7114 Series

16-bit High-Speed High-Precision Stray Field Immunity Magnetic Encoder Programmable Multi-Interface Angle Sensor with ABZ/UVW/PWM/SPI/SSI Outputs

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1 Product Information

1.1 Product Features

- 16-bit high precision absolute angle output.
- Supports both single pole-pair and multi pole-pair magnet applications.
- Ultra-low latency, with a data update time of $1\,\mu$s.
- SPI communication with data rate up to 10 Mbps.
- SSI communication with angle data output up to 5 Mbps.
- Programmable ABZ output from 4 to 16384 steps per revolution.
- Programmable UVW output from 1 to 32 pole pairs.
- PWM 12-bit angle output with adjustable frequency, and support for calibration status indication.
- Operating voltage from 3.3 V to 5 V.
- Operating temperature from $-40\,^{\circ}$C to $125\,^{\circ}$C.

1.2 Typical Applications

- Absolute angle position detection.
- Brushless DC motor control.
- Closed-loop stepper motor systems.
- Platform screen door control in rail transit systems.

1.3 Product Overview

KTH7114 is a high speed and high precision magnetic encoder with an advanced Automatic Non-Linearity Calibration function, abbreviated as ANLC. Users can trigger the calibration process either by writing to registers or by using an external calibration pin. The chip can then automatically measure the sensor non-linearity error, calculate the compensation parameters, and store the calibration result into the internal MTP memory. This function requires no complicated external intervention and can significantly improve the linearity of angle measurement.

KTH7114 provides multiple flexible communication interfaces and output modes to meet the needs of different application scenarios.

- **SPI interface:** Supports 3-wire SPI communication with CPOL $= 1$ and CPHA $= 1$. It is used to read 16-bit angle data, access internal registers, and configure parameters. An 8-bit CRC check is provided during angle and register read operations. This 3-wire SPI interface does not support parallel CS selection. To save MCU IO resources, multiple SDA lines may be connected to the MCU for data reading.
- **ABZ incremental output:** Provides programmable quadrature ABZ output with resolution up to 16384 steps per revolution. Absolute position start-up is supported, so the chip can output a burst of AB pulses after power-on to indicate the absolute position.

- **SSI synchronous serial interface:** Supports 2-wire SSI communication for absolute angle output, with maximum rate up to 5 Mbps.
- **PWM output:** Provides programmable PWM output from 120 Hz to 3.8 kHz, and the PWM signal can also indicate the chip calibration status.
- **UVW commutation output:** Supports programmable UVW commutation output from 1 to 32 pole pairs.

The interfaces and output modes listed above provide flexible data interaction methods and convenient system integration options for the user.

2 General Description

2.1 System Architecture

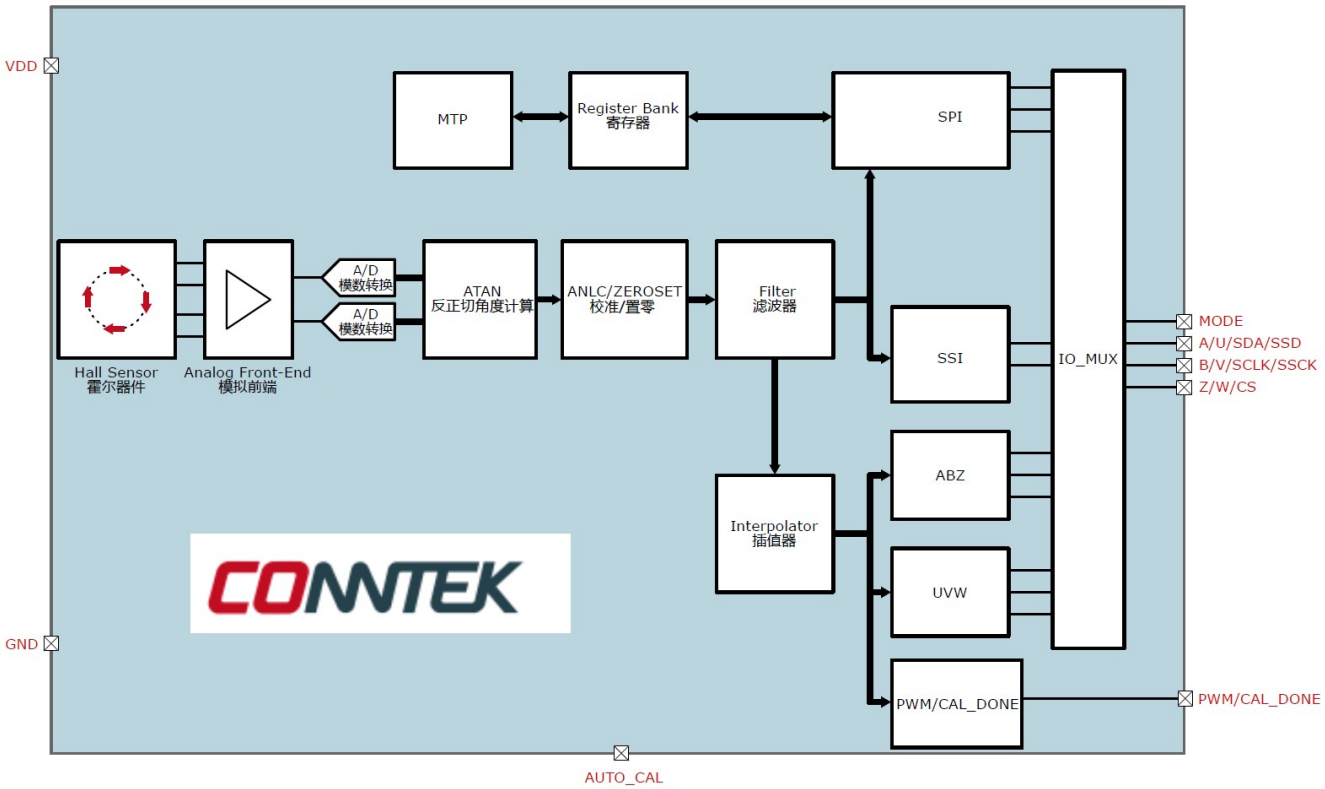

Figure 1: System block diagram

KTH7114 is a Hall angle encoder. It integrates Hall sensing elements, analog-to-digital conversion modules, and various processing blocks for accurate angle measurement and digital signal output.

The Hall elements generate voltage signals, which are converted by the ADC into two orthogonal digital signals. These signals are then processed by the ATAN module to obtain a 16-bit digital angle. After that, the digital angle passes through zero setting, rotation direction setting, and filtering.

The filtered angle can be directly output through SPI and SSI interfaces, so that users can read it with an MCU or other circuits. In addition, the angle can also be expressed through PWM modulation, where the duty cycle represents the angle value. To improve refresh rate, the filtered angle can be further processed by the interpolator and then sent to the ABZ encoder block, where it is converted into the required encoded signals.

Various system operating parameters are stored in the programmable MTP memory and can be modified through SPI commands to meet different application requirements.

2.2 Recommended Application Circuit

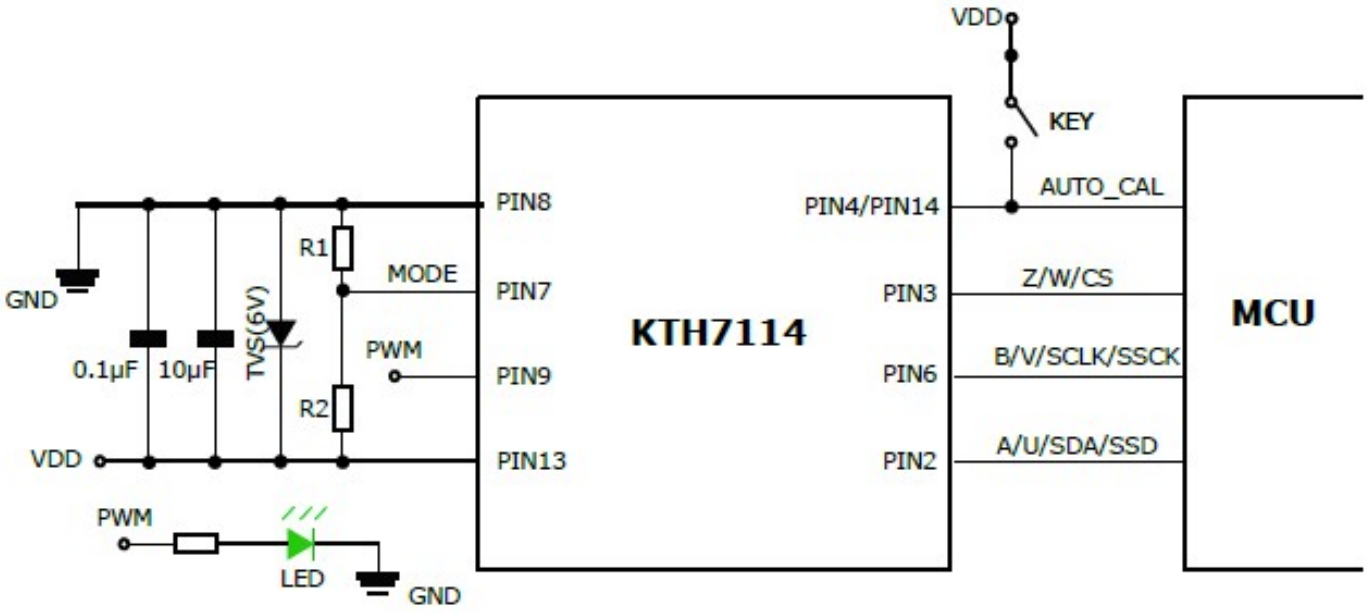

Figure 2: Recommended application circuit

Notes:

- $R1$ and $R2$ are $5.1\,\mathrm{k}\Omega$ selection resistors. If $R2$ is populated and $R1$ is not populated, MODE is pulled high and the device is configured for 3-wire SPI output. If $R1$ is populated and $R2$ is not populated, MODE is pulled low and the device can be configured for ABZ, UVW, or SSI output.
- During PCB design, if only one interface such as SPI or ABZ is used, $R1$ and $R2$ may be omitted and MODE may be directly connected to VDD or GND.
- During PCB design, if the SPI interface is used, resistor $R3$ may be omitted. If other interfaces are used, $R3$ must be retained, and the recommended value is $10\,\mathrm{k}\Omega$.
- AUTO_CAL may be triggered by an external push button, or driven high by the MCU. If this function is not used, the pin may be left floating.

- PWM can output the calibration-done indication, so it may be connected to an LED as a visual indicator.
- Pin 4 and pin 14 are both AUTO_CAL pins. Only one of them needs to be routed out for use. If unused, the pin may be left floating.

2.3 Pin Definition

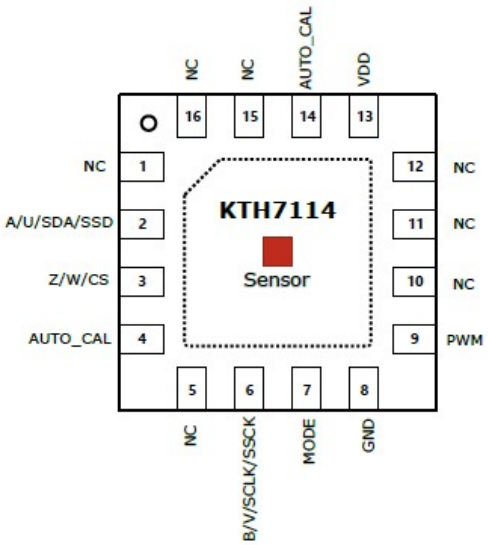

Figure 3: QFN-16L 3 mm × 3 mm package, with the sensor located at the geometric center

Table 1: Pin functions

Pin No.	Name	Function
1	NC	Not connected. The IO must be left floating.
2	A/U/SDA/SSD	Controlled by the MODE pin and the IO_MUX register.
3	Z/W/CS	Controlled by the MODE pin and the IO_MUX register.
4	AUTO_CAL	External calibration trigger input, active high.
5	NC	Not connected. The IO must be left floating.
6	B/V/SCLK/SSCK	Controlled by the MODE pin and the IO_MUX register.
7	MODE	Interface output control.
8	GND	Ground.
9	PWM	Duty-cycle output.
10	NC	Not connected.
11/12	NC	Not connected. The IO must be left floating.
13	VDD	Power supply.
14	AUTO_CAL	External calibration trigger input, active high.
15/16	NC	Not connected. The IO must be left floating.
17	T-PAD	Thermal pad. Connect it to GND.

2.4 16-Bit Binary Angle Coding

The angle value of KTH7114 is represented by a 16-bit binary code. By converting the angle into a 16-bit binary value, precise angle representation can be achieved. For example, the angle can be expressed as an integer in the range from 0 to 65535. Unless otherwise stated, all angles in this datasheet are represented in 16-bit binary form.

The relationship between the angle output from $0°$ to $360°$ and the 16-bit binary value is given by

$$\text{Angle}\,(0° \text{ to } 360°) = \frac{\text{16-bit binary value}}{2^{16}} \times 360° \tag{1}$$

3 Key Parameters

Table 2: Key specifications at 3.3 V supply

Parameter	Min	Typ	Max
Operating voltage	3.0 V	3.3 V	5 V
Magnetic field strength	30 mT	60 mT	150 mT
Operating current		16 mA	
Start-up time		20 ms	
Latency time		$1\,\mu$s	
Output noise ($1\,\sigma$)		$0.015°$	
Non-linearity error		$\pm 0.1°$	
Rotational speed			120000 rpm
ESD (HBM)		± 5 kV	

4 Magnet Installation Guide

4.1 On-Shaft Magnet Installation Recommendation

Table 3: On-shaft magnet installation recommendation

Para.	Description	Min	Typ	Max	Unit
D_{mag}	Magnet diameter (radial magnetization)		10	30	mm
T_{mag}	Recommended magnet thickness		2.5	5	mm
B_{pk}	Magnetic field at chip	30		150	mT
AG	Air gap		1.0	5.0	mm
RS	Rotational speed			120	krpm
D_{ISP}	Installation offset	0		1.0	mm
TC_{mag1}	NdFeB temperature coefficient		−0.120		%/°C
TC_{mag2}	SmCo temperature coefficient		−0.035		%/°C

Recommended magnet materials are NdFeB or SmCo.

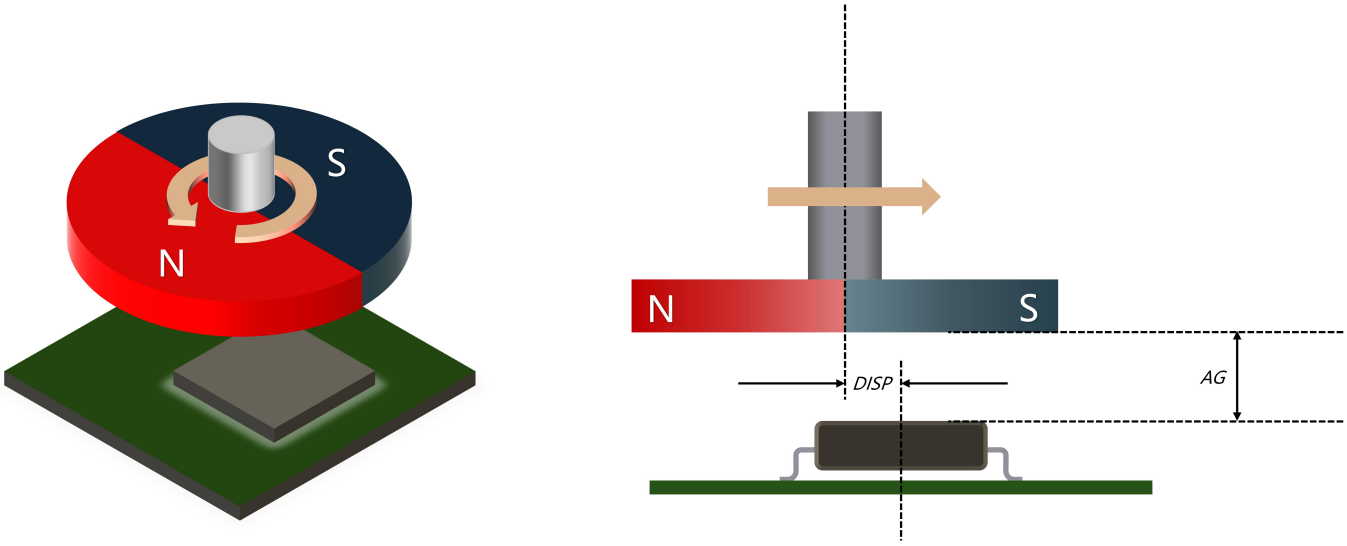

Figure 4: Recommended magnet placement

5 Register Configuration

5.1 Register Map

Address	Register								Default
	7	6	5	4	3	2	1	0	
0x00	ZERO[7:0]								0x00
0x01	ZERO[15:8]								0x00
0x02	RD	AUTO_ZERO_SET	Z_PHASE[1:0]		Z_EDGE	Z_WID[2:0]			0x00
0x03	PPT[7:0]								0xFF
0x04	RESERVE				PPT[11:8]				0x03
0x05	ABZ_START_T[3:0]				ABZ_START_MODE	ABZLIMIT_F[2:0]			0x00
0x06	RAM_HYS[7:0]								0x07
0x07	RESERVE	RAM_HYS[14:8]							0x00
0x08	RESERVE			NPP[4:0]					0x00
0x09	PWM_F[7:0]								/
0x0A	PWM_F[15:8]								/
0x0D	FW[7:0]								0x88
0x10	RESERVE					IO_MUX			0x00
0x16	RESERVE			REG_CAL	ANLC_EN	RESERVE			0x08
0x72	RESERVE		ANLC_STATUS[1:0]		RESERVE				0x00

Figure 5: Register map

5.2 Parameter Description

Table 4: Parameter description

Symbol	Default	Description
ZERO[15:0]	0	Zero position setting; default is 0.
RD	0	Forward/reverse rotation setting; default forward is 0.
AUTO_ZERO_SET	0	Auto-zero setting; if set to 1, the chip output angle is 0.
Z_PHASE[1:0]	0	ABZ Z-signal phase; default is 0.
Z_EDGE	0	Z-signal rising edge is aligned with absolute zero by default; otherwise the falling edge is aligned.
Z_WID[2:0]	0	Z-signal output width; default is 1 LSB.
PPT[11:0]	1023	ABZ resolution; default 1024 lines, 4096 steps/rev.
ABZ_START_T[3:0]	2	ABZ output delay; default starts output 20 ms after power-on.
ABZ_START_MODE	0	Set to 1 for ABZ absolute output mode; default is incremental output.
ABZLIMIT_F[2:0]	0	ABZ output bandwidth; default maximum frequency 16 MHz.
RAM_HYS[14:0]	7	Angle output hysteresis.
NPP[4:0]	0	UVW pole-pair output; default outputs 1 pole pair.
PWM_F	x	PWM output frequency adjustment; factory trimmed to 1 kHz (typ.).
FW[7:0]	136	Filter depth; default is 0x88 (136 decimal).
IO_MUX	0	Default ABZ output when MODE is pulled high.
REG_CAL	0	Self-calibration enable; set to 1 to start self-calibration.
ANLC_EN	1	Non-linearity calibration effect enabled for angle output.
ANLC_STATUS[1:0]	0	Self-calibration status; 0 means calibration not started.
RESERVE	0	Reserved by the manufacturer; not user-defined; default is 0.

6 SPI Interface

KTH7114 uses a 3-wire SPI interface and operates in Mode 3 with CPOL $=$ 1 and CPHA $=$ 1. The interface supports angle reading, register read and write, and MTP programming. The maximum SPI communication rate is 10 Mbps.

6.1 SPI Timing

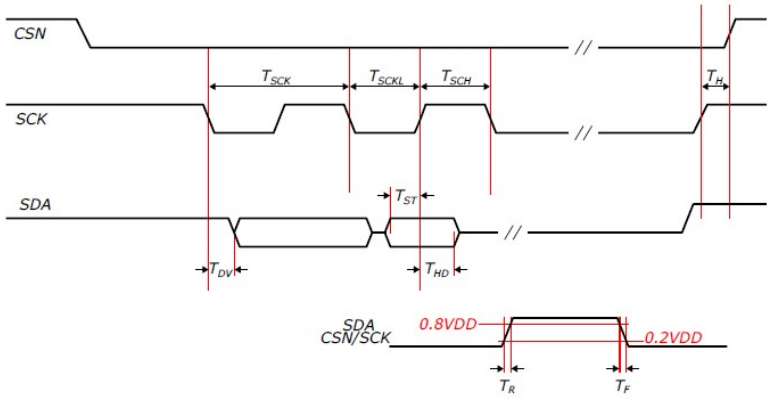

Figure 6: SPI timing diagram

Table 5: SPI timing parameters (load 20 pF)

Symbol	Description	Min	Typ	Max
T_{SCK}	SCK clock period (ns)	100		
T_{SCKL}	SCK low-level period (ns)	50		
T_{SCKH}	SCK high-level period (ns)	50		
T_H	Interval from SCK rising edge to CSN rising edge (ns)	120		
T_R	Digital signal rise time (ns)		10	
T_F	Digital signal fall time (ns)		10	
T_{DV}	MISO data valid time (ns)			50
T_{ST}	MOSI data setup time (ns)	50		
T_{HD}	MOSI data hold time (ns)	50		

Note: To ensure reliable data communication, hardware and firmware designs should comply with these timing parameters.

On the 3-wire interface the timing diagram shows a single data line (SDA). The parameters T_{DV}, T_{ST}, and T_{HD} use MISO/MOSI naming as in the table, corresponding to data driven by the device and setup/hold for data driven by the host, respectively.

6.2 Reading Absolute Angle Through SPI

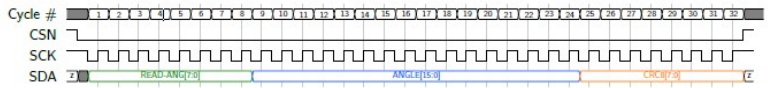

Figure 7: SPI standard angle read timing

The procedure for reading the absolute angle through SPI is as follows.

1. Send command: 8-bit `0x00`.

2. Receive data: 16-bit angle + 8-bit CRC.
3. The number of SCLK pulses can be adjusted as required; for example, issuing only eight SCLK pulses to read the upper eight bits of the angle is supported.
4. The interval between two SPI transactions must be greater than 150 ns.

CRC follows the CRC8/ITU standard.

- Polynomial: $x^8 + x^2 + x + 1$ ($0\text{x}07$).
- Initial value: $0\text{x}00$.
- Result XOR value: $0\text{x}55$.

6.3 Register Access Control (Unlock and Lock)

A register access control mechanism (unlock and lock) is implemented.

The device is locked by default after power-on; registers cannot be written.

Writing the unlock password $32'h20240101$ enables register write access.

Writing the lock password $32'h20241231$ locks the registers again.

In the locked state, angle and register values can still be read; register writes are not allowed.

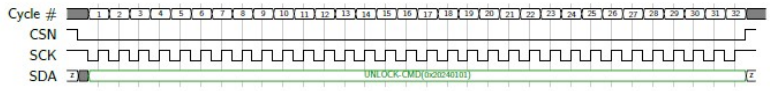

Figure 8: SPI unlock timing diagram

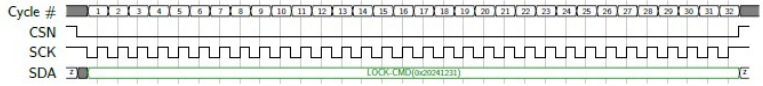

Figure 9: SPI lock timing diagram

During normal operation, once register configuration is completed, the device can be set to allow only angle reading through SPI, while disabling register write operations. This prevents unintended interference from affecting register settings and improves system reliability.

6.4 Reading Registers Through SPI

The procedure for reading registers is as follows.

1. Send command: 8-bit $0\text{x}11$ + 8-bit register address.
2. Receive data: 8-bit register value + 8-bit CRC.
3. The upper 16 bits are the read command issued to the device; the lower 16 bits are the returned register value and CRC.

4. The interval between two SPI transactions must be greater than 150 ns.

Figure 10: SPI register read timing diagram

6.5 Writing Registers Through SPI

The procedure for writing registers is as follows.

1. First send the unlock password $32'h20240101$.
2. Send command: 8-bit $0x33$ + 8-bit register address + 8-bit write data.
3. Receive data: 8-bit register value. The device returns the written register value in the same frame.

The high-level duration of the 24th SCLK cycle must be greater than 100 ns.

Important timing requirements are as follows.

- The interval between two SPI transactions must be greater than 150 ns.
- After a register write, wait at least 100 ns before sampling the returned value.

Figure 11: SPI register write timing diagram

6.6 Writing Register Values Into MTP Through SPI

The register writes described above are volatile and are not retained after power-off. The values written to registers must therefore be programmed into MTP (non-volatile memory). The MTP programming procedure is as follows.

1. First ensure that the registers are unlocked by sending the unlock password $32'h20240101$.
2. Send the 24-bit MTP programming command $0x2255AA$.
3. The entire transfer consists of command bits only; there is no return data.

Important notes are as follows.

- The interval between two MTP programming operations must be greater than 400 ms.

- MTP programming is irreversible, so the parameters must be carefully verified before programming.
- It is recommended to perform MTP programming under a professional testing environment.
- Do not power off during programming, otherwise data loss or damage may occur.

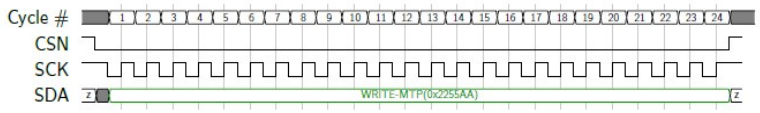

Figure 12: SPI MTP programming timing diagram

7 SSI Interface

SSI (Synchronous Serial Interface) is a synchronous serial interface protocol. KTH7114 supports reading angle data through SSI.

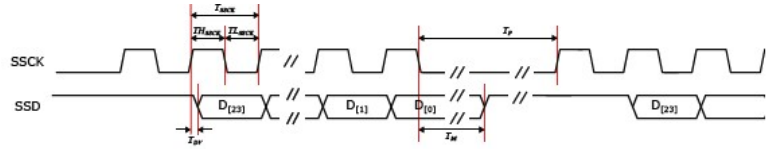

Figure 13: SSI timing diagram

Table 6: SSI timing parameters

Symbol	Description	Min	Max	Unit
t_{DV}	SSD data valid delay		15	ns
T_{SSCK}	SSCK clock period	0.2	10	μs
T_{LSSCK}	SSCK low-level period	0.1	5	μs
T_{HSSCK}	SSCK high-level period	0.1	5	μs
T_M	Transfer timeout (monostable)	10		μs
T_p	Pause time (dead time)	16		μs

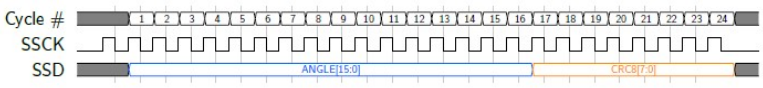

Figure 14: SSI standard angle read timing

KTH7114 operates as an SSI slave. It supports angle reads only and does not support register read or write. Data is output MSB first.

8 ABZ Output

Address	Register								Default
	7	6	5	4	3	2	1	0	
0x03	PPT[7:0]								0xFF
0x04	RESERVE				PPT[11:8]				0x03
0x05	ABZ_START_T[3:0]				ABZ_START_MODE	ABZLIMIT_F[2:0]			0x00

Figure 15: ABZ related registers

KTH7114 provides incremental ABZ outputs for angular position. The default resolution is 14 bit, corresponding to 16384 steps per revolution or 4096 pulse periods per revolution (PPT).

The phase relationship between A and B indicates rotation direction: when rotating clockwise (CW), A leads B; when rotating counterclockwise (CCW), B leads A. During power-up, A, B, and Z all remain at a high level.

For CCW rotation, the rising edge of B leads the rising edge of A by one quarter of a period. For CW rotation, the rising edge of A leads the rising edge of B by one quarter of a period.

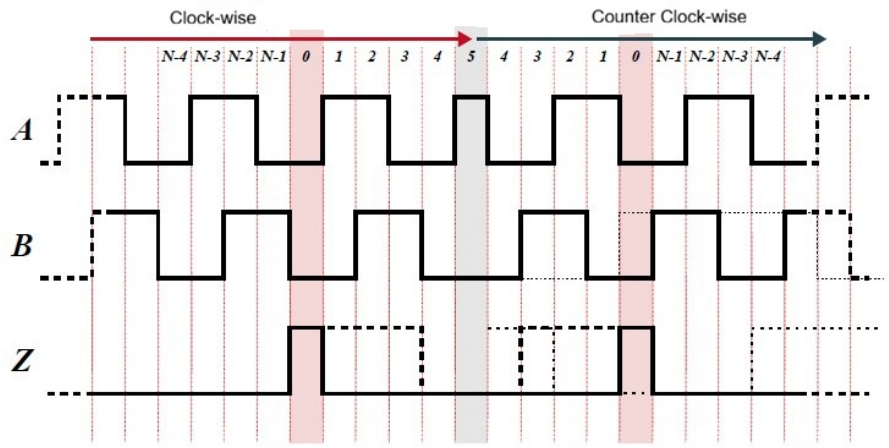

Figure 16: ABZ output timing

8.1 ABZ Output Resolution

The ABZ incremental output can be set to any integer pulse-period resolution up to 4096 pulses per revolution. The resolution is programmed through the PPT[11:0] field in MTP; see Table 7.

Table 7: ABZ resolution versus PPT[11:0]

PPT[11:0]	ABZ pulses/rev	ABZ steps/rev
0	1	4
1	2	8
2	3	12
	...	
4093	4094	16376
4094	4095	16380
4095	4096	16384

8.2 ABZ Output Frequency

The ABZ output frequency is at most 16 MHz (AB edge frequency). The maximum output rate can be reduced by programming ABZLIMIT; see Table 8.

Table 8: Maximum ABZ output frequency versus ABZLIMIT

ABZLIMIT	Maximum frequency
0	16 MHz
1	8 MHz
2	4 MHz
3	2 MHz
4	1 MHz

8.3 ABZ Start Mode

KTH7114 provides two ABZ start modes, controlled by the ABZ_START_MODE register.

- Normal start (ABZ_START_MODE = 0): after start-up, ABZ outputs incremental pulses directly.
- Absolute position start (ABZ_START_MODE = 1): at start-up, ABZ outputs a burst of pulses that represent the current absolute position.

When absolute position start is enabled, after ABZ_EN is asserted the device waits one cycle of the internal 16 MHz clock, latches the current angle as the absolute position, and then drives a pulse burst on AB corresponding to that position.

The number of pulses is

$$N = \frac{\min(\mathrm{ABS}, 65536 - \mathrm{ABS})}{65536} \times \mathrm{PPT} \tag{2}$$

where ABS is the absolute position in 16-bit binary form and PPT is the configured pulses per revolution.

For example, using Equation (2), at absolute position $90°$ (binary value 16384) with PPT $= 511$, AB outputs 128 pulses. If the absolute position is greater than $180°$, the AB direction is reversed and the burst counts down from $360°$ toward the current position.

8.4 ABZ Start Delay

The ABZ output start delay is set with ABZ_START_T[3:0]; see Table 9.

Table 9: ABZ start delay settings

ABZ_START_T[3:0]	Start delay
1	10 ms
2	20 ms (default)
3	30 ms
4	40 ms
5	50 ms
6	75 ms
7	100 ms

This parameter reduces the effect of unstable conditions during the initial power-on interval on ABZ output accuracy.

9 UVW Output

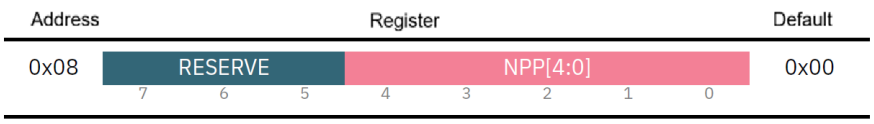

Figure 17: UVW related registers

The UVW output simulates three Hall switch signals for three-phase motor commutation. As shown in Figure 18, the duty cycle of each logic signal is 50%, and the phase shift between adjacent signals is $120°$.

If the number of motor pole pairs is greater than that of the target magnet, KTH7114 can generate multiple UVW periods by dividing the digital angle into the required commutation steps within each $360°$ revolution. The parameter NPP[4:0] configures the simulated pole-pair number and therefore determines the commutation step angle of the UVW output. The corresponding relationship is listed in Table 10.

Table 10: UVW pole-pair configuration through NPP[4:0]

NPP[4:0]	Pole Pairs	States per Revolution
00000	1	6
00001	2	12
00010	3	18
00011	4	24
00100	5	30
00101	6	36
00110	7	42
00111	8	48
...	...	...
11110	31	186
11111	32	192

For example, for a four-pole motor, that is, a motor with 2 pole pairs, the spacing of the UVW commutation signals is 30°, as illustrated in Figure 19.

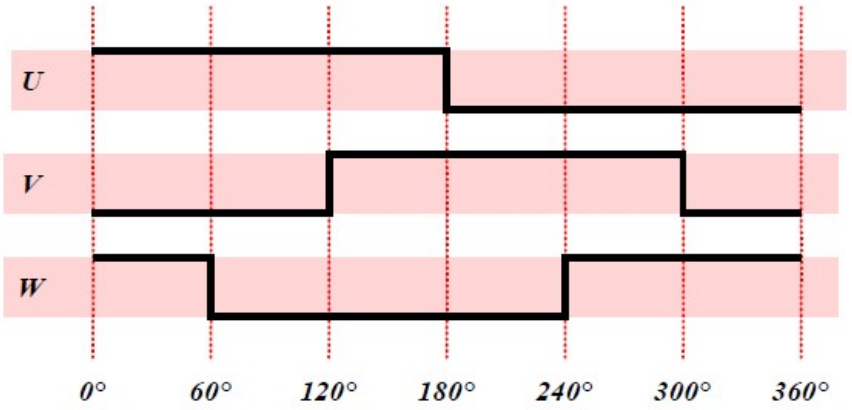

Figure 18: UVW output for a one-pole-pair rotor

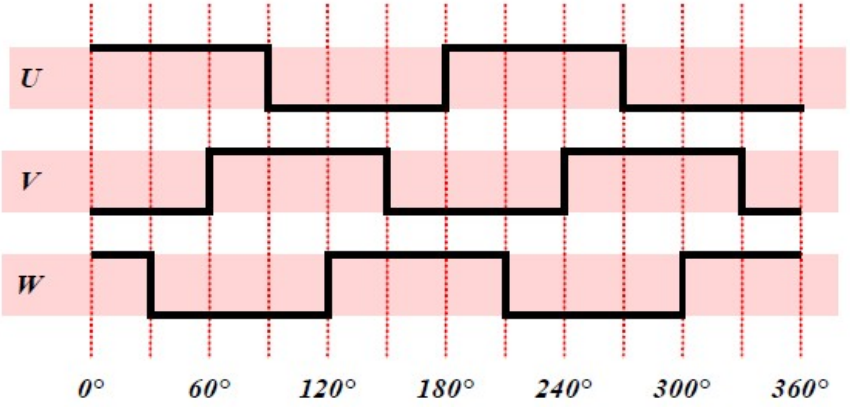

Figure 19: UVW output for a four-pole, two-pole-pair rotor

9.1 UVW Start-Up Delay

The start-up delay of the UVW output is the same as that of the ABZ output, and it is controlled by the ABZ_START_T[3:0] parameter. This ensures that, during the initial stage after power-on, the UVW signal starts only after the system has become stable, which improves overall system reliability.

9.2 Phase Relationship Between UVW and Z Signal

In KTH7114, the edges of the UVW signals are aligned with the Z signal. This ensures accurate synchronization between motor commutation and the zero position, which is especially important in applications that require precise position control.

10 PWM Absolute Position Output

Address	Register	Default
0x09	PWM_F[7:0] (7 6 5 4 3 2 1 0)	/
0x0A	PWM_F[15:8] (7 6 5 4 3 2 1 0)	/

Figure 20: PWM related registers

KTH7114 provides a single-wire PWM absolute position output mode, as shown in Figure 21. PWM is the default output on pin 9.

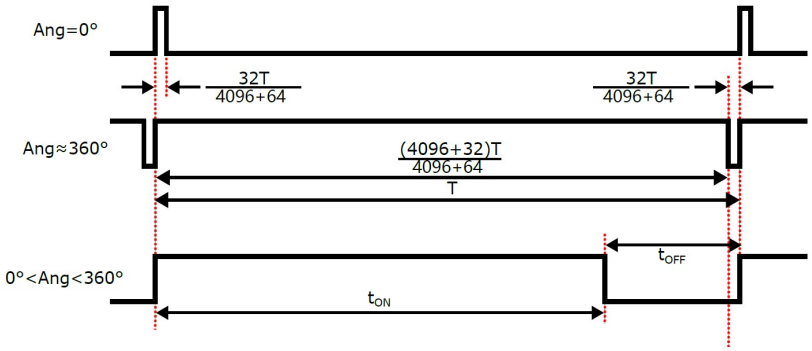

Figure 21: PWM timing

10.1 PWM Output Frequency

The PWM output frequency is adjustable and controlled by the `pwm_f` parameter (register field PWM_F). The output frequency is calculated as

$$\text{PWM(Hz)} = \frac{(120.284 - 3846.0)}{65536.0} \times PWM\_F + 3846.0 \qquad (3)$$

- When $PWM\_F = 0$, the output frequency is 3.846 kHz.
- When $PWM\_F = 65535$, the output frequency is 120.284 Hz.

These boundary values follow from Equation (3).

10.2 PWM Resolution and Angle Calculation

For the PWM output, the duty cycle is proportional to the magnetic field angle, with 12-bit resolution. When the duty cycle is $\frac{32}{4096+64}$, the corresponding angle is $0°$. When the duty cycle is $\frac{4096+32}{4096+64}$, the corresponding angle is $360°$. For an arbitrary angle,

$$Ang = \frac{360}{4096}\left((4096+64)\cdot\frac{t_{\text{ON}}}{t_{\text{ON}}+t_{\text{OFF}}}-32\right) \tag{4}$$

where t_{ON} and t_{OFF} are the high-level and low-level times of the PWM period, respectively.

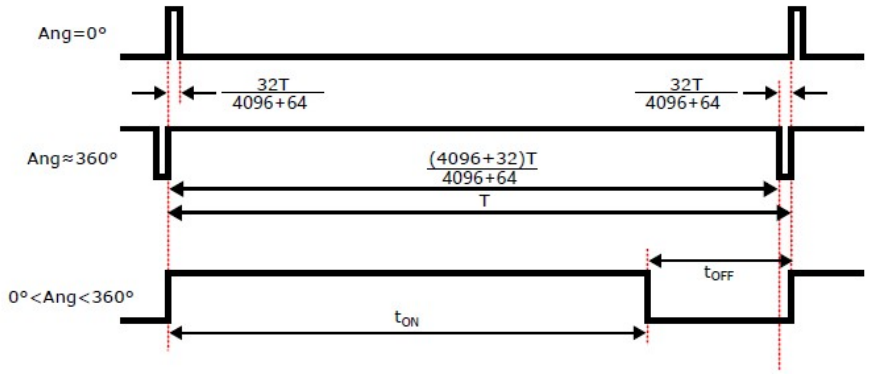

Figure 22: PWM timing at $0°$, near $360°$, and intermediate angle

10.3 PWM Indication During Non-Linearity Calibration

During non-linearity calibration, PWM indicates status as follows.

- Output frequency 3.8 Hz and 50% duty cycle: calibration in progress.
- Constant high level: calibration completed successfully.
- Constant low level: calibration failed.

When the `AUTO_CAL` signal is pulled low, PWM returns to normal angle output.

10.4 PWM Start-Up Delay

As with ABZ and UVW, PWM start-up delay is controlled by ABZ_START_T[3:0]. This lets the system stabilize after power-on before PWM angle output starts, so initial transients do not degrade output accuracy.

11 Automatic Non-Linearity Calibration

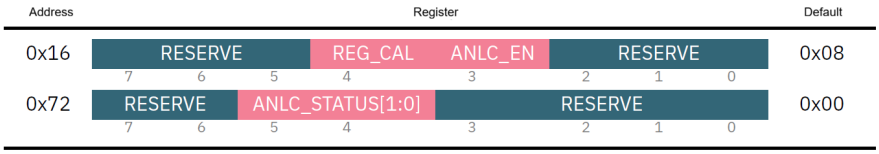

Figure 23: Non-linearity calibration related registers

KTH7114 integrates an advanced Automatic Non-Linearity Calibration function, which compensates the non-linearity error of the sensor under real operating conditions and improves angle measurement accuracy.

11.1 Calibration Principle

The calibration module samples angle error at 16 equally spaced points within one full rotation and calculates compensation parameters based on these samples. During calibration, the PWM output toggles at approximately 3.8 Hz with a duty cycle of 50%, indicating that the calibration process is in progress. After calibration is completed, the PWM signal returns to normal operation.

11.2 Calibration Status

The calibration status is indicated by the ANLC_STATUS[1:0] register, as shown in Table 11.

Table 11: Non-linearity calibration status

ANLC_STATUS[1:0]	Description
0	Calibration not started
1	Calibration in progress
2	Calibration failed
3	Calibration completed

11.3 Calibration Method

KTH7114 provides a register-triggered calibration method.

By setting the REG_CAL register to 1, the device starts the non-linearity calibration process. After calibration is completed, REG_CAL must be cleared to 0 to finalize the calibration procedure.

11.4 Calibration Recommendations

To achieve optimal calibration results, the following conditions are recommended.

The magnetic field strength should remain stable during calibration, and the relative position between the magnet and the sensor should not change.

The rotation speed should be kept constant, typically within the range of 100 to 1000 rpm. Excessively high or low speed may degrade calibration accuracy.

Calibration should be performed under actual application conditions, so that the compensation reflects real operating environments.

For off-axis applications, it is recommended to first adjust the GAINTRIM parameter and then perform non-linearity calibration.

After calibration is completed, the calibration parameters are automatically stored in MTP memory and will not be lost after power-off.

12 System Operating Settings

Address	Register								Default
0x00	ZERO[7:0]								0x00
	7	6	5	4	3	2	1	0	
0x01	ZERO[15:8]								0x00
	7	6	5	4	3	2	1	0	
0x02	RD	AUTO_ZERO_SET	Z_PHASE[1:0]		Z_EDGE	Z_WID[2:0]			0x00
	7	6	5	4	3	2	1	0	
0x06	RAM_HYS[7:0]								0x07
	7	6	5	4	3	2	1	0	
0x07	RESERVE	RAM_HYS[14:8]							0x00
	7	6	5	4	3	2	1	0	
0x0D	FW[7:0]								0x88
	7	6	5	4	3	2	1	0	

Figure 24: System configuration related registers

12.1 Rotation Direction

The RD register defines the relationship between rotation direction and angle increment.

By default, when RD is set to 1, the output angle increases when the magnet rotates clockwise (viewed from the top of the chip).

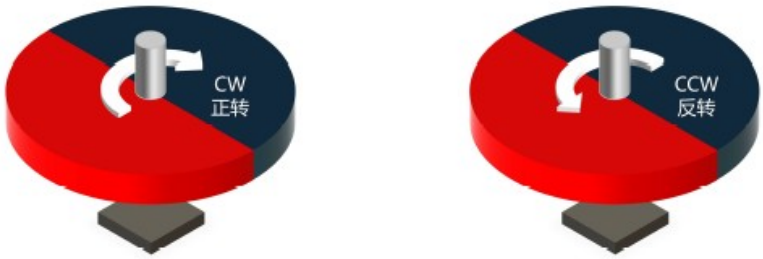

Figure 25: The definition of CW and CCW

12.2 Zero Position Setting

Zero position setting is used to align the sensor output angle with the mechanical zero position. The system provides two zero-setting methods: automatic zero setting and manual zero setting.

12.2.1 Automatic Zero Setting

Automatic zero setting supports two trigger methods: register trigger and level trigger.

For register trigger, when the AUTO_ZERO_SET register is set to 1, the device automatically performs the following operations.

First, it calculates the zero offset according to

$$zero\_set\_angle = RD?(ZERO - ango) : (ZERO + ango) \tag{5}$$

Then the calculated zero_set_angle is written into the ZERO[15:0] register.

After that, the new zero value is automatically programmed into MTP memory.

Finally, the AUTO_ZERO_SET register is cleared automatically after the operation is completed.

12.2.2 Manual Zero Setting

Manual zero setting is implemented by directly writing to the ZERO[15:0] register.

The register range is from 0 to 65535, corresponding to $0°$ to $360°$.

The written value takes effect immediately and affects the angle value of all output interfaces.

The manually written value is not retained after power-off, so it must be saved by an MTP programming command if non-volatile storage is required.

The influence of zero setting on the angle output is given below.

- When $RD = 0$, the output angle is equal to the raw angle minus ZERO.
- When $RD = 1$, the output angle is equal to the raw angle plus ZERO minus 65536.

Table 12: Comparison of zero-setting methods

Method	Advantage	Disadvantage
Register automatic setting	Easy to use, automatically saved	Requires SPI communication
Level automatic setting	No communication interface required, convenient operation	Requires an extra control pin
Manual setting	Precise control, high flexibility	Must be saved manually, operation is more complex

The ZERO[15:0] register defines the zero position, and this value applies to all angle output types. The sensor zero position can be programmed with full 16-bit resolution.

When $RD = 1$, the ZERO value can be calculated from the current SPI binary output and the desired target angle according to

$$ZERO = \sim \left(\text{16-bit binary value} - \left(\frac{\text{Target Angle}}{360}\right) \times 2^{16}\right) + 1 \quad (6)$$

When $RD = 0$, the ZERO value can be calculated according to

$$ZERO = \text{16-bit binary value} - \left(\frac{\text{Target Angle}}{360}\right) \times 2^{16} \quad (7)$$

For example, using Equation (6), when $RD = 1$ and the 16-bit binary value is 16384, the SPI output angle is $90°$. If ZERO[15:0] is set to the two's complement of 16384, that is, 49152, the output becomes 0, corresponding to an output angle of $0°$.

Using Equation (7), when $RD = 0$ and the 16-bit binary value is 16384, the SPI output angle is also $90°$. If ZERO[15:0] is set to 16384, the output becomes 0, corresponding to an output angle of $0°$.

12.3 Hysteresis

Hysteresis is introduced to prevent false switching and improve noise immunity. In practice, this means that the output does not change state immediately when the input changes, but only after the input exceeds a defined threshold. This mechanism reduces the influence of noise and interference, thereby improving system stability and precision.

The hysteresis function is effective for all output interfaces.

The hysteresis parameter is configured by RAM_HYS[14:0], where 1 LSB corresponds to

$$\frac{1}{32768} \times 360° \quad (8)$$

The default value is 7, which corresponds to approximately $0.07693°$ by Equation (9).

By introducing output hysteresis, the system can reduce error caused by small disturbances and improve immunity to interference. This is especially important in applications that require both high precision and stable operation.

Table 13: Hysteresis parameter configuration

RAM_HYS[14:0]	Hysteresis Angle	Description
0	0°	No hysteresis
1	0.01099°	Minimum hysteresis value
2	0.02197°	
4	0.04395°	
7	0.07693°	Default value
8	0.08789°	
16	0.17578°	
32	0.35156°	
64	0.70313°	
128	1.40625°	Maximum hysteresis value

The hysteresis angle is calculated as

$$\text{Hysteresis Angle} = \frac{RAM\_HYS \times 360}{32768} \tag{9}$$

12.4 Filter

The filter depth affects both the effective resolution and the output bandwidth of the system.

The effective resolution is defined as the $\pm 3\sigma$ noise range, which mainly influences speed fluctuation. The output bandwidth determines the dynamic response of the system. Therefore, increasing the filter depth improves noise performance but reduces response speed.

Table 14 shows the relationship between filter depth and effective resolution. The default value of the FW[7:0] register is `0x88`.

Table 14: Effective resolution versus filter depth

FW[7:0]	Filter Level	Effective Resolution (bit)
0x00	0	9.5
0x11	1	10
0x33	3	11
0x77	7	12
0x88	8	13
0xAA	10	14
0xFF	15	15

From the table, it can be seen that a higher filter level results in higher effective resolution. However, this also reduces the bandwidth of the output signal.

Therefore, the selection of filter depth should be based on application requirements. For applications requiring high precision and low noise, a higher filter level is recommended. For applications requiring fast dynamic response, a lower filter level should be selected.

13 Selection Guide

Table 15: Model selection guide

Model	Noise (1σ)	Output Interface	Time Constant τ	Magnetic Field / Application
KTH7114	$0.015°$	SPI, SSI, PWM, ABZ	0.51 ms	30–150 mT / Industrial automation

This table provides a quick reference for selecting the appropriate device according to noise performance, interface type, and application requirements.

14 Ordering Information

Table 16: Ordering information

Model	Package	Operating Temperature	Application	Pins	CRC Support
KTH7114-QN16	QFN 3 mm × 3 mm-16L	−40°C to 125°C	Industrial automation	16	Yes

The ordering information specifies the package type, operating temperature range, and functional options of the device.

15 Reflow Soldering Profile

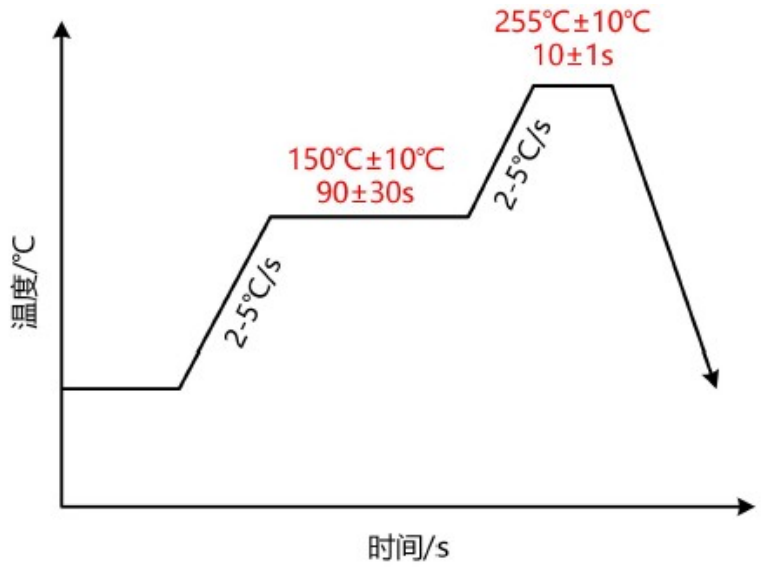

Figure 26: Reflow soldering temperature profile

The reflow soldering profile shown above defines the recommended temperature curve during the soldering process. Following this profile ensures proper solder joint formation and prevents damage to the device caused by excessive thermal stress.