KTM5900

24bit TMR Magnetic Encoder
Supports 1-4096 Pole Pairs
Nonlinear Self-calibration
Dual 16-bit 2MHz SAR ADC

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Table of Contents

Revision History

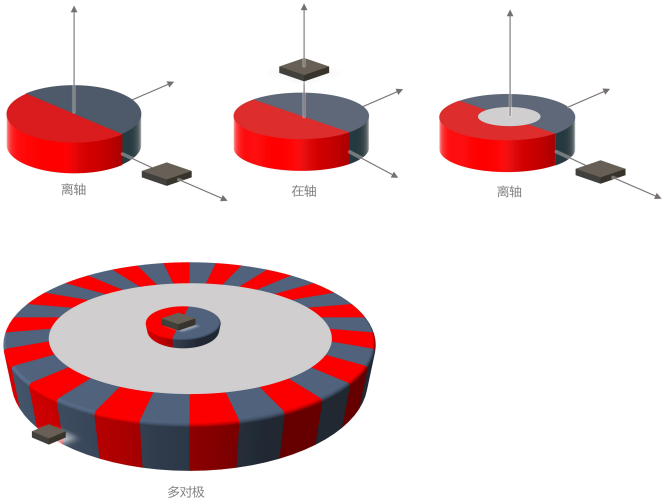
Version	Date	Description
Rev. 1.0	2026.1.25	Initial release.
		Updated package description from QFN32 to HFBP5x5-32L throughout the document.
		Updated Figure 2 caption from ”QFN32-5x5 Top View” to ”HFBP5x5-32L Top View”.
		Enhanced product features to include off-axis applications support and both on-axis and off-axis mounting capabilities.
		Added ”Off-axis angle measurement” and ”Coreless motors” to typical applications list.
		Updated product introduction to emphasize internally integrated high-precision TMR magnetic sensor.
		Updated system architecture description to include TMR sensor module, adjustable gain amplifier, and other functional modules.
		Updated ZREF pin description to ”Reference Z Signal Selection”.
		Updated application circuit description to emphasize internally integrated TMR sensor.
		Updated operating parameters: magnetic field strength range changed from 10-150mT to 30-80mT.
		Reorganized magnet parameters into ”On-Axis Magnet Mounting Recommendations” and ”Off-Axis Magnetic Ring Mounting Recommendations” sections.
		Updated magnet parameter tables with revised values and added important alignment notes for both on-axis and off-axis mounting.
		Added ”Internally Integrated TMR Parameters” section with TMR signal output schematic and parameter table.
		Updated table captions to remove ”with External AMR Sensor” references.
		Added complete CRC8 reference code with step-by-step calculation example and CRC_TABLE lookup array (256 entries).
		Clarified SPI Response 4 structure with explicit bit example (10-bit revolution + 16-bit angle + 2-bit state + 8-bit CRC = 36 bits total).
		Explicitly stated state bit semantics: low bit (bit 0) for event alarms, high bit (bit 1) for fatal alarms.
		Clarified CRC8 calculation requires XOR with 0xFF at the final step.
		Added note that CRC verification is optional and last 8 bits can be discarded if not needed.
		Added reference to FAE or official website for further CRC8 application notes.
		Added ”One-Button Zero Setting Function” section in SPI chapter, including F.LOAD and F.OFS register descriptions and usage examples.

Table 1: Document Revision History

1 Product Information

1.1 Product Features

- Max. 24-bit resolution of one pole pair
- Supports 1-4096 pole pairs
- Dual 16-bit 2MHz SAR ADC
- Max. 36MHz SPI
- Programmable ABZ (1-65536 lines)
- Programmable UVW (1-256 pole pairs)
- Independent PWM absolute angle
- Auto linear & non-linear calibration
- Single pole pair post-calibration INL ≤ ±0.025°
- Off-axis applications INL ≤ ±0.06°
- Supports both on-axis and off-axis mounting
- Integrated programmable op-amp
- High bandwidth input 80MHz
- Ultra low latency 3μs
- Integrated high-precision TMR magnetic sensor
- Operating temp: -40°C to 125°C
- HFBP5x5-32L package



1.2 Typical Applications

- Servo motors
- Linear motors
- DDR direct drive motors
- Hollow joint robots
- Off-axis angle measurement
- Coreless motors

1.3 Product Introduction

KTM5900 is a 24-bit absolute angle TMR magnetic encoder that forms a high-speed, high-precision non-contact magnetic encoder module. It has the ability to read differential analog sine and cosine signals from the sensor at a maximum 2MHz sampling rate using a 16-bit SAR ADC, enabling angle calculation through its high-speed digital circuit and output position information.

KTM5900 provides versatile angle output modes to meet different application requirements. First, it supports up to 36Mbps SPI absolute angle output, and SPI can also be used to configure MTP (Multiple-Time Programmable memory). Additionally, it provides programmable ABZ quadrature pulse incremental output with up to 65536 lines, offering high resolution and precise position information. Moreover, KTM5900 supports programmable UVW incremental output with up to 256 pole pairs. Finally, KTM5900 supports PWM absolute angle output.

KTM5900 has many user-friendly features, such as automatic linear calibration, automatic non-linear calibration, Z signal calibration (when multiple Z signals are available, the system can select one for calibration), absolute position synchronization for multi-pole pair

applications, and programmable operational amplifier gain. KTM5900 has made some optimizations to its functional safety, such as SPI angle output with 8-bit CRC verification, and the integration of many self-diagnostic alarm functions, such as TMR Input Sine/Cosine Amplitude Anomaly, Input Undervoltage Detection, etc.

2 Overall Introduction

2.1 System Architecture

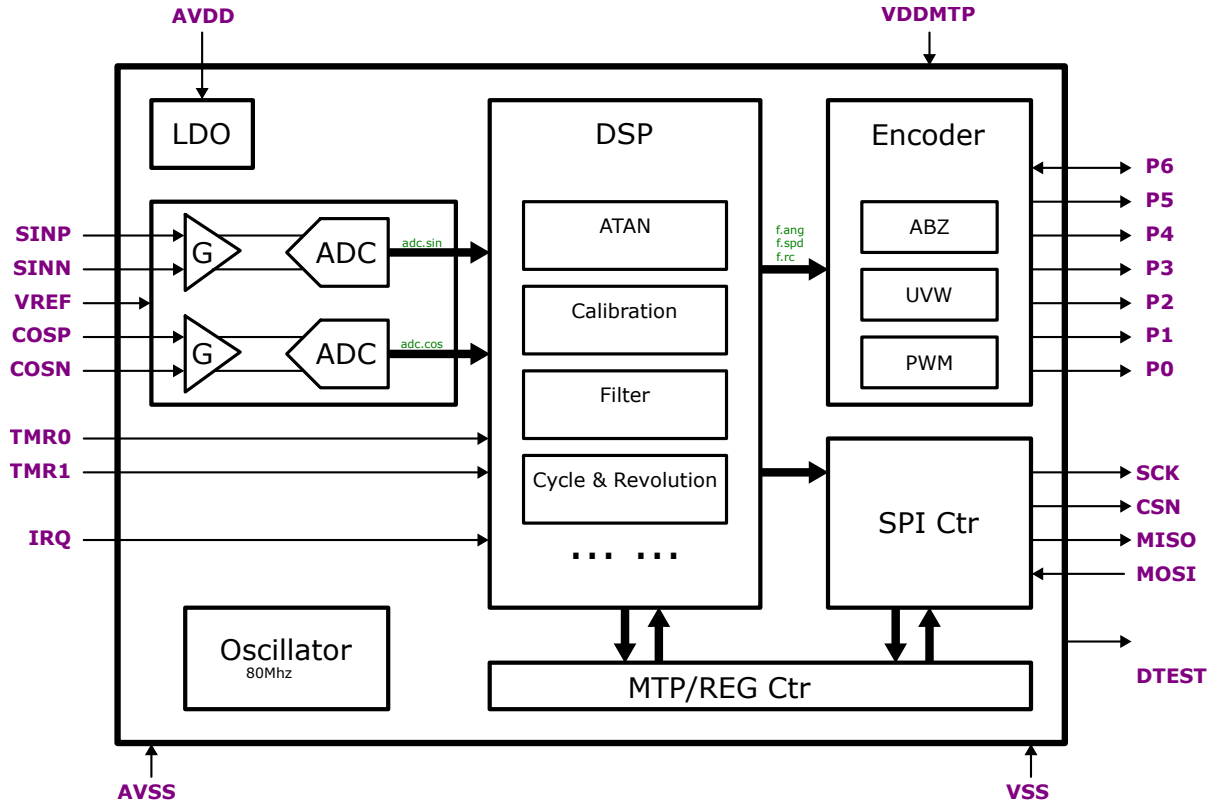


Figure 1: KTM5900 Chip Functional Diagram

KTM5900 is a versatile absolute angle encoder processor. It includes several functional modules, including a TMR sensor module, adjustable gain amplifier, high-speed SAR ADC module, subdivision module, correction and calibration modules, filter module, and a rich set of interface modules, which can be configured through registers for the desired encoder resolution. KTM5900 offers a wide range of output options, including ABZ/UVW/PWM/SPI interfaces.

The system is equipped with automatic calibration and adaptive functions to correct sensor offset, sine/cosine amplitude matching, and phase orthogonality, ensuring minimal angle error and jitter. Additionally, the KTM5900 SoC features an industry-leading 2MHz 16-bit SAR ADC to enhance performance and precision.

A significant advantage of KTM5900 is its ability to automati-

cally detect and correct non-linear errors during normal operation, with just a button press or an SPI command. Furthermore, KTM5900 integrates a 256-point error lookup table, allowing customers to improve absolute accuracy by writing non-linear error corrections from optical encoders into KTM5900. With the internally integrated high-precision TMR sensor and a single-pole magnet combination forming an encoder, both one-button self-calibration and the 256-point error lookup table can achieve INL≤0.025°.

2.2 Pin Definitions

Pin No.	Pin Name	I/O	Function
1	**AVSS**	I	Analog Ground
2	**VREF**	O	ADC Ref. Voltage
3	**VSSAMR**	I	Ground
4	**/**	N	NC
5	**/**	N	NC
6	**/**	N	NC
7	**/**	N	NC
8	**/**	N	NC
9	**AVSS**	I	Analog Ground
10	**AVDD**	I	Analog Power
11	**IRQ**	O	Alarm
12	**P6**	I/O	Mux. Parallel Output
13	**P5**	O	Mux. Parallel Output
14	**P4**	O	Mux. Parallel Output
15	**P3**	O	Mux. Parallel Output
16	**P2**	O	Mux. Parallel Output
17	**P1**	O	Mux. Parallel Output
18	**P0**	O	Mux. Parallel Output
19	**MISO**	O	SPI
20	**MOSI**	I	SPI
21	**CSN**	I	SPI
22	**SCK**	I	SPI
23	**VSS**	I	Ground
24	**DVDDL**	O	Digital 1.8V Output
25	**DVDD**	I	Digital Power Input
26	**ZREF**	I	0 Calib.Trigger
27	**/**	N	NC
28	**/**	N	NC
29	**DTEST**	I	Digital Test
30	**VDDMTP**	I	MTP Power
31	**AVDD**	I	Analog Power
32	**AVSS**	I	Analog Ground

Table 2: Pin List

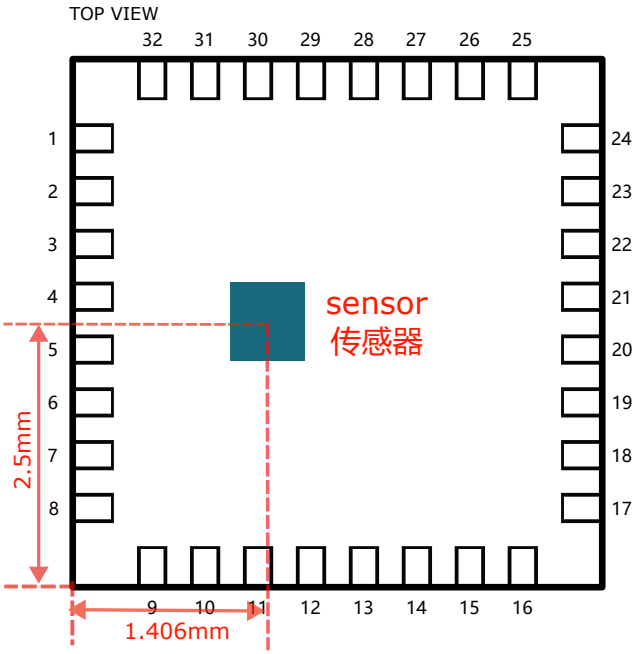


Figure 2: HFBP5x5-32L Top View

2.3 Application Circuit

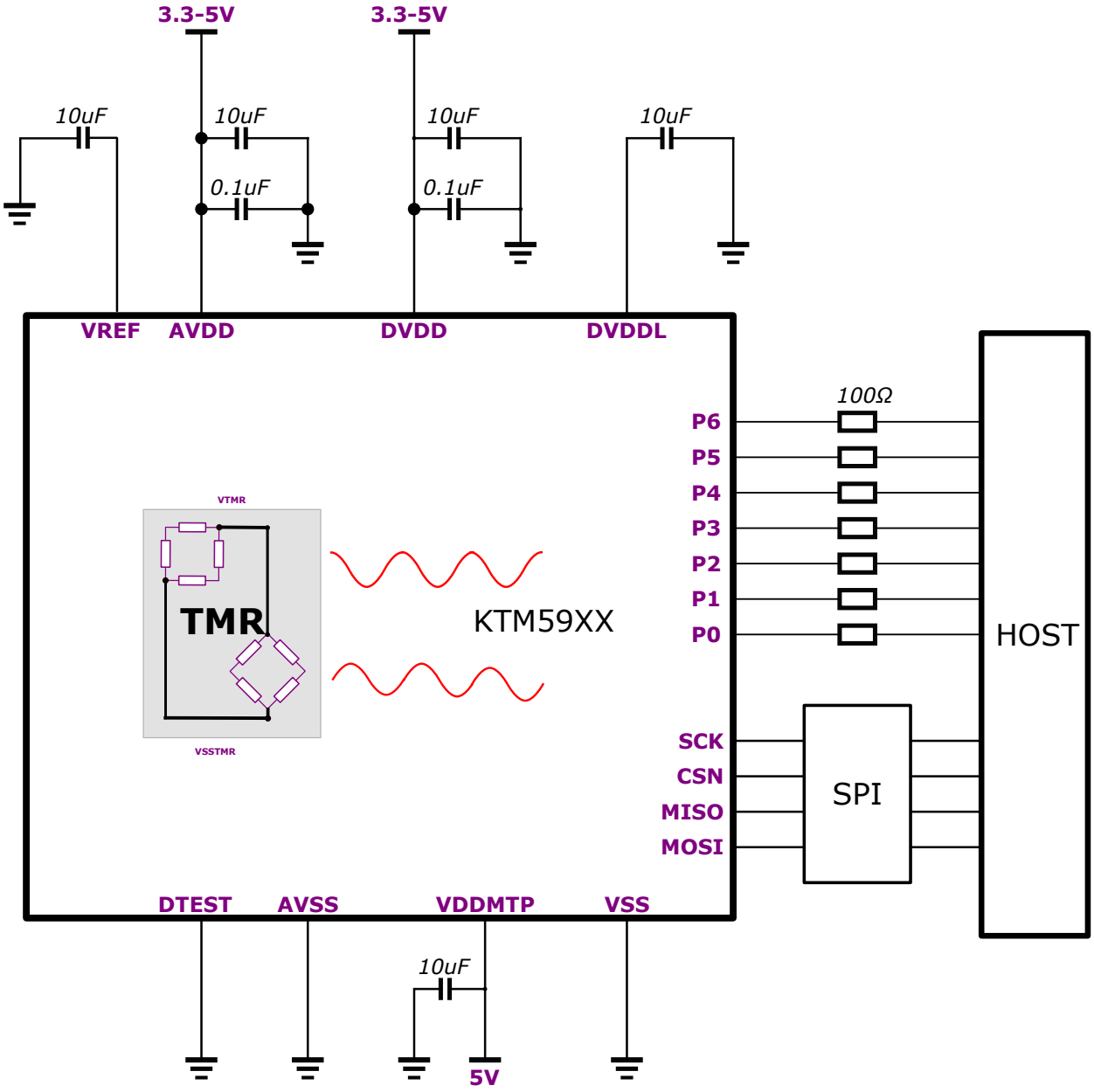


Figure 3: KTM5900 Application Circuit Diagram

The application circuit for KTM5900 is shown in Figure 3. The chip integrates a high-precision TMR sensor internally. After receiving analog input, KTM5900 can convert it into absolute angle information and transmit it to the control processor HOST through interfaces such as ABZ, UVW, SPI, and others. Ports P0-P5 can be programmed as ABZ, UVW, or their differential signals ~ABZ, ~UVW. It is important to note that the recommended capacitors in the schematic are necessary for ensuring system accuracy and stability.

2.4 Normal Operating Parameters

Parameter	Min.	Typical	Max.
Operating Voltage DVDD , AVDD	3.0V	3.3V-5V	5.5V
MTP Programming Voltage VDDMTP	4.5V	5V	5.5V
Magnetic Field Strength		30mT	80mT
Operating Current		32mA	
Startup Time		23ms	
Delay Time		0.5us	
Operating Temperature	-40°C		125°C
Rotation Speed			180,000rpm
ESD (HBM)		±5KV	

Table 3: Operating Parameters

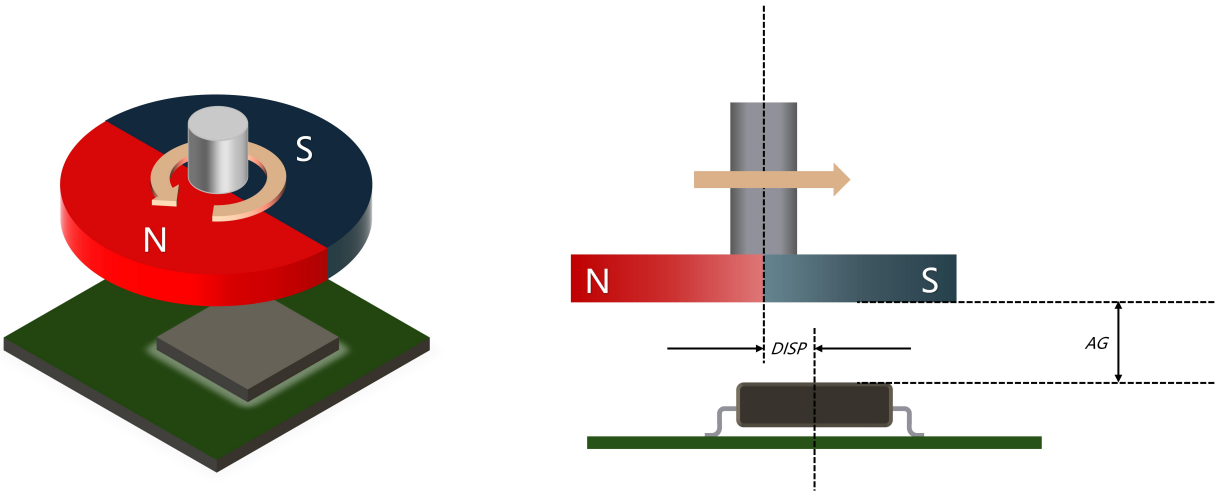
2.5 On-Axis Magnet Mounting Recommendations

Table 4: On-Axis Magnet Mounting Recommendations

Para.	Description	Min	Typ.	Max	Unit
D_{mag}	Radially magnetized magnet diameter		10	30	mm
T_{mag}	Recommended magnet thickness		2.5	5	mm
B_{pk}	Chip operating magnetic field	30		80	mT
AG	Air gap		2.0	5.0	mm
RS	Rotational speed			180	krpm
$DISP$	Mounting deviation		0	1.0	mm

Note: Special attention must be paid to the fact that the chip center and the sensor center are not at the same position. Alignment must be aligned with the sensor center.

Figure 4: Chip Positioning for On-Axis Magnet



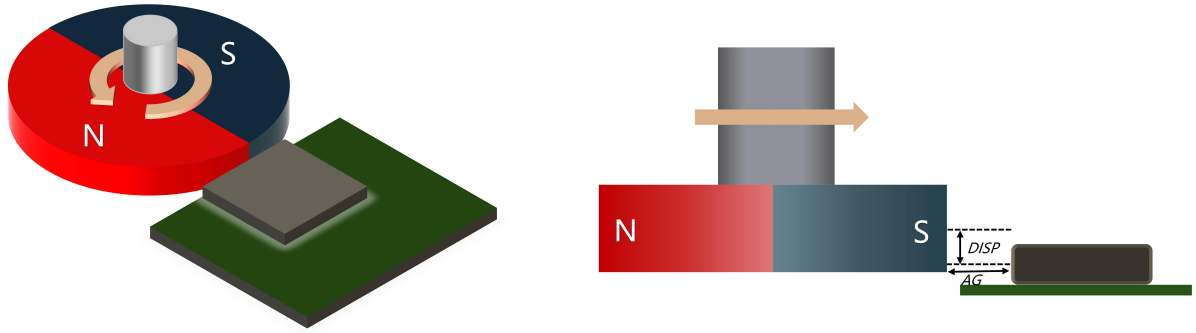
2.6 Off-Axis Magnetic Ring Mounting Recommendations

Table 5: Off-Axis Magnetic Ring Mounting Recommendations

Para.	Description	Min	Typ.	Max	Unit
D_{mag}	Inner diameter of radially magnetized magnet or magnetic ring	0	10	20	mm
D_{mag}	Outer diameter of radially magnetized magnet or magnetic ring	6	16	30	mm
T_{mag}	Recommended magnet thickness	1	4	8	mm
B_{pk}	Chip operating magnetic field	30		80	mT
AG	Air gap		2	5	mm
RS	Rotational speed			180	krpm
$DISP$	Mounting deviation	-5	0	5	mm

Note: Special attention must be paid to the fact that the chip center and the sensor center are not at the same position. For off-axis placement, the chip should be placed as close as possible to the sensor, i.e., the chip edge at PIN1-PIN8 should be placed close to the magnet.

Figure 5: Chip Positioning for Off-Axis Magnetic Ring



3 Electrical Parameters

Parameter	Min.	Typical	Max.
ABZ Output Frequency			20MHz
ABZ Output Current			2mA
ABZ Output Pulses	1		65,536
UVW Output Pulses	1		256
PWM Output Frequency		973Hz	
SPI Output VOH	VDD-0.4V		
SPI Output VOL			0.4V
SPI Output VIH	0.8VDD		
SPI Output VIL			0.2VDD
MTP Erase Cycles	1,000		
Output Noise (6 sigma)		0.01°	
Non-linearity Error		±0.025°	

Table 6: Electrical Parameters

4 Internally Integrated TMR Parameters

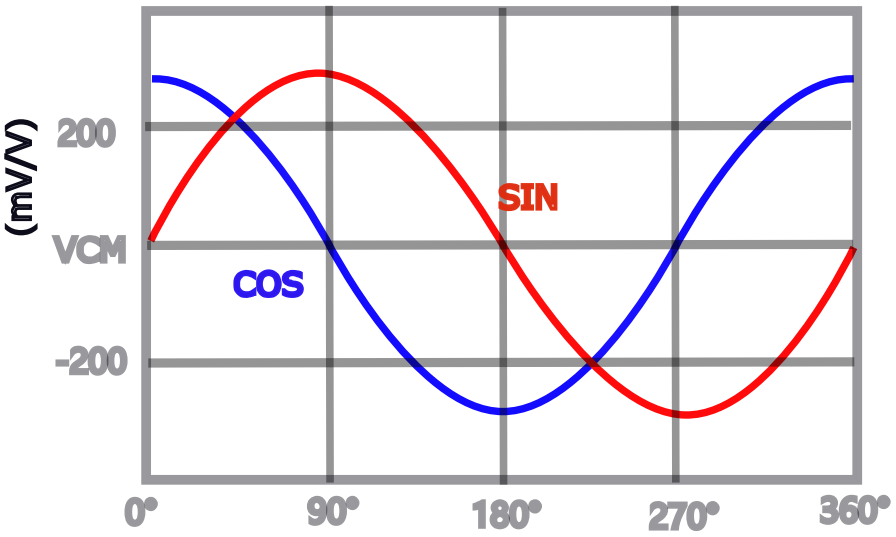


Figure 6: Integrated TMR Signal Output Schematic of KTM5900

The integrated TMR schematic of KTM5900 is shown in Figure 6. Within the magnetic field angle range of 0-360°, the TMR outputs a pair of orthogonal signals, SIN (sine) and COS (cosine). The relevant parameters of this TMR are shown in the following table:

Table 7: TMR Parameters

Parameter	Minimum	Typical	Maximum
Operating Magnetic Field Strength	30mT		80mT
Output Sensitivity		300mV/V	
Magnetoresistance	4KΩ	5KΩ	6KΩ
Magnetoresistance Temperature Coefficient		-0.0005	
Angle Error		0.2°	0.6°
Operating Temperature	-40 °C		125 °C
Storage Temperature	-40 °C		125°C
SMT Temperature			250 °C

5 SPI Communication and MTP Control

KTM5900 provides a reliable and efficient communication method through the SPI interface, facilitating communication between microcontrollers and peripheral devices. Additionally, it features internal MTP functionality for secure storage of configurations and calibration data. The SPI communication mode used is mode 0 with CPOL=0 and CPHA=0.

5.1 SPI Timing

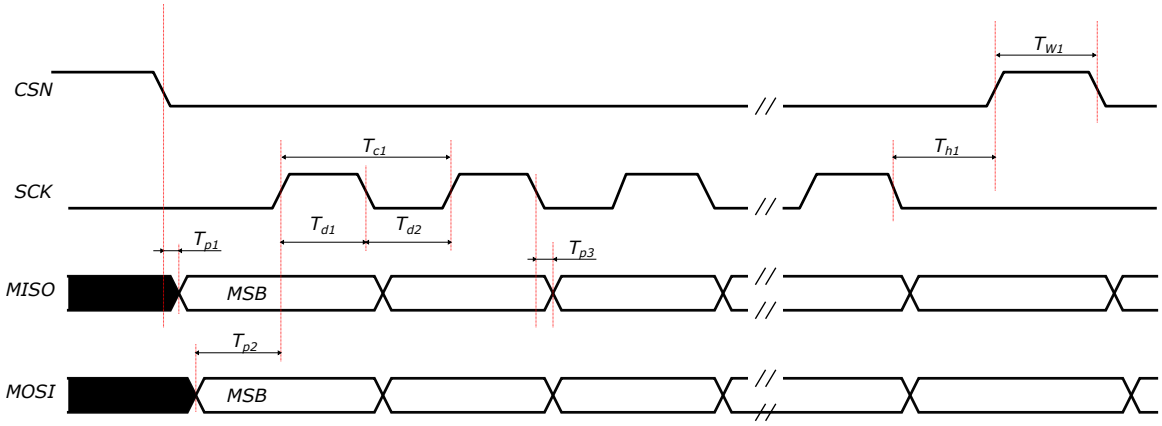


Figure 7: SPI Timing Diagram

Here, we can observe an SPI timing diagram in Figure 7 and a table of SPI timing parameters for KTM5900 products under 20pF load conditions in Table 8. This table lists the symbols for each parameter, their descriptions, and the minimum, typical, and maximum values in nanoseconds (ns). These parameters help define the timing requirements for SPI communication, ensuring reliable data transfer between microcontrollers using KTM5900 products and peripheral devices.

Symbol	Description	Min.	Max.	Unit
T_{c1}	SCK Clock Period	30		ns
T_{d1}	High Period of SCK Clock	15		ns
T_{d2}	Low Period of SCK Clock	15		ns
T_{p1}	Time interval between CSN falling edges and Valid data	50		ns ns
T_{p2}	Time interval between Valid data output and first SCK rising edges	15		ns
T_{p3}	Time interval between SCK falling edges and Valid data		8	ns
T_{h1}	Time interval between last falling edges and CSN rising edges		12.5	ns
T_{w1}	Hold Time of CSN	20		ns

Table 8: SPI Timing Parameters (with 20pF load conditions)

KTM5900 products use the SPI interface in CPOL=0 and CPHA=0 mode for communication between microcontrollers and peripheral devices. The SPI interface consists of four lines: SCK, MOSI, MISO, and CSN, implemented according to the SPI international standard. Data is transmitted in fixed-length 32-bit packets.

This SPI timing parameter table is very useful for understanding how to correctly use and debug the hardware and firmware design of the SPI interface. Please note that to ensure reliable data communication, hardware and firmware design should adhere to these timing parameters.

All these SPI parameters mentioned above are implemented in our provided hardware and firmware, which can be configured and optimized according to your application requirements. If you encounter any issues during usage, our technical support team is available to assist you.

In summary, the SPI interface of KTM5900 products is a powerful and versatile communication tool that can be widely used for communication between various microcontrollers and peripheral devices. By correctly using and understanding these SPI timing parameters, you can fully utilize its performance to meet your specific application requirements.

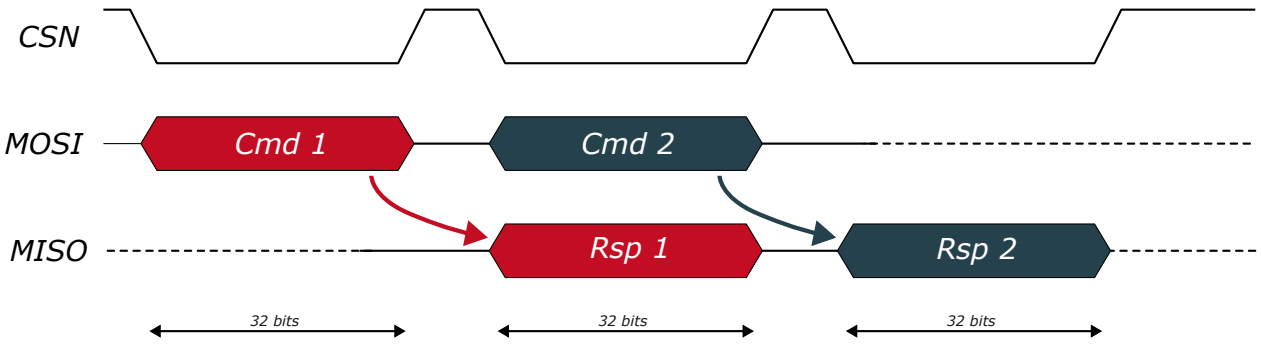


Figure 8: SPI Command and Response Timing Diagram

SPI communication employs an overlapping structure that allows sending the response of the previous command while transmitting the next command. Figure 8 illustrates an example of a single-device setup where the host controls a KTM5900 slave device.

5.2 SPI Commands

The chip supports several SPI commands as shown in Table 9:

- **Command 1: Write Multi-Pole Pair and Multi-Revolution Counter** used to configure angle output for quick configuration of multi-pole count and multi-revolution count.
- **Command 2: Register Write** writes the desired value to the corresponding register.
- **Command 3: Register Read** returns the register value for the respective address bits upon receiving the next SPI command.
- **Command 4: Angle and Status Read** returns the current angle value + status + CRC upon receiving the next SPI command.

The command length must meet specific requirements, and the specific mode used by KTM5900 products is determined by application requirements. More details will be provided when introducing detailed functionalities.

Command 1: Write Multi-Pole or Multi-Revolution Counter

6	1	3	Reserved	Multi-Pole Count	Revolution Count
31 30 29	28 27	26 25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

Command 2: Control Register Write

2	3	3	Reserved	Register Address	Register Data
31 30 29	28 27	26 25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

Command 3: Control Register Read

3	0	2	Reserved	Register Address	Ignore
31 30 29	28 27	26 25 24	23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

Response 3: Register Read Response

8-bit Data	Ignore
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Command 4: Angle and Internal Signal Read

1	0	3	0
31 30 29	28 27	26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Response 4: Angle and Internal Signal Response

0-54bit Revolution and Angle Output Programmable	2-bit State	8-bit CRC

Table 9: SPI Command List

5.3 Angle and Internal Signal Read (SPI Command 4)

Response 4 in the SPI communication protocol provides information about the angle and internal system signals. For example, if the response structure is 10-bit revolution count + 16-bit angle + 2-bit state + 8-bit CRC, the total response data is 36 bits. Let's break down the structure of this response:

- **Revolution Count (10 bits):** A 10-bit revolution count value in the response. This value indicates the number of complete revolutions the device has made.
- **Angle Data (16 bits):** The response includes a 16-bit angle value. This angle value represents the current position or angle of the device.
- **State Bits (2 bits):** Two bits in the response are dedicated to state information. These bits provide information about the system's status and any alarm conditions. The low bit (bit 0) set to 1 indicates event alarms configured in Section 13. The high bit (bit 1) set to 1 indicates a

fatal alarm condition, such as system startup failure.

- **CRC Data (8 bits):** The final 8 bits in the response are used for CRC (Cyclic Redundancy Check) data. CRC is a form of error-checking code to ensure data integrity during transmission. If CRC verification is unnecessary for your use case, you have the option to discard the last 8 bits of data.

5.3.1 CRC Data Explanation

The CRC data, which consists of the last 8 bits of the response, plays a crucial role in ensuring the integrity of transmitted data. It is used for error-checking and verification purposes. Here's a more detailed explanation of the CRC data:

- **CRC Calculation Formula:** The CRC check employs a specific polynomial formula $X^8 + X^2 + X + 1$. This formula is used to perform a mathematical calculation on the data to create the CRC value.
- **Initial Value:** The CRC calculation starts with an initial value of 00. This initial value is part of the formula and is used in the calculation process.
- **Result XORed with FF:** After the CRC calculation is performed, the result is XORed with 0xFF (hexadecimal) to create the final CRC value. This XOR operation is a standard step in CRC calculations.
- **Example Calculation:** Let's illustrate this with an example. Consider a response that includes a 10-bit revolution count, a 16-bit angle, and 2-bit state. If the received binary data is 1010 1100 1100 1101 1101 0000 0000 (in hexadecimal: ACC DD00), and the CRC8 checksum value is calculated as 47, the complete received data becomes ACCDD0047. This means that the CRC calculation has been applied to the entire response, including the revolution count, angle, state bits, and CRC itself.
- **Further Information:** For a more comprehensive understanding of CRC8 checksum calculations and its application in your specific context, you can contact the Field Application Engineer (FAE) or download the detailed application note from the official website. This resource will provide you with in-depth insights into CRC calculations and best practices for implementing data integrity checks.

5.3.2 CRC8 Reference Code

The following is the CRC8 reference code. Taking the example above where the transmitted data is 28 bits + CRC8 for a total of 36 bits, the transmitted data is 28 bits. Pad 4 zeros at the high bits to form a 32-bit data (0A CC DD 00), represented as data[31:0]:

Listing 1: CRC8 Reference Code

```
// Example code                          // Example
crc = 0x00;                              // crc = 0x00;
crc = CRC_TABLE[crc ^ data[31:24]];      // 0x36 = CRC_TABLE[0x00 ^ 0x0A];
crc = CRC_TABLE[crc ^ data[23:16]];      // 0xE8 = CRC_TABLE[0x36 ^ 0xCC];
crc = CRC_TABLE[crc ^ data[15:8]];       // 0x8B = CRC_TABLE[0xE8 ^ 0xDD];
crc = CRC_TABLE[crc ^ data[7:0]];        // 0xB8 = CRC_TABLE[0x8B ^ 0x00];
crc = crc ^ 0xFF;                        // crc = 0xB8 ^ 0xFF = 0x47;
```

The CRC_TABLE array is:

Listing 2: CRC8 Lookup Table

```
CRC_TABLE[256]={
 0x00, 0x07, 0x0e, 0x09, 0x1c, 0x1b, 0x12, 0x15, 0x38, 0x3f, 0x36, 0x31, 0x24, 0x23, 0x2a, 0x2d,
 0x70, 0x77, 0x7e, 0x79, 0x6c, 0x6b, 0x62, 0x65, 0x48, 0x4f, 0x46, 0x41, 0x54, 0x53, 0x5a, 0x5d,
 0xe0, 0xe7, 0xee, 0xe9, 0xfc, 0xfb, 0xf2, 0xf5, 0xd8, 0xdf, 0xd6, 0xd1, 0xc4, 0xc3, 0xca, 0xcd,
 0x90, 0x97, 0x9e, 0x99, 0x8c, 0x8b, 0x82, 0x85, 0xa8, 0xaf, 0xa6, 0xa1, 0xb4, 0xb3, 0xba, 0xbd,
 0xc7, 0xc0, 0xc9, 0xce, 0xdb, 0xdc, 0xd5, 0xd2, 0xff, 0xf8, 0xf1, 0xf6, 0xe3, 0xe4, 0xed, 0xea,
 0xb7, 0xb0, 0xb9, 0xbe, 0xab, 0xac, 0xa5, 0xa2, 0x8f, 0x88, 0x81, 0x86, 0x93, 0x94, 0x9d, 0x9a,
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 0x3e, 0x39, 0x30, 0x37, 0x22, 0x25, 0x2c, 0x2b, 0x06, 0x01, 0x08, 0x0f, 0x1a, 0x1d, 0x14, 0x13,
 0xae, 0xa9, 0xa0, 0xa7, 0xb2, 0xb5, 0xbc, 0xbb, 0x96, 0x91, 0x98, 0x9f, 0x8a, 0x8d, 0x84, 0x83,
 0xde, 0xd9, 0xd0, 0xd7, 0xc2, 0xc5, 0xcc, 0xcb, 0xe6, 0xe1, 0xe8, 0xef, 0xfa, 0xfd, 0xf4, 0xf3}
```

Abbr.	Full Name	Related Section
L	Linear Calibration	Section 7
N	Non-linear adjustment Control	Section 8
F	Filter Control	Section 9
S	SPI Serial Interface Control	Section 5
M	Multi Cycle Ctrl	Section 6
A	ABZ Incremental Interface Control	Section 10
U	UVW Interface Control	Section 11
P	PWM Interface Control	Section 12
E	IRQ & Event	Section 13

Table 10: Functional Block Names and Descriptions of Control Registers (ctrREG) Sections

5.4 SPI Module Control Registers

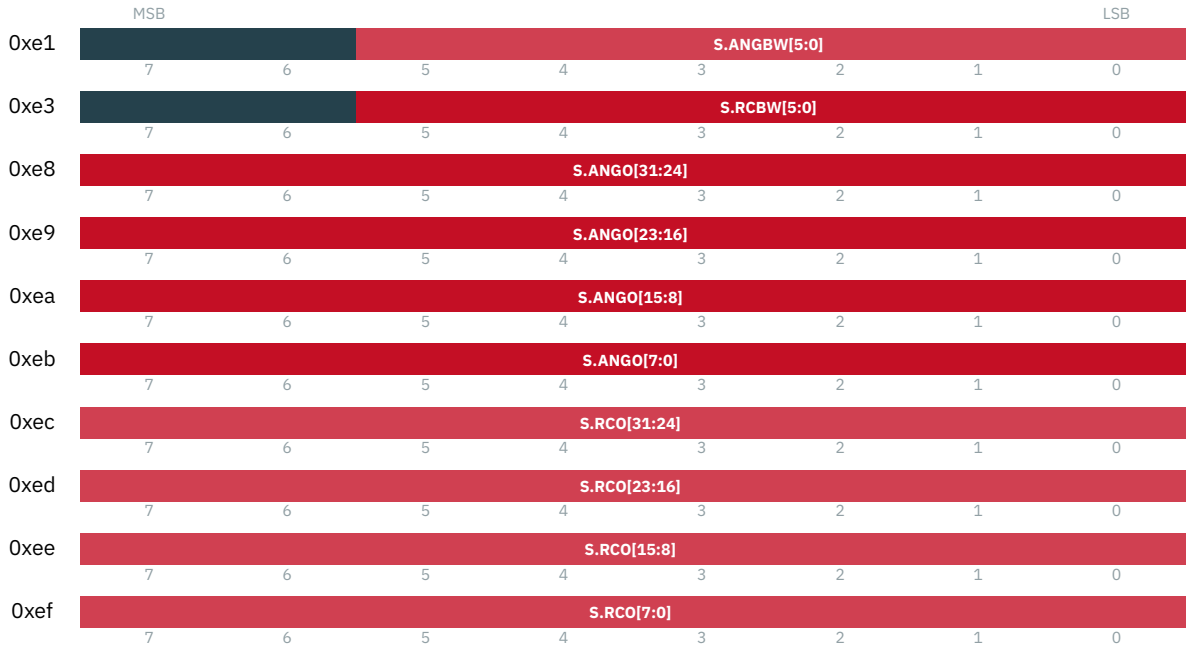


Table 11: SPI Module Control Register ctrREG Section S

5.5 SPI Angle Output Width Configuration

The width of various signal bits in the SPI output can be customized using the S.RCBW and S.AGBW registers. In this case, the total SPI output width may not strictly adhere to the standard 32-bit or 40-bit format. These output signals always start from the Most Significant Bit (MSB), and if the actual number of bits is less, the system will pad 1's after the Least Significant Bit (LSB) to ensure data integrity and consistency.

SPI Digital Output (Current Angle) Bit Width Parameter

Used to set the bit width of SPI angle data. When it does not reach the maximum value, bit width truncation will start from the MSB of the internal register.

SPI Digital Output (Current Revolution Count) Bit Width Parameter

Used to set the bit width of SPI revolution count data. When it does not reach the maximum value, bit width truncation will start from the LSB of the internal register.

5.6 SPI Output Angle/Revolution Count Offset

SPI Output Angle/Revolution Count Offset

Users can set offsets via SPI using the S.ANGO and S.RCO registers. For example, to decrease the output angle by 90 degrees, set the data in S.ANGO as 0100 0000 0000 0000 0000 0000 0000 0000; to decrease the revolution count by 1 revolution, set the data in S.RCO as 0000 0000 0000 0000 0000 0000 0000 0001.

5.7 One-Button Zero Setting Function

Due to the installation process, the encoder angle and the motor's electrical angle may not be perfectly aligned. Customers need to perform encoder-to-motor zero alignment. In this case, the operation can be performed through F.LOAD. The specific operation is as follows: By default, F.LOAD is 0. Set register F.LOAD to 1 to create a rising edge of the F.LOAD signal. When the rising edge is triggered, the angle output is set to zero. This operation applies to the angle output of SPI, ABZ, UVW, and PWM simultaneously.

One-Button Zero Setting Register

Additionally, F.OFS[29:0] is provided for angle zero point correction. F.OFS has a total of 30 bits, and its calculation formula is as follows:

Zero Point Angle Position

$$\text{SPI Output Angle} = \text{Actual Angle} - 360^\circ \times \frac{\text{F.OFS}}{2^{30}} \quad (1)$$

Additional Notes:

- Using F.LOAD for one-button zero setting: For example, if the current read angle is converted to 180°, set register F.LOAD from 0 to 1 to complete the one-button zero setting. At this time, the angle read from SPI output conversion is 0°, and F.OFS reads as 100000 00000000 00000000 00000000.
- Using F.OFS for zero setting: For example, if the current read angle is converted to 180°, to complete zero setting, F.OFS needs to be set to 100000 00000000 00000000 00000000. At this time, the angle read from SPI conversion is also 0°.

6 Multiple Pole Pairs and Multi-Turn Settings

	MSB							LSB
0x70	M.CPR[7:0]							
	7	6	5	4	3	2	1	0
0x71					M.CPR[11:8]			
	7	6	5	4	3	2	1	0
0x73	M.CC[7:0]							
	7	6	5	4	3	2	1	0
0x74					M.CC[11:8]			
	7	6	5	4	3	2	1	0
0x76	M.RC[31:24]							
	7	6	5	4	3	2	1	0
0x77	M.RC[23:16]							
	7	6	5	4	3	2	1	0
0x78	M.RC[15:8]							
	7	6	5	4	3	2	1	0
0x79	M.RC[7:0]							
	7	6	5	4	3	2	1	0

Table 12: Multiple Pole Pairs and Multi-Turn Settings Register `ctrREG Section M`

6.1 Number of Pole Pairs Setting

Number of Pole Pairs Setting

KTM5900 allows multiple pole pairs signals, such as the magnetic grating shown in Figure **??** or the optical encoder signal shown in Figure **??**, to be converted into absolute angles for one mechanical cycle or one rotation. The number of pole pairs can be easily set by configuring the M.CPR register. It's important to note that the set parameter is one less than the actual number of pole pairs. For example, if a customer is using a 32 pole pair magnet, the M.CPR should be set to 31. When the analog signal from the optical encoder is input to KTM5900, KTM5900 will output the corresponding angle from 0-360° for one rotation of the optical encoder.

6.2 Current Number of Pole Pairs and Current Number of Turns

Current Number of Pole Pairs Counter

The M.CC register represents the current number of pole pairs. This register is read-only. Upon initial power-up, customers can write the current number of pole pairs through SPI command 1.

Current Number of Turns

The M.RC register represents the current number of turns. This register is read-only. Upon initial power-up, customers can write the current number of turns through SPI command 1.

7 Linear Error Detection and Calibration (L)

KTM5900 integrates a linear error correction feature for eliminating linear errors caused by offset, gain, and phase errors in the x and y channels. This feature allows users to calibrate and correct linear errors, thereby improving the accuracy of their encoder applications.

The system supports two modes: online automatic calibration and manual parameter input, providing flexibility and efficiency in correcting linear errors.

7.1 Control Register ctrREG (L/Linear Calibration Function Block)

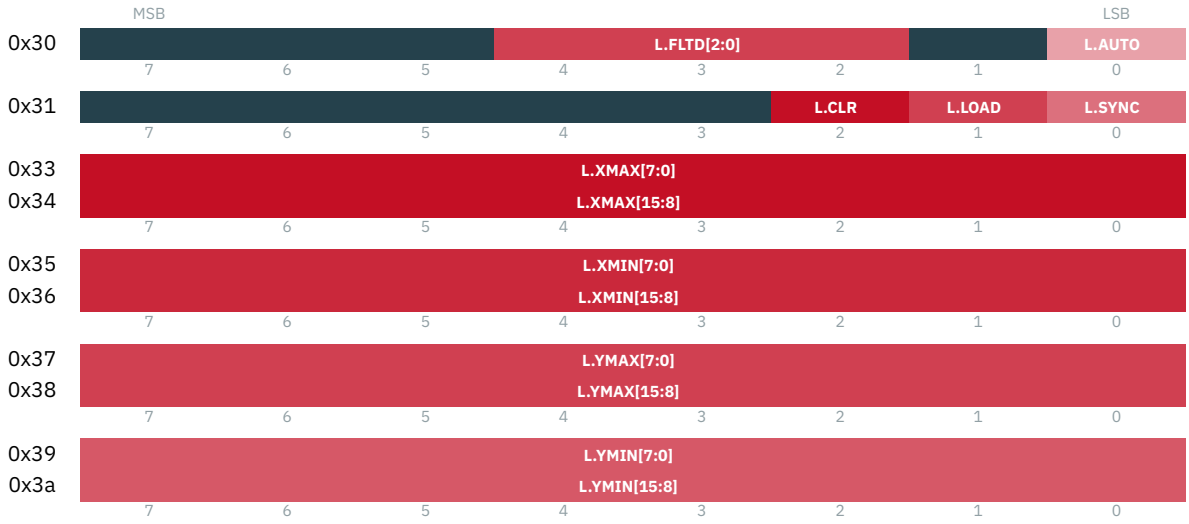


Table 13: Control Register ctrREG Function Block (Section L)

Table 13 provides a comprehensive overview of the control registers (CtrREG) used in the linear calibration process. The table displays addresses, register names, and their corresponding bit positions in a systematic and easily understandable manner. Each row in the table represents a specific register address, and its corresponding bits (B0 to B7) indicate control flags or parameters associated with that address.

The L.AUTO parameter is used to enable online automatic calibration mode for respective modules. ”Online” means that this calibration process is carried out in real-time, without the need to shut down or take the device offline. Real-time calibration is often essential as it can effectively reduce linear errors caused by environmental factors or device aging during operation.

L.FLTD is a control parameter with 3 bits (i.e., ranging from 0 to 7). This parameter plays a crucial role in the automatic fitting of correction parameters (such as L.XMAX, L.XMIN, L.YMAX, L.YMIN) by the linear correction module. In particular, L.FLTD is used for noise filtering.

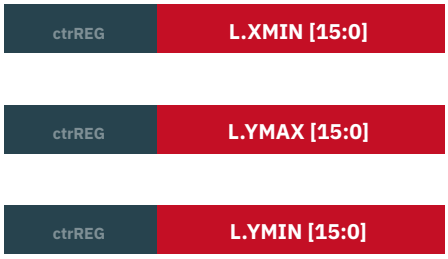
Due to the presence of noise in the measurement process, noise filtering is necessary. Here, the L.FLTD parameter is used to control the depth of the filter.

A higher value results in deeper filtering, which typically produces more stable correction parameters.

When the L.CLR parameter is set to 1, it clears the existing calibration parameters. The cleared calibration parameters are data used by KTM5900for linear calibration, not the values of the registers.

L.SYNC is an instruction for reading automatically calculated linear calibration values. After being set to 1, calibration values can be read through the L.XMAX, L.XMIN, L.YMAX, L.YMIN registers.

Corresponding to L.SYNC, L.LOAD is used to write respective parameters back into the funREG. After being set to 1, it writes the values of the L.XMAX, L.XMIN, L.YMAX, L.YMIN registers into the calibration module.



L.XMAX, L.XMIN, L.YMAX, and L.YMIN are the maximum and minimum values for the analog signals SIN and COS, respectively.

- Recommended steps for automatic linear calibration:
  Set L.FLTD to 2 or a greater value, run the motor for a few revolutions to reach a stable state, set the register L.AUTO to 1 to start automatic calibration. After the motor has run for more than 10 revolutions, the linear calibration is complete. Set L.SYNC to 1 to synchronize the calibration values to the registers L.XMAX, L.XMIN, L.YMAX, and L.YMIN. Use the MTP write instruction TOP.MCMD set to 0x02 to write the linear calibration values into MTP (see Section 12), to ensure that the values are not lost when power is turned off.
- Recommended steps for manual linear calibration:
  Collect the maximum and minimum values of the sine and cosine analog signals, and write them into the corresponding registers L.XMAX, L.XMIN, L.YMAX, and L.YMIN. After setting L.LOAD to 1, KTM5900will automatically load the values of the registers L.XMAX, L.XMIN, L.YMAX, and L.YMIN into the linear calibration module. When the calibration effect appears to be good, use the MTP write instruction TOP.MCMD set to 0x02 to write the linear calibration values into MTP (see Section 12), to ensure that the values are not lost when power is turned off.
- The system automatically fits linear error (gain error, offset error, phase error) parameters based on real-time motion information of the motor. Although it is not required that the motor must operate in a high-speed stable state, it is recommended to perform the calibration in such a state to improve the accuracy and speed of fitting.
- After calibration is complete, the system will use the fitted parameters to perform real-time linear calibration. If environmental factors cause the linear error to

change, automatic calibration can be restarted to update the parameters.

- If the system's linear error changes slowly, consider keeping the automatic calibration mode continuously enabled. In this way, the system will adjust the fitting parameters in real-time to adapt to changes in error.

8 Non-linear Error Detection and Correction Module (N)

In KTM5900, the non-linear error detection and correction module (referred to as the N module) is crucial for ensuring high precision and reliability in the angle encoder system. Due to their physical properties and limitations in the manufacturing process, angle encoders' output signals may be affected by non-linear errors. These errors can cause a deviation between the encoder output and the actual angle. To address this issue, we have designed a system comprising multiple specialized modules to precisely correct these non-linear errors.

	MSB							LSB
0xa0						N1.INTP	N1.EN	N256.EN
	7	6	5	4	3	2	1	0
0xa1	N1.MSBI[3:0]							
	7	6	5	4	3	2	1	0
0xa2			N1.PMTP	N1.LOCK		N1.AUTO		
	7	6	5	4	3	2	1	0
0xaf	N256.OPR	N256.RW	N256.INDX[5:0]					
	7	6	5	4	3	2	1	0
0xb0	N256.REG0[7:0]							
0xb1	N256.REG0[15:8]							
	7	6	5	4	3	2	1	0
0xb2	N256.REG1[7:0]							
0xb3	N256.REG1[15:8]							
	7	6	5	4	3	2	1	0
0xb4	N256.REG2[7:0]							
0xb5	N256.REG2[15:8]							
	7	6	5	4	3	2	1	0
0xb6	N256.REG3[7:0]							
0xb7	N256.REG3[15:8]							
	7	6	5	4	3	2	1	0
0xb8	N256.REG4[7:0]							
0xb9	N256.REG4[15:8]							
	7	6	5	4	3	2	1	0
0xba	N256.REG5[7:0]							
0xbb	N256.REG5[15:8]							
	7	6	5	4	3	2	1	0
0xbc	N256.REG6[7:0]							
0xbd	N256.REG6[15:8]							
	7	6	5	4	3	2	1	0
0xbe	N256.REG7[7:0]							
0xbf	N256.REG7[15:8]							
	7	6	5	4	3	2	1	0

Table 14: Non-linear Error Detection and Correction Module Registers ctrERG Section N

- **One-Click Self-Calibration Module** The one-click self-calibration module can complete data iteration when the motor rotates above 200rpm. KTM5900 automatically calculates the non-linear error and stores it in MTP.
- **Calibration Module (256 Points)** The 256-point calibration module provides more reference points for finer calibration. It offers 256 reference points, each with a specific angular position, optimizing angle measurement across a broader range.

Through the integrated application of these modules, KTM5900 can effectively detect and correct non-linear errors in the angle encoder, ensuring high precision and reliable angle measurement in various application environments. This systematic approach not only enhances the accuracy of measurements but also strengthens the system's adaptability, maintaining stable and reliable performance under different working conditions.

8.1 Automatic Fitting of Errors in One-Click Self-Calibration Module

One-Click Self-Calibration Request

When N1.AUTO is set to 1, calibration data reference automatic fitting is enabled. In this mode, the system continuously calibrates and computes and updates the latest calibration data references. These data iterate and stabilize based on real-time operation and are temporarily stored internally, not readable externally.

One-Click Self-Calibration Module Enable

When N1.EN is set to 1, the calibration module is activated.

One-Click Self-Calibration Module Online Interpolation Enable

When N1.INTP is set to 1, the one-click self-calibration online interpolation function is enabled. This function calculates the curve interpolation between the current angle and the nearest reference point, providing smoother and more continuous calibration data, enhancing the continuity and accuracy of the output data.

Locking Calibration Results in N1.AUTO Mode

When N1.AUTO is set to 1 and N1.LOCK is 0, calibration data will iterate and stabilize based on operational data. Changes will continue until N1.LOCK is set to 1, at which point the internal registers will stop updating the computed results.

Storing Calibration Results to MTP in N1.AUTO Mode

When N1.PMTP is set to 1, the internal one-click self-calibration data will be written to MTP. Since writing to MTP takes some time, it is recommended to lock the internal calibration reference data before writing, i.e., set N1.LOCK to 1.

In summary, using the automatic one-click self-calibration feature involves the following steps: first, start the motor and rotate it uniformly at 4000rpm or above; second, start the calibration module by setting N1.AUTO to 1; third, enable one-click self-calibration online interpolation by setting N1.INTP to 1; fourth, wait for the motor calibration to achieve the desired effect, typically within 5s, then lock the calibration results by setting N1.LOCK to 1; fifth, store the calibration results to MTP by setting N1.PMTP to 1; sixth, enable the one-click self-calibration module by setting N1.EN to 1 and setting the registers involved in previous steps to 0, completing the one-click self-calibration, and stop the motor rotation.

8.2 Calibration Module (256 Points)

This module is a high-precision non-linear calibration tool that internally stores 256 precise reference point correction

values. The 256 correction values are the differences between KTM5900 and ideal values. These reference points are evenly distributed across the angular range from 0 to 360 degrees, each corresponding to a specific angular position. This design allows the system to automatically apply preset correction values when the encoder's output signal passes these reference points or their nearby positions. Such corrections help correct the signal's non-linear errors, achieving higher accuracy and reliability in various application scenarios.

The module is particularly suitable for scenarios requiring highly precise calibration, such as in conjunction with high-precision optical encoders, ensuring data synchronization and consistency between them. This significantly enhances the overall precision and stability of the system, especially in fields like precision measurement and high-speed motion control.

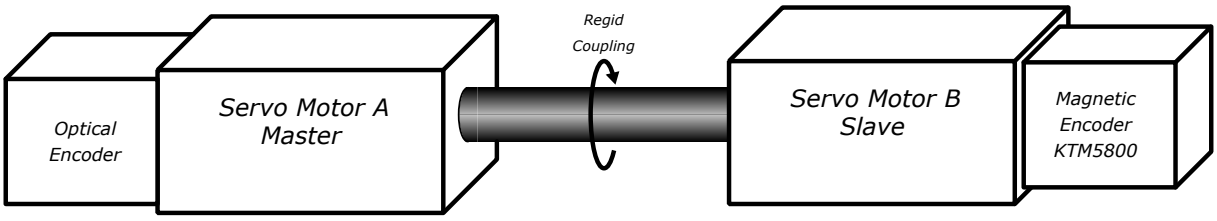


Figure 9: Non-linear Calibration in Conjunction with Optical Encoders

ctrREG	N256.EN

256 Calibration Module Enable

When N256.EN is set to 1, the 256-point non-linear calibration module is enabled, and calibration reference data is sourced from MTP.

8.3 Representation of Calibration Data (256 Points)

The 256-point calibration data is stored in Multi-Times Programmable memory (MTP). The calibration data for each reference point is represented by 16 bits, collectively named N256.REF[255:0].

ctrREG	N256.MSBI [3:0]

MTP Calibration Data (256 Points) MSB Index

KTM5900 internal angle data is 30 bits, while calibration data is only 16 bits. The N256.MSBI register specifies which position in the 30-bit angle data the 16-bit calibration data's Most Significant Bit (MSB) should correspond to.

Since the 256-point correction value is the difference between the magnetic position and the ideal value, the error angle represented by the correction value `angle.error` is a signed floating-point number between negative 180° and positive 180°. The correction value is calculated as follows, and the two's complement is taken for negative values.

$$\texttt{N256.REF}[x] = \text{unsigned}(\texttt{angle.error} \times \frac{65536}{360} \times 2^{(12-\texttt{N256.MSBI})})$$

Application Example

Assuming the input angle is $ANG_{in} = 45$ degrees, to calculate the calibration error angle, we can follow these detailed steps:

1. Determine the reference point: First, determine the calibration reference point corresponding to the 45-degree angle. In KTM5900, we have 256 calibration reference points evenly distributed from 0 to 360 degrees. Since each reference point covers an angle of about $360/256 \approx 1.40625$ degrees, the 45-degree angle roughly corresponds to the 32nd reference point, i.e., the 16-bit reference point `N256.REF`[31] (since indexing starts from 0).

2. If the angle error `angle.error` is -1° and N256.MSBI is 13, the correction value is calculated using the following formula:

$$\texttt{N256.REF}[31] = \text{unsigned}(-1 \times \frac{65536}{360} \times 2^{(12-13)}) = 65445$$

9 Filter Module (F)

KTM5900 incorporates a dedicated low-pass filter capable of operating in fixed bandwidth and adaptive dynamic modes, used for real-time processing of angle and velocity data. This filter enables users to obtain smoother and more accurate measurements of angle and velocity.

Table 15 lists the various addresses and corresponding data bits used for the digital filter. These parameters are primarily used to adjust the filter bandwidth, operating modes, etc.

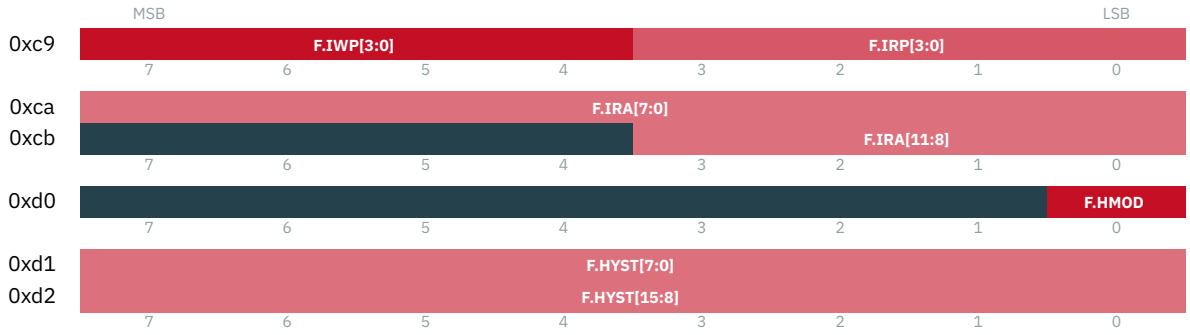


Table 15: Control Registers for the Filter (Section F)

9.1 Parameters of the Dedicated Low-Pass Filter

The dedicated low-pass filter has several important parameters that can be used to finely adjust the filter's performance and characteristics, including but not limited to the filter's depth[1], reset angle, and reset strength.

ctrREG	F.IWP [3:0]

Filter Working Depth Coefficient

F.IWP is a key parameter for controlling the depth or working strength of the filter. This parameter has a significant impact on the mathematical model of the filter. The larger the value of F.IWP, the deeper the filtering depth, the less the noise, and the slower the response of KTM5900. The default value of F.IWP is 8, and it is generally not recommended for customers to set F.IWP greater than 9.

[1] "Filter depth" is not a standard academic term, but it is widely used in engineering practice. Generally speaking, a filter with a deep depth (large numerical value) refers to a filter with a relatively small bandwidth, high noise removal capability, but slower response.

Filter Reset Critical Angle

ctrREG	F.IRA [11:0]

When the dedicated low-pass filter is enabled, the F.IRA parameter allows the system to automatically reset the filter when the difference between the input and output angles of the filter module exceeds the critical angle

controlled by F.IRA. This is a very useful adaptive mechanism, especially suitable for when the system's state changes significantly.

$$\text{Filter Reset Critical Angle} = \text{F.IRA} \times \frac{360^\circ}{4096} \tag{2}$$

Filter Reset Depth Coefficient

ctrREG	F.IRP [3:0]

IIR-filter Reset Power

Meanwhile, F.IRP is used to precisely control the "strength" of the filter during a reset. When the system detects a need for a filter reset, the original filter working depth coefficient F.IWP will be temporarily replaced by the filter reset depth coefficient F.IRP. The value of F.IRP can be set to the same value as F.IWP.

9.2 Hysteresis Settings

Hysteresis, also known as magnetic lag, is a common term in the automation industry, typically used to describe a phenomenon in sensors when detecting objects or measuring physical changes. Hysteresis can be defined as the error amount between the applied control signal and the system's resulting changes. In KTM5900, hysteresis is placed at the filter output position to prevent extremely minor signal interferences from causing high-order changes in the angle signal.

In KTM5900, fixed offset hysteresis is provided. When the direction changes, the lag module will offset the input angle with a preset hysteresis value. This means that when using this type of hysteresis, there will be a fixed angle offset in a certain direction (clockwise or counterclockwise). The figure below shows an example of input and output angles.

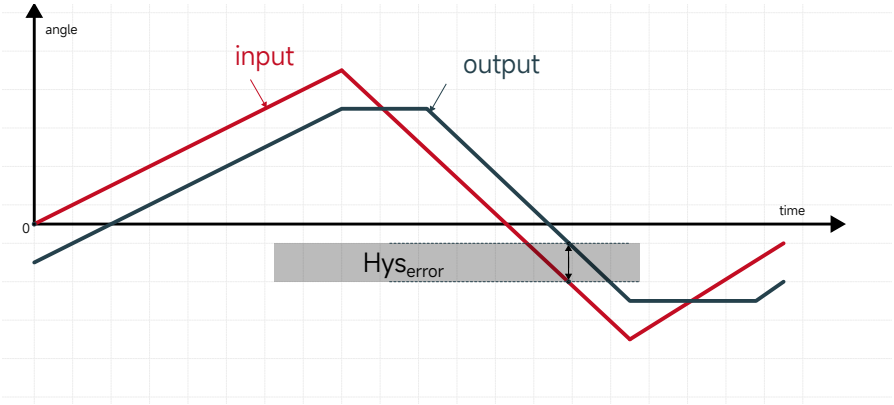


Figure 10: Fixed Offset Hysteresis.

ctrREG	F.HYST [15:0]

Hysteresis Error Value

Comprising a 16-bit unsigned integer (*unsigned*), used for setting the hysteresis angle, and the correspondence with the angle is calculated according to the formula below.

$$\text{Hysteresis Error (degrees)} = 5.625^{\circ} \times \frac{unsigned(\text{F.HYST})}{2^{16}} \quad (3)$$

This type of hysteresis setting is located at the output position of the filter in the KTM5900 chip, ensuring that the system maintains a stable output in the presence of changes in sensor signals or noise, thereby providing more accurate measurement and control. By utilizing the hysteresis effect, the KTM5900 chip can reduce false alarms caused by temporary fluctuations or noise, ensuring that the system provides reliable performance under various conditions.

10 ABZ Encoder Output Module (A)

ABZ signal output is a common form of output for angle encoders. It provides encoder position information mainly through three signal lines, namely A, B, and Z[2]. Among them, A and B signals are two orthogonal signals with a phase difference of 90 degrees, used to determine the rotation direction and relative position of the encoder; the Z signal is a pulse signal that appears only once per revolution, used to provide an absolute position reference for the encoder.

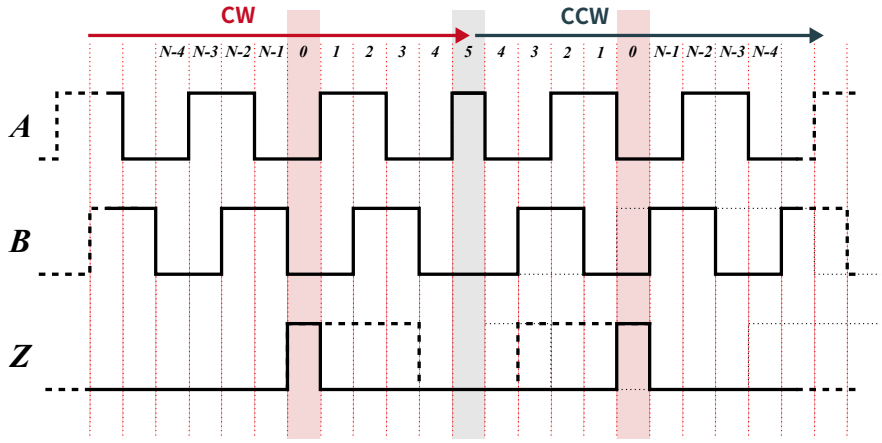


Figure 11: ABZ Output Timing

In KTM5900, we have a dedicated module to control the output of ABZ signals, as shown in Figure 13. The main function of this module is to convert the internal numerical angle values into A, B, Z digital signal outputs. To better adapt KTM5900 to various application scenarios, we provide users with modifiable related parameters, such as resolution, output frequency, and signal polarity.

The angular position increment output of KTM5900 is accomplished by outputting incremental signals A and B. AB incremental signals have a maximum of **24-bit resolution**[3], meaning that in each **rotation cycle**[4], it can provide up to $2^{24} = 16'777'216$ steps, and A, B signals each have an accurate $PPT = 2^{24}/4 = 4'194'304$ pulse cycles per revolution.

For the convenience of users in setting the operating parameters of ABZ, we store these parameters in Section A of CtrREG, and the specific settings are shown in Table 20.

[2] We can refer to Figure 11, where the phase difference between A and B signals is used to indicate the direction of rotation. Specifically, when rotating clockwise, the A signal leads while the B signal follows; conversely, when rotating counterclockwise, the B signal leads while the A signal follows. Notably, during the power-up period, all three ABZ signals maintain a high level.

[3] In the engineering field, Period Per Turn PPT is commonly used to represent resolution. For a 24-bit resolution, $PPT = 2^{\text{resolution bits}}/4$, and this parameter is controlled by A.PPT. Incremental interface is a common interface method that can provide continuous position information.

[4] In multi-turn applications, the standard is based on one full rotation of the outer circle.

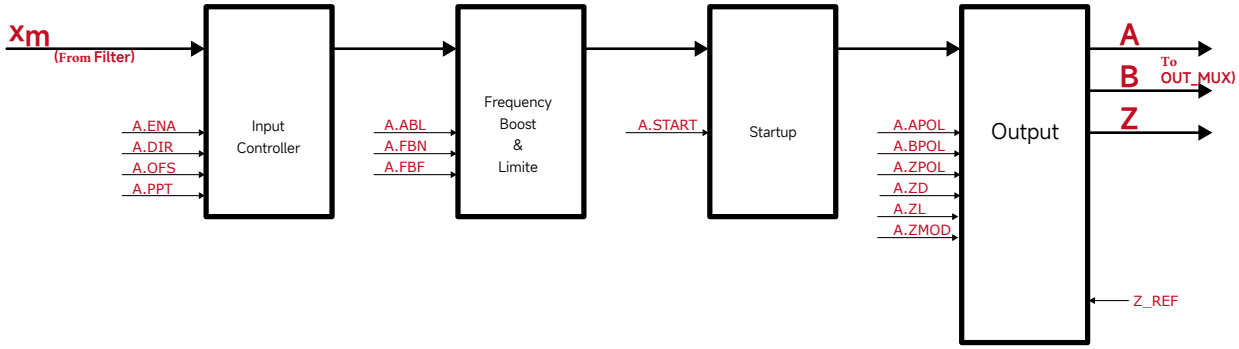


Figure 12: System Structure of ABZ Module

	MSB							LSB
0xf0				A.ZPOL	A.BPOL	A.APOL	A.DIR	A.ENA
	7	6	5	4	3	2	1	0
0xf1			A.ZL[1:0]		A.ZD[1:0]		A.ZMOD[1:0]	
	7	6	5	4	3	2	1	0
0xf2	A.PPT[7:0]							
0xf3	A.PPT[15:8]							
0xf4	A.PPT[23:16]							
	7	6	5	4	3	2	1	0
0xf5	A.OFS[7:0]							
0xf6	A.OFS[15:8]							
	7	6	5	4	3	2	1	0
0xf7	A.ABL[7:0]							
	7	6	5	4	3	2	1	0

Table 16: Control Registers for ABZ ctrERG Section A

10.1 Input Control

ctrREG	A.ENA

Module Enable Parameter

This parameter controls the start and stop functionality of the ABZ module. The default value is 1, indicating that the module is enabled. However, when set to 0, the ABZ module will stop working, and both the module's input and output will be paused. To change the operating parameters of the ABZ module, we need to follow the steps listed in Table 17. First, we need to turn off the ABZ module, then change the required parameters, which can be rewritten directly through SPI or read from MTP. After completing all parameter changes, restart the ABZ module, and it will operate with the new parameters.

Please note: When A.ENA =1, all changes to the ABZ control registers listed in Table 20, except for A.ENA, will not be immediately reflected in

Step	Description
1	Disable the ABZ module, set A.ENA =0.
2	Change the relevant parameters. Parameters can be rewritten directly through SPI or read from MTP.
3	Restart the ABZ module, set A.ENA =1. At this point, ABZ will operate with the new parameters.

Table 17: Steps for Rewriting Control Registers of ABZ

the operating registers and will not immediately change the actual operating parameters of ABZ. To change the module's operating parameters, the steps mentioned above must be followed.

ctrREG **A.DIR**

Input Angle Direction Parameter

This parameter is used to control the rotational direction of the ABZ signals. Its default value is 0. However, when we set it to 1, the input angle value of the ABZ module will be reversed.[5] If for some reason, such as assembly or the definition of rotation direction, it is necessary to adjust the direction of the ABZ signal output, we can achieve this by changing A.DIR.

[5] For example, when the A signal leads the B signal by 1/4 cycle during positive direction rotation, then in the negative direction rotation, the A signal will lag the B signal by 1/4 cycle.

ctrREG **A.OFS [15:0]**

Angle Offset Parameter

This is a 16-bit unsigned value used to set the angle offset for ABZ output. This offset value will be added to the high 16 bits of the ABZ module's input angle. Using the following formula, we can calculate the actual angle offset value:

$$\text{ABZ Output Angle Offset (degrees)} = 360 \times \frac{\text{A.OFS}}{2^{16}} \tag{4}$$

ctrREG **A.PPT [23:0]**

Angle Resolution Parameter

Resolution is used to describe the smallest angle that the ABZ signal can discern per turn. To accommodate multi-turn applications, A.PPT is designed as a 24-bit unsigned integer. Its default value is 4095 (4096 lines), used to determine the resolution of ABZ. Even in multi-turn applications, each turn of rotation is still calculated as 360 degrees. The correlation between A.PPT and the actual resolution can be seen in Table 18. The actual resolution can be calculated through the following formula:

A.PPT [23:0]	AB Resolution Pulses/Turn	AB Steps per Turn Steps/Turn
0	1	4
1	2	8
2	3	12
...	...	...
1021	1022	4088
1022	1023	4092
1023	1024	4096

Table 18: ABZ Resolution

$$\text{Actual Resolution (degrees)} = \frac{360^\circ}{(\text{A.PPT} + 1) \times 4} \tag{5}$$

10.2 ABZ Output Frequency Limiting

ctrREG **A.ABL [7:0]**

ABZ Output Maximum Frequency Limit Parameter

The A.ABL parameter is used to set the maximum output frequency for the A and B signals. With a main frequency of $80MHz$, we can use the following formula to calculate the actual maximum frequency limit for the A or B signal:

$$\text{Maximum Frequency}[MHz] = \frac{20MHz}{\text{A.ABL} + 1} \tag{6}$$

Based on this maximum frequency limit, we can also calculate the maximum rotation speed for ABZ:

$$\text{Maximum Rotation Speed}[rpm] = 60 \times \frac{20MHz}{\text{A.ABL} + 1} \times \frac{1}{\text{A.PPT} + 1} \tag{7}$$

However, it's important to note that if the rotation speed exceeds this maximum frequency limit, the A and B signals will output at the maximum frequency. Additionally, depending on the settings of the IRQ module, the system may issue an overspeed warning. In such cases, due to the mismatch between the frequency of A and B and the actual rotation speed, the angle values obtained from the output of the ABZ module may lag behind the actual angle values.

This frequency limiting mechanism plays a vital role in ensuring the stability and reliability of the ABZ signal output. By preventing the A and B signals from exceeding the maximum frequency, it helps to avoid potential issues caused by signal distortion or processing limitations of the receiving system. Users should carefully set the A.ABL parameter according to the specific requirements of their application scenario to ensure optimal performance of the ABZ encoder output.

10.3 Output Control

ctrREG	A.APOL

ctrREG	A.BPOL

ctrREG	A.ZPOL

Inversion Parameters for Signals A, B, and Z

These three parameters are all set to 0 by default. When set to 1, they will correspondingly invert the A, B, and Z signals. This inversion feature can be very useful in certain specific application scenarios, for example, when the polarity of the output signal is opposite to what is expected, this feature can be used for adjustment.

ctrREG	A.ZMOD [1:0]

Z Signal Output Mode Parameter

The output mode of the Z signal[6] varies with different settings, corresponding to different output modes. Different output modes can meet different application needs, ensuring that the chip can adapt to various working environments. Please refer to Table 19 for specifics.

A.ZMOD	Z Signal Output Mode
00	No Z output
11	No Z output
01	Controlled by chip pin ZREF
10	Normal mode

Table 19: Z Signal Output Modes

- When A.ZMOD $= 00$ or A.ZMOD $= 11$, no Z output pulse is generated, and the Z output is in an inactive state[7].
- When A.ZMOD $= 01$, a Z pulse is generated only when chip pin ZREF $= 1$. This mode is suitable for linear or rotational applications where the CPR (Counts Per Revolution) is 1[8].
- When A.ZMOD $= 10$, a Z pulse is generated (synthesized) at the output position determined by ABZPH for each revolution. This is a common mode for single-turn incremental and multi-turn absolute applications[9].

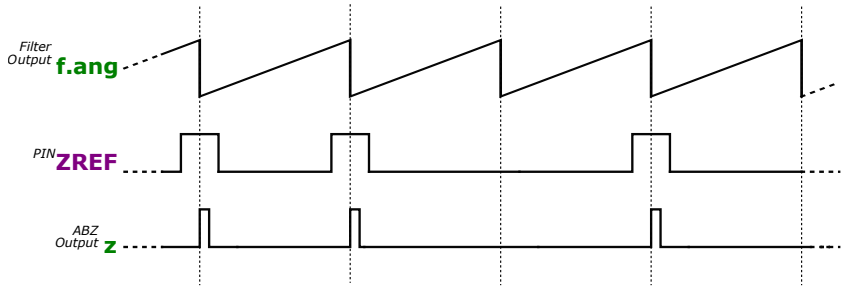


Figure 13: Diagram for A.ZMOD $= 10$, indicating the selection of the Z signal

Position and Width of the Z Signal

The rising edge of the Z signal occurs once per revolution at the zero position. The position and width of the Z signal can be set using ZL[1:0] and ZD[1:0] bits. By default, the ZL[1:0] and ZD[1:0] parameters are both set to 00[10].

[6] Z signal, also known as the Index signal or zero position signal. In encoder applications, the Z signal is often used to provide a reference point to help the system determine the exact position of the object.

[7] This mode is typically used in applications that do not require Z signal output.

[8] In this mode, the generation of the Z pulse is closely related to the state of the external pin $ZREF$, providing users with a flexible way to control the output of the Z pulse.

[9] Multi-turn absolute applications are typically used in applications where it's necessary to track the position of an object across multiple complete rotations, such as in motor position control.

[10] This means that, if no settings are made, the position and width of the Z signal will both be their default values.

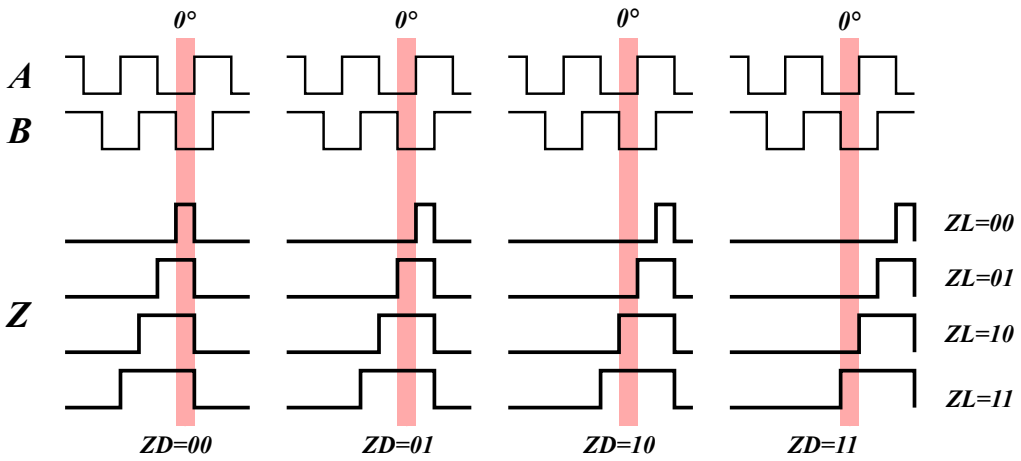


Figure 14: Width ZL and Position ZD of the Z Signal for AB

11 UVW Encoder Output (U)

The simulation of UVW output signals is crucial for the efficient commutation of three-phase motors. These signals emulate the output of three Hall effect sensors, characterized by a 50% duty cycle and a phase shift of 120°, ensuring the smooth operation of the motor.

The UVW module receives a 16-bit binary angle value as input, whose direction can be set through `U.DIR`. The input angle can also be offset through `U.OFS` to correct the output waveform. The polarity of the output signals u, v, and w can be controlled via `U.POL`.

Figure 15 shows the ideal waveform of UVW output signals during the rotation of a single pole pair rotor. The duty cycle and phase shift of the signals have a significant impact on motor performance.

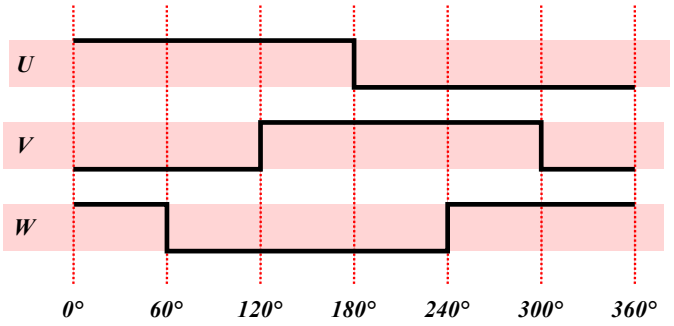


Figure 15: UVW Output Waveform during the Rotation of a Single Pole Pair Rotor

For motors with a different number of pole pairs, the UVW signal output mode needs to be adjusted accordingly. As shown in Figure 16, the output waveform for a two-pole pair (four-pole) rotor is distinctly different from that of a single pole pair. This difference is crucial for the motor control system, as it allows for more precise control and adjustment.

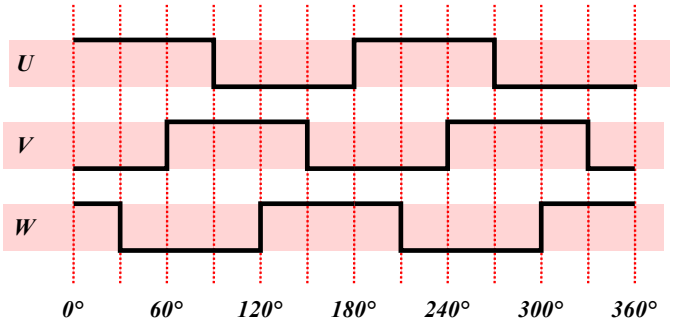


Figure 16: UVW Output Waveform during the Rotation of a Two Pole Pair Rotor

KTM5900 series chips accommodate motors with different numbers of

pole pairs by setting the U.PPT register, allowing for software-based subdivision of commutation steps, thereby generating the required multiple UVW cycles for every 360° rotation. This is crucial for various motor designs, ensuring the versatility of the chip's application.

	MSB							LSB
0x100						U.POL	U.DIR	U.ENA
	7	6	5	4	3	2	1	0
0x101	U.PPT[7:0]							
	7	6	5	4	3	2	1	0
0x102	A.OFS[7:0]							
0x103	A.OFS[15:8]							
	7	6	5	4	3	2	1	0

Table 20: UVW Control Register Table

Here are detailed explanations of the control registers for UVW output signals:

ctrREG	U.ENA

UVW Enable Parameter

When this register is set to 1, the UVW module is activated; when set to 0, the module is turned off. Only when this register is set to 0 can the UVW-related registers below be changed.

ctrREG	U.DIR

UVW Direction Parameter

This register controls the sign of the angle input, thereby determining the rotation direction of the motor. A binary value of 1 represents the positive direction, and 0 represents the reverse direction.

ctrREG	U.POL

UVW Polarity Parameter

The U.POL setting controls the level direction of the output signal to meet the requirements of different types of motors. When set to 1, the output is of positive polarity; when set to 0, it is of negative polarity.

ctrREG	U.OFS [15:0]

UVW Offset Parameter

This register is used to fine-tune the phase of the UVW signal to optimize motor performance. Slight adjustments to the input angle allow for precise control of motor speed and position.

UVW Pole Pair Parameter

The [2:0] bits of U.PPT are used to set the number of pole pairs of the chip, enabling the KTM5900 chip to support motors with different numbers of pole pairs through software configuration.

$$\text{Actual Number of Pole Pairs} = unsigned(\text{U.PPT}) + 1 \tag{8}$$

This flexibility is crucial for adapting to various motor specifications, ensuring that the output signals match the actual needs of the motor, thereby achieving efficient and precise motor control.

With the configuration of these registers, the KTM5900 chip provides a powerful tool for implementing complex motor control strategies. Whether in low-speed or high-speed, simple or complex motor applications, precise UVW signal output ensures the optimization of motor performance.

12 Overall System Configuration (TOP)

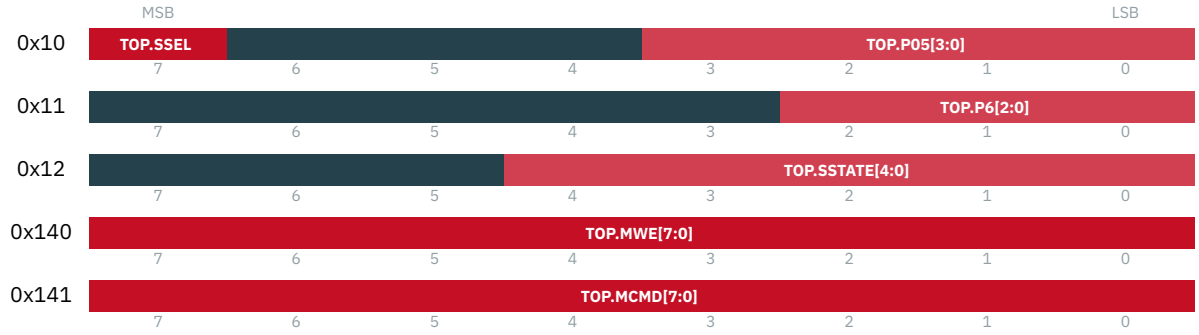


Table 21: Overall System Configuration ctrERG Section TOP

12.1 Chip and Magnetic Sensor Connection Settings

Sensor Selection Parameter

KTM5900 is designed with flexibility, supporting connections to both AMR (Anisotropic MagnetoResistance) and TMR (Tunnel MagnetoResistance) sensors. These two types of sensors differ in their physical properties. In particular, AMR sensors can only output the absolute value of the magnetic field strength and do not provide information on the direction of the magnetic field. In contrast, TMR sensors can provide information on the direction of the magnetic field. Therefore, users need to set the TOP.SSEL parameter to inform the KTM5900 chip whether an AMR sensor or a TMR sensor is being used.

0 = TMR sensor; 1 = AMR sensor.

12.2 Parallel Output Pin Configuration P0 to P6

KTM5900 includes 7 parallel output ports, from P0 to P6. These ports are highly flexible and configurable, capable of outputting a variety of signals such as a, b, z, u, v, w, and clock signals. The specific signal selection depends on the configuration of TOP.P05 and TOP.P6.

ctrREG	TOP.P05 [3:0]

IO Mode Setting

TOP.P05 is used to configure the behavior of P0 to P5. The following table shows the functionality of each pin under different configurations:

TOP.P05	P5 P4 P3	P2 P1 P0
0000	HiZ	HiZ
0001	HiZ	+a b z
0010	HiZ	+u v w
0100	+a b z	HiZ
0101	+a b z	-a b z
0110	+a b z	+u v w
1000	+u v w	HiZ
1001	+u v w	+a b z
1010	+u v w	-u v w

ctrREG	TOP.P6 [2:0]

P6 Pin Function Selection

P6 pin function selection, which can be configured as input or output. The following table shows the functionality of P6 under different configurations:

TOP.P6	Input/Output	P6
000/other	None	Z
001	Output	`pwm`
100	Input	Calibration trigger signal `calibration`
101	Input	Zero signal `zero`
110	Output	Chip internal clock `sysclk`

Current startup state machine status, used for debugging. After power-up, only when this register is 15 does it indicate that KTM5900 has started successfully.

12.3 MTP Read/Write Control

MTP lock register. Write 0xc5 to unlock the MTP command register. Reading returns whether the MTP command register is writable.

TOP.MCMD is the MTP command register.

- 0x0 - IDLE
- 0x2 - Write Configuration (All registers changed by the user will be written to MTP for saving, they won't be lost when power is turned off)

13 Alarms and Detection (IRQ)

Table 22: Alarm and Detection Registers (Section IRQ)

Interrupt Pin Configuration

IRQ.OD determines the output method of the interrupt pin. When set to 0, the interrupt pin is a push-pull output, suitable for scenarios requiring strong driving capability. When set to 1, the interrupt pin is an open-drain output, suitable for scenarios where multiple outputs need to be connected on the same line, such as sharing interrupt signals among multiple devices.

Alarm Status

In the IRQ module, the IRQ.STA register plays a crucial role in latching and clearing specific alarm states. This register contains multiple bits, each representing a specific state or error in the system. Here are detailed explanations of these bits:

AMR Input Sine/Cosine Amplitude Anomaly

IRQ.STA[2]=`alampAmp`

When the amplitude of the sine or cosine signal input from the AMR sensor is too low or too high, this bit will be set. This may be due to sensor damage, signal path interference, or configuration errors.

tmrMisMatch - TMR Input Mismatch

IRQ.STA[6]: Indicates that the TMR0 and TMR1 timer inputs are inconsistent with the sine/cosine signal input from the AMR sensor, possibly due to signal asynchrony, clock errors, or other hardware issues.

filterDelay - Excessive Filter Lag

IRQ.STA[7]: This bit will be set when the response lag of the filter exceeds the set normal range, usually indicating improper filter configuration or insufficient processing capacity.

abzLimit - ABZ Output Limit

IRQ.STA[8]: If the output speed of the ABZ encoder exceeds the system's processing capacity or preset safety limits (A.ABL), this bit will be set, usually indicating system performance issues or potential hardware failure.

abzFatal - Severe ABZ Output Lag

IRQ.STA[9]: When the lag of the ABZ encoder output exceeds 180 degrees, this bit is set, indicating that position data may be inaccurate or lost, usually due to serious faults in the encoder or driving circuit.

crcFail - SPI CRC Decoding Error

IRQ.STA[10]: The setting of this bit indicates an error in the CRC check of data received via SPI communication, possibly due to transmission errors, signal interference, or hardware failures.

mtp1bit - MTP Single Bit Error Detected

IRQ.STA[11]: This bit is set when a 1-bit error is detected by the MTP (Multi-Times Programmable Memory), possibly due to memory damage, programming errors, or hardware faults.

uvderVol - Undervoltage Detected

IRQ.STA[12]: This bit is set when a voltage lower than the normal operating range is detected, possibly due to unstable power supply, power adapter failure, or system circuit issues.

overVol - Overvoltage Detected

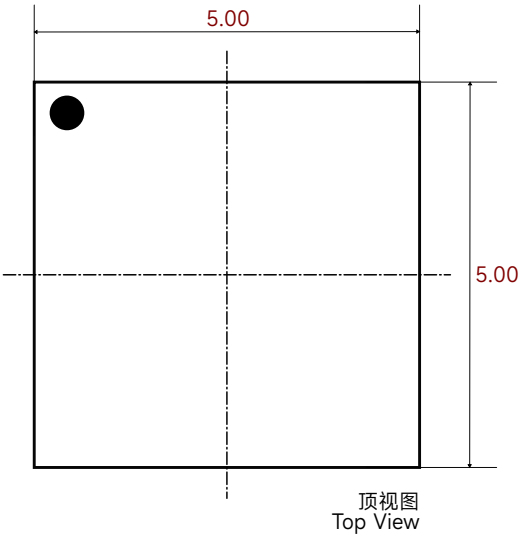
IRQ.STA[13]: When the system detects a voltage exceeding the safe operating range, this bit is set. Excessive voltage can cause system damage or unstable operation and usually requires immediate inspection of the power supply and circuit.

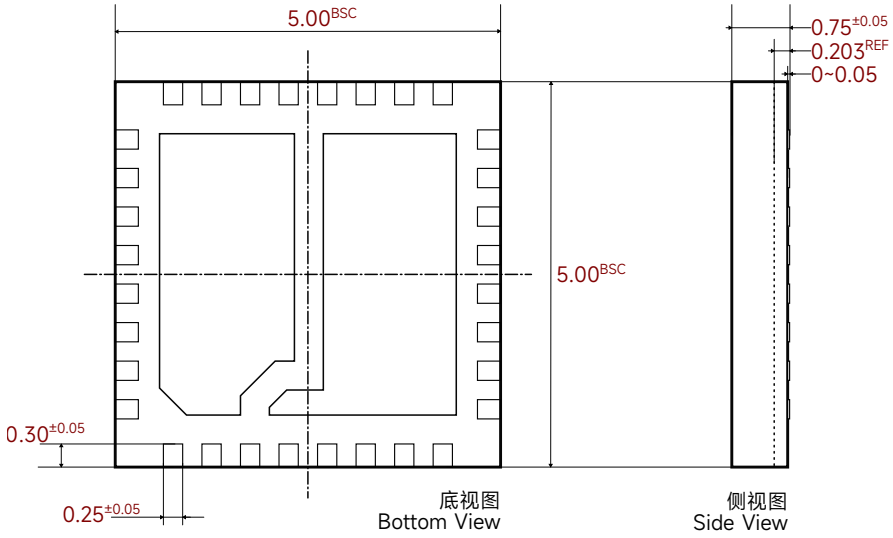
ctrREG	IRQ.SIE [15:0]

Status Interrupt Enable Configuration

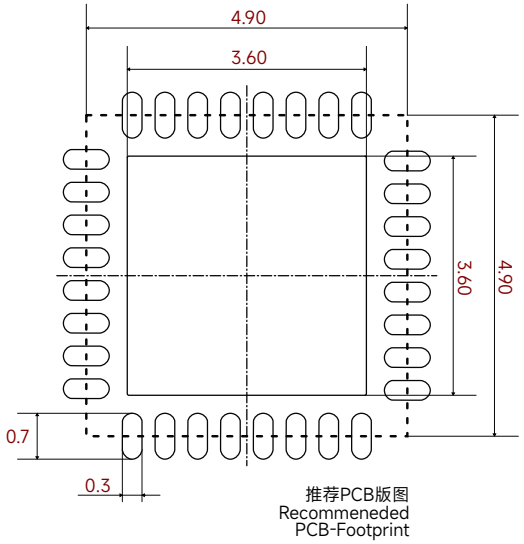
IRQ.SIE allows the system to enable or disable the IRQ PIN foot output alarm function. Corresponds bit by bit with IRQ.STA. For example, if bit13 of IRQ.SIE is set to 1, an alarm will be output by IRQ when overvoltage occurs. If bit13 is 0, no alarm will be output by IRQ for overvoltage.

14 Package Information

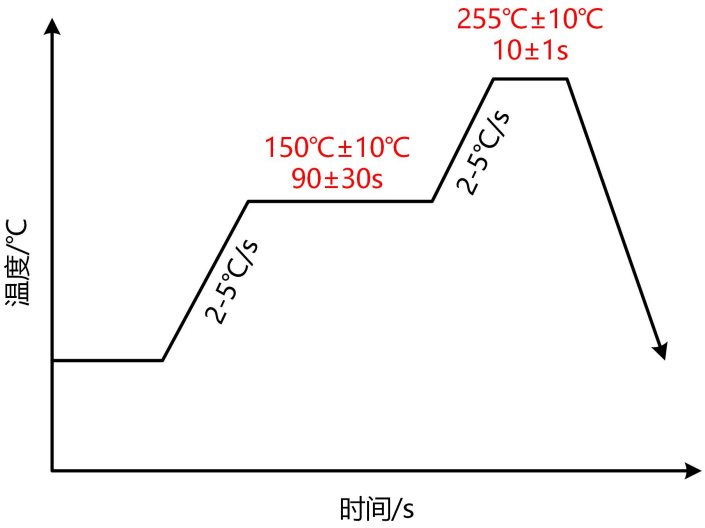




15 Recommended Pad



16 Recommended Soldering Temperature Curve



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