*Click **here** to ask an associate for production status of specific part numbers.*

MAX22216/MAX22217

Quad Smart Serial-Controlled Solenoid and Motor Driver with Advanced Diagnostic

General Description

The MAX22216/MAX22217 integrate four programmable 36V half-bridges. It is primarily intended to drive inductive loads such as on-off solenoid valves, DC motors, proportional valves, bi-stable valves, relays, etc. The MAX22216 is capable of up to $3.2A_{FS}$ per half-bridge, whereas the MAX22217 is capable of up to $1A_{FS}$ per half-bridge. The MAX22216/MAX22217 operate from -40°C to +125°C ambient temperature.

The MAX22216/MAX22217 half-bridges support two different use cases. In the first case, configuration settings can be entered through a serial peripheral interface (SPI) and can be changed at any time. Alternatively, settings can be stored in one-time programmable (OTP) registers, which are loaded at power-up. This enables stand-alone operations. Registers are user-programmable. The OTP writing procedure must be executed in a factory under well-controlled temperature and voltage conditions.

High-side/low-side single-ended drive operations and bridge-tied load (BTL) configurations are supported. Channel parallelization is also supported.

Voltage control, current control, and mixed schemes are supported.

In voltage drive regulation mode (VDR mode), the half-bridge output voltage is controlled. Supply variations are internally compensated.

In current drive regulation mode (CDR mode), the half-bridge output current is controlled. The current is internally sensed and fed back to the controller for accurate closed-loop regulation. Proportional and integral gains can be configured to optimize steady-state errors and dynamic performance.

The MAX22216/MAX22217 integrate functions aimed to optimize solenoid and DC motor drive control. These include a two-level sequencer for power saving, drive signal ramp control (RAMP) for noise reduction, a dither function (DITH) to counteract the effects of static friction and hysteresis, a fast demagnetization feature (DC_H2L) to shorten on-off cycles, and a DC-Motor current limiter for limiting inrush and stall currents.

Advanced diagnostic functions are available to improve system reliability and enable predictive maintenance. These include the detection of plunger movement (DPM), inductance measurement, travel time measurement, open-load detection (OL), and real-time current monitoring through a serial Interface.

The MAX22216/MAX22217 feature a full set of protection circuits, including overcurrent protection (OCP), overtemperature protection (OVT), and undervoltage lockout (UVM). A fault indicator pin is asserted whenever faults are detected.

The MAX22216/MAX22217 are offered in TQFN32 5mm x 5mm packages.

Applications

- Solenoid On-Off Valves and Relays
- DC Motors
- Proportional Valves
- Bi-Stable Latching Solenoid Valves
- Switching Driver with Real-Time Current Measurement
- Digital Output Interface

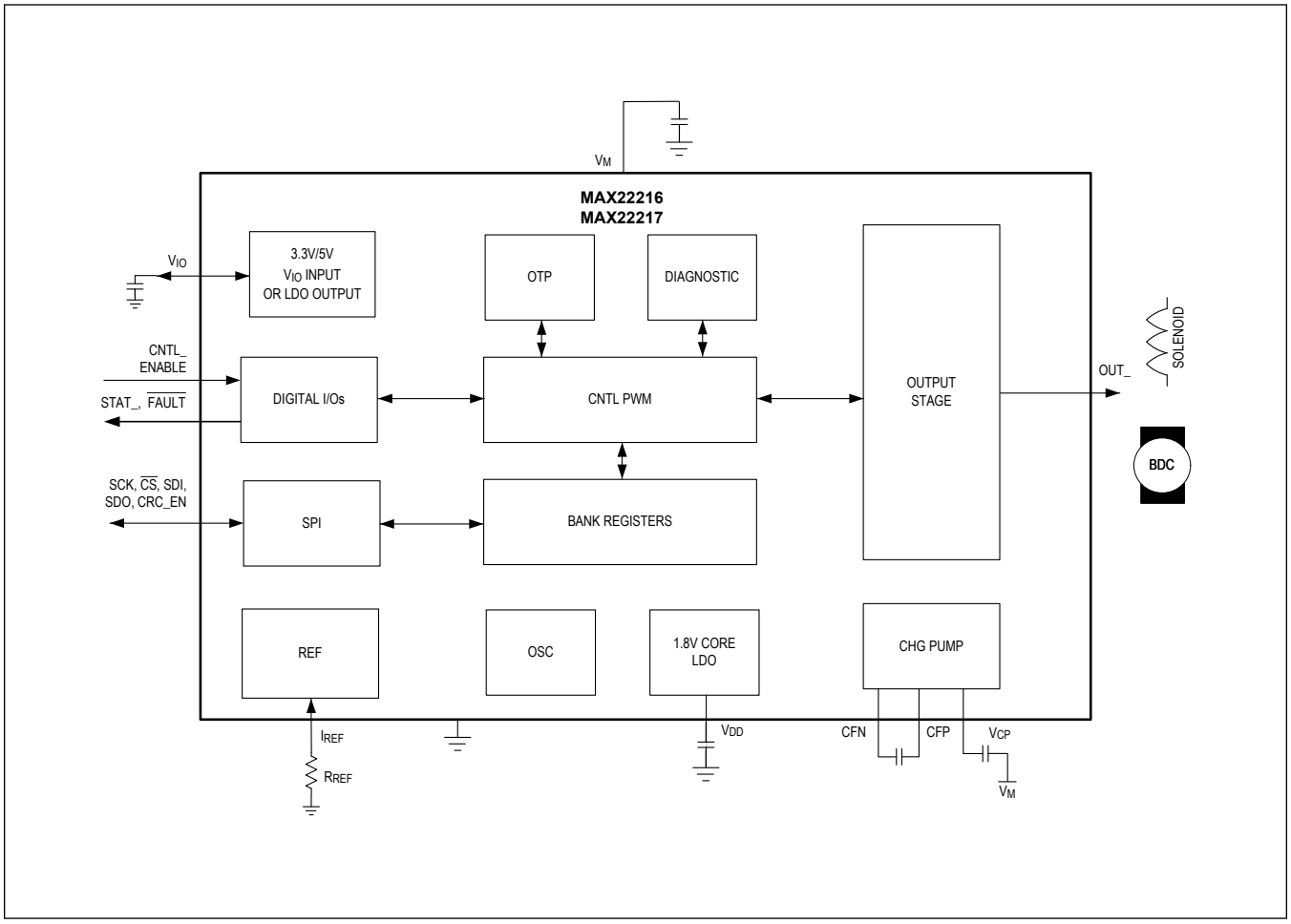
Benefits and Features

- Four Serial Controlled 36V Half Bridges
  - 1.7A DC (T_A = 25°C) and 3.2A Full-Scale Current Capability (MAX22216)
  - 0.55A DC (T_A = 25°C) and 1A Full-Scale Current Capability (MAX22217)
- Low R_{ON} for High Efficiency
- High Flexibility:
  - Independent Channel Setting
  - High-Side/Low-Side/Bridge-Tied Load Configuration/Parallel Mode Supported
- Advanced Control Methods
  - Voltage/Current Drive Regulation
  - Two Levels Sequencer for Power Saving
  - DC-Motor Drive with Current Limiter
  - Dithering Function
  - Ramp up/down Control
  - Demagnetization Voltage Control
  - Integrated Current Sense
- Diagnostic Functions:
  - Reaction and Travel Time Measurement
  - Detection of Plunger Movements
  - Open-Load Detection
  - Inductance Measurement
  - Digital Current Sense Monitor
- Full Set of Protections
  - Overcurrent Protection
  - Thermal Protections
  - Undervoltage Lockout

***Ordering Information** appears at end of data sheet.*

19-101721; Rev 0; 9/23

Simplified Block Diagram



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Absolute Maximum Ratings

V_M to GND ..... -0.3V to +42V
V_{CP} to GND..... V_M - 0.3V to min (+42V, V_M + 6V)
C_{FP} to GND..... V_M - 0.3V to V_{CP} + 0.3V
C_{FN} to GND.....-0.3V to min (+42V, V_M + 0.3V)
CNTL_ to GND .....-0.3V to main (6V, V_{IO} + 0.3V)V
OUT_ to GND ..... -0.3V to V_M + 0.3V
PGND to GND ..... -0.3V to +0.3V
CRC_EN to GND.....-0.3V to min (6V, V_{IO} + 0.3V)V
STAT_ to GND .....-0.3V to V_{IO} + 0.3V
ENABLE to GND ..... -0.3V to V_M + 0.3V
$\overline{CS}$ to GND.....-0.3V to min (6V, V_{IO} + 0.3V)V
SDI to GND.....-0.3V to min (6V, V_{IO} + 0.3V)V
SCK to GND.....-0.3V to min (6V, V_{IO} + 0.3V)V
SDO to GND .....-0.3V to min (6V, V_{IO} + 0.3V)V
V_{DD} to GND ..... -0.3V to min (+2.2, V_M + 0.3)V
V_{IO} to GND .....-0.3V to +6V
$\overline{FAULT}$ to GND.....-0.3V to +6V
I_{REF} to GND.....-0.3V to min (+2.2, V_{DD} + 0.3)V
Continuous Power Dissipation (2s2p Board) (T_A = +70°C, derate 34.5mW/°C above +70°C.) 2758.6mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to 150°C
Lead Temperature (soldering, 10s)..... +300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN 32 - 5mm x 5mm

Package Code	T3255Y+4C
Outline Number	21-100214
Land Pattern Number	90-100082
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	-
Junction to Case (θ_{JC})	-
Thermal Resistance, **Four-Layer Board:**	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_M = 4.5V to 36V, V_{IO} = 2.2V to 5.25V, R_{REF} = 12kΩ, ENABLE = logic high, Typical values assume T_A = 25°C and V_M = 24V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_M		4.5		36	V
Logic Input Supply Voltage	V_{IO}		2.2		5.25	V
Sleep Mode Current consumption	I_{SLEEP}	Enable logic low		4	18	µA

Electrical Characteristics (continued)

(V_M = 4.5V to 36V, V_{IO} = 2.2V to 5.25V, R_{REF} = 12kΩ, ENABLE = logic high, Typical values assume T_A = 25°C and V_M = 24V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Nap Mode Current Consumption	I_{NAP}	Enable logic high, Active = 0			210	450	µA
Quiescent Current Consumption	I_{VM}	Enable logic high, Active = 1			7	9	mA
LOGIC LEVEL INPUTS-OUTPUTS							
Input Voltage Level - High	V_{IH}			0.7 x V_{IO}			V
Input Voltage Level - Low	V_{IL}					0.3 x V_{IO}	V
Input Hysteresis	V_{HYS}				0.15 x V_{IO}		mV
Logic Input Pin Pulldown Resistance	R_{PD}	To GND. Pins CNTL_, SCK, SDI, CRC_EN.		70	100	130	kΩ
$\overline{CS}$ Pin Pullup Resistance	R_{PU}	To V_{IO}		70	100	130	kΩ
Logic-Low Output Voltage	V_{OL}	I_{LOAD} = 5mA, STAT_ and $\overline{FAULT}$ pin				0.4	V
Logic-High Output Voltage	V_{OH}	I_{LOAD} = -5mA		V_{IO} - 0.4			V
Enable Voltage Level High	$V_{IH(EN)}$			0.9			V
Enable Voltage Level Low	$V_{IL(EN)}$					0.6	V
Enable Pulldown Input Resistance	$R_{PD(EN)}$			0.8	1.5		mΩ
OUTPUT SPECIFICATIONS							
Output On-Resistance Low Side	$R_{ON(LS)}$	MAX22216	SNSF[1:0] = "00"		0.17	0.330	Ω
			SNSF[1:0] = "01"		0.23	0.45	
			SNSF[1:0] = "10"		0.43	0.83	
		MAX22217			0.43	0.83	
Output On-Resistance High Side	$R_{ON(HS)}$				0.17	0.33	Ω
Output Leakage	I_{LEAK}	Driver OFF		-5		5	µA
Dead Time	t_{DEAD}				0.1		µs
Slew-Rate Control	SRC	SRC[1:0] = "00"			Fast/No limit		V/µs
		SRC[1:0] = "01"			200		
		SRC[1:0] = "10"			100		
		SRC[1:0] = "11"			50		

Electrical Characteristics (continued)

(V_M = 4.5V to 36V, V_{IO} = 2.2V to 5.25V, R_{REF} = 12kΩ, ENABLE = logic high, Typical values assume T_A = 25°C and V_M = 24V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PROTECTION CIRCUITS							
Overcurrent Protection Threshold	OCP	SNSF[1:0] = "00"		4			A
	t_{OCP}	SNSF[1:0] = "01"		2.5			
	OCP	SNSF[1:0] ="10"		1.2			
Overcurrent Protection Blanking Time	TOCP			1.45	2.1	2.85	µs
UVLO Threshold on V_M	UVLO	Rising		3.75	4	4.25	V
		Falling			3.88	4.12	
Thermal Protection Threshold Temperature	T_{SD}				165		°C
Thermal Protection Temperature Hysteresis	T_{SD_HYST}				20		°C
Open-Load Detection Current	I_{OL_LS}	OL_EN_ = 1	HSnLS = 0, Pulldown current		75	135	µA
	I_{OL_HS}		HSnLS = 1, Pullup current	-50	-22		
Open-Load Detection Voltage	V_{OL_LS}	OL_EN_ = 1	HSnLS = 0		1.7	2.4	V
	V_{OL_HS}		HSnLS = 1	V_M - 2.4	V_M - 1.75		
Open-Load Detect Deglitch Time	t_{OL}			189	200	211	µs
LINEAR REGULATORS / V_{DD} REGULATOR							
V_{DD} Regulator Output Voltage	V_{VDD}	I_{LOAD} = 20mA			1.868		V
V_{DD} Current Limit	$IVDD_{LIM}$			20			mA
LINEAR REGULATORS / V_{IO} REGULATOR - (for Stand-Alone USE CASE)							
V_{IO} Regulator Output Voltage	V_{VIO}	EN_LDO = 1, I_{LOAD} = 10mA	V5nV3 = 1	4.8	5	5.2	V
			V5nV3 = 0	3.15	3.3	3.4	
V_{IO} Current Limit	$IVIO_{LIM}$	Total current. Internal loads account for maximum 10mA		10			mA
CONTROL							
Internal Oscillator Frequency	FCLK			23.7	25	26.3	MHz
PWM Blanking Time	t_{BLK}	SRC[1:0] = "11", T_BLANKING[1:0] = "00"			2.28		µs
	TBLK	SRC[1:0] = "00", T_BLANKING[1:0] = "00"			1.16		
CDR Maximum Full Scale - LS or FB	IFSMAX	MAX22216 GAIN[1:0] = "00" - LS or FB config. (*Note 1*)	SNSF[1:0] = "00"		3.2		A
			SNSF[1:0] = "01"		2.1		
			SNSF[1:0] = "10"		1		

Electrical Characteristics (continued)

(V_M = 4.5V to 36V, V_{IO} = 2.2V to 5.25V, R_{REF} = 12kΩ, ENABLE = logic high, Typical values assume T_A = 25°C and V_M = 24V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CDR Maximum Full Scale - HS	IFSMAX	MAX22216 GAIN[1:0] = "00" - HS config. (Note 1)	SNSF[1:0] = "00"		1.5		A
		MAX22216 GAIN[1:0] = "00" - HS config. (Note 1)	SNSF[1:0] = "01"		1		
			SNSF[1:0] = "10"		0.5		
CDR Maximum Full Scale - LS or FB	IFSMAX	MAX22217 GAIN[1:0] = "00" - LS or FB config. (Note 1)			1		A
CDR Maximum Full Scale - HS	IFSMAX	MAX22217 GAIN[1:0] = "00" - HS config. (Note 1)			0.5		A
CDR Constant	K_{CDR}	MAX22216			1.017		mA
		MAX22217			0.339		
VDR Constant	K_{VDR}				30.518		µV
Resistance Measurement Constant	K_R				8.437		mΩ
REF Pin Resistor Range	R_{REF}	See Note 2			12kΩ ± 5%		kΩ
Supply Voltage (V_M) Monitoring Constant	K_{VM}				9.73		mV
CONTROL / ACCURACY (Note 3)							
Current Control and Monitor - Accuracy	DCDR	MAX22216, GAIN[1:0] = "00"	I_{OUT} ≥ 250mA, SNSF[1:0] = "00"	-5		5	%
			I_{OUT} ≥ 140mA, SNSF[1:0] = "01"	-5		5	
			I_{OUT} ≥ 70mA, SNSF = "10"	-5		5	
		MAX22217, GAIN[1:0] = "00"	I_{OUT} ≥ 70mA	-5		5	
FUNCTIONAL TIMINGS							
Disable Time	t_{DIS}	Enable falling edge to OUT_ tristated				20	µs
Enable Time	t_{EN}	From enable logic high to normal operation (see Note 4 for details)				0.8	ms
Fixed Wake-Up Time	t_{FWU}	From active = 1 to normal operation (excluding user OTP download) - (Note 5)				1.1	ms
Variable Wake-Up Time	t_{VWU}	Time required to download one user-configurable OTP register (2 bytes). (Note 5)			2.56		µs
SPI SPECIFICATIONS							
SCK Clock Period	t_{CLK}	V_{IO} > 3V		100			ns
		V_{IO} < 3V		140			
SCK High Time	t_{CH}			20			ns
SCK Low Time	t_{CL}			20			ns

Electrical Characteristics (continued)

(V_M = 4.5V to 36V, V_{IO} = 2.2V to 5.25V, R_{REF} = 12kΩ, ENABLE = logic high, Typical values assume T_A = 25°C and V_M = 24V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ SCK Valid before or after change of $\overline{CS}$	t_{CC}			20			ns
$\overline{CS}$ Pulse-Width High	t_{CSH}	See also *Note 6*		20			ns
SDI Setup Time before SCK Rising Edge	t_{DS}			10			ns
SDI Hold Time after SCK Rising Edge	t_{DH}			10			ns
SDO Propagation Delay	t_{DO}	C_{LOAD} = 15pF	V_{IO} > 3V			40	ns
			VIO < 3V			75	

Note 1: Recommended "CDR Max full scale" specifies the maximum current at which the device has been characterized and tested. The device can possibly deliver currents higher than IFSMAX, provided that the overcurrent protection and thermal limitations are not exceeded.

Note 2: Current control and monitor accuracy is directly proportional to the accuracy of the resistor connected to the I_{REF} pin. Use ±1% tolerance or better resistors whenever accuracy is required. Accuracy data in this data sheet assumes an ideal REF = 12kΩ resistor.

Note 3: Guaranteed by Bench characterization. Not production tested. R_{REF} = 12kΩ

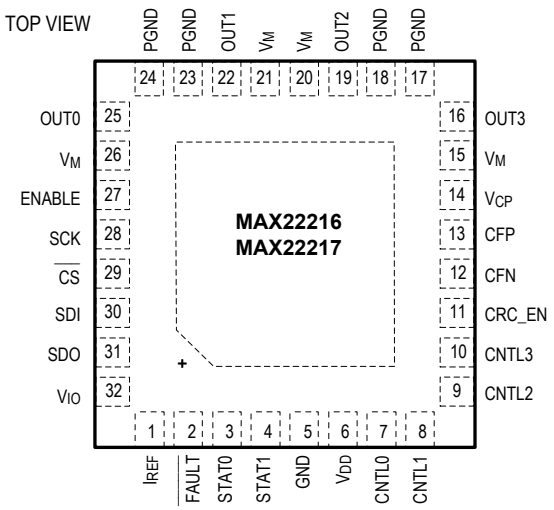
Note 4: The enable command must be held logic high for longer than 0.8ms to ensure the MAX22216/MAX22217 complete its power-up sequence. Commands shorter than 0.8ms can cause the device to enter in unpredictable status.

Note 5: The total wake-up time (t_{WU}) is given by the sum of a fixed (T_{SWU}) and a variable contribute N x T_{VWU} in which N is the total number of user-programmable OTP registers (2 bytes each) written into the OTP bank. (See the *Wake Up time for OTP download at power up* section.)

Note 6: A longer T_{CSH} is required whenever a fault condition needs to be cleared. We recommend longer than 1µs T_{CSH} whenever a fault condition needs to be cleared.

Pin Configuration

MAX22216/MAX22217



TQFN
5mm x 5mm

Pin Description

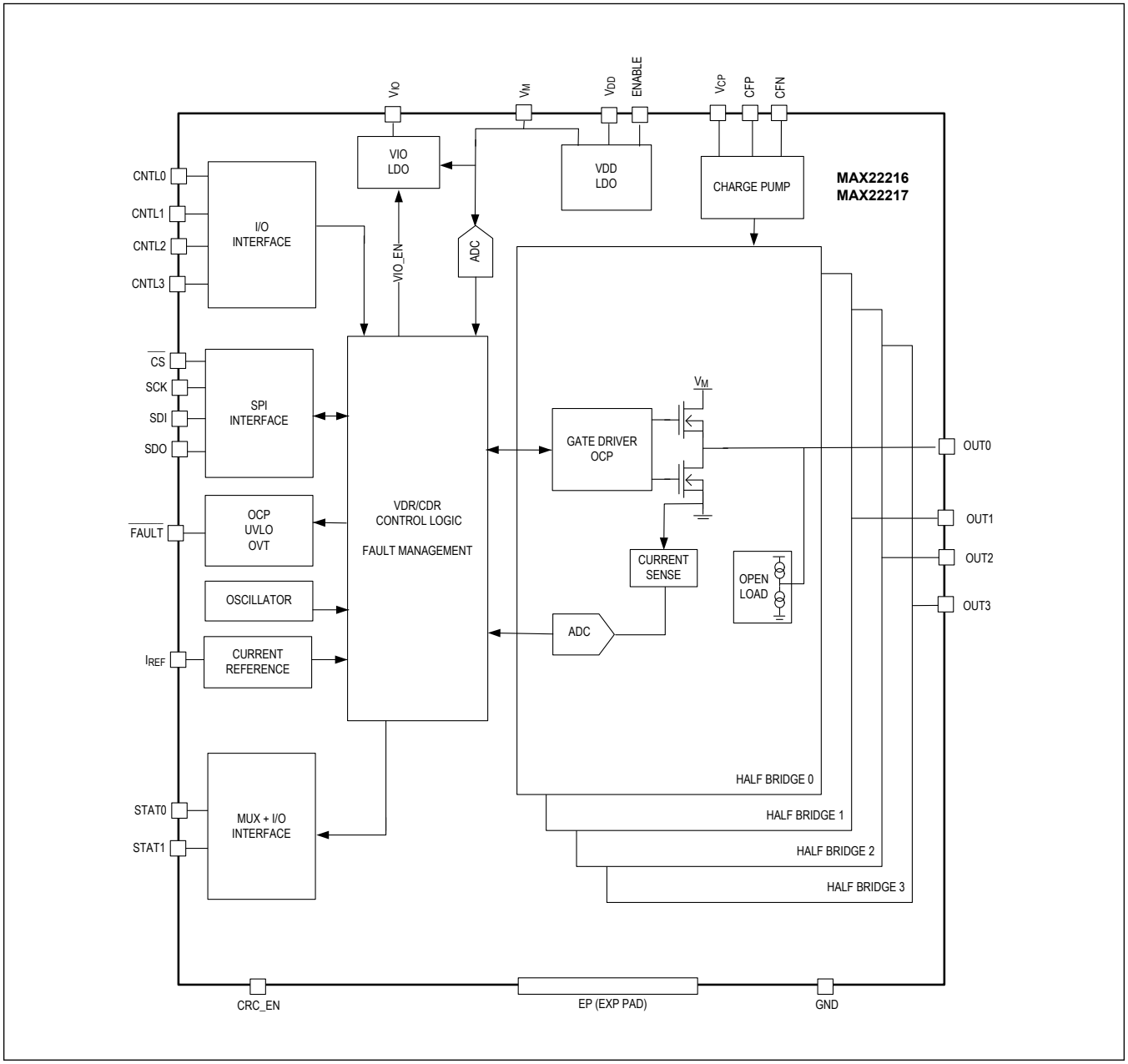
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
15, 20, 21, 26	V_M	Supply Voltage Input. All V_M pins must be shorted on the board. Bypass V_M to GND with 0.1µF local ceramic capacitors close to pins 21, 20 and pins 26, 15. Add electrolytic reservoir tank capacitors as required by the application (typically values >10µF).		Power
32	V_{IO}	I/O Supply Input Voltage Pin if the Internal Linear Regulator is Disabled (EN_LDO = 0 default condition). For SPI-based applications, connect V_{IO} to the external MCU supply voltage for proper communication between the controller and the MAX22216/MAX22217. Bypass V_{IO} to GND with a 100nF or greater capacitor. Voltage regulator output if the internal linear regulator is enabled (EN_LDO = 1). This configuration is used for stand-alone OTP-based applications. The linear regulator output can be configured either at 3.3V or 5V. Connect at least a 0.47µF bypass capacitor to GND to ensure the regulator stability. The maximum external load is 10mA.		
6	V_{DD}	1.8V LDO Regulator Output. Bypass GND with a 2.2µF ceramic capacitor.		Power
12	C_{FN}	Charge Pump Capacitor–N Side. Connect a 22nF, V_M-rated ceramic capacitor from C_{FN} to C_{FP}.		Power
13	C_{FP}	Charge Pump Capacitor–P Side. Connect a 22nF, V_M-rated ceramic capacitor from C_{FN} to C_{FP}.		Power

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
14	V_{CP}	Charge Pump Output. Connect a 1µF, 5V, or greater ceramic capacitor to V_M.		Power
17, 18, 23, 24	PGND	Power Ground. All PGND pins must be shorted on the board.		GND
5	GND	Signal Ground		GND
25	OUT0	Driver Output Channel 0		Output
22	OUT1	Driver Output Channel 1		Output
19	OUT2	Driver Output Channel 2		Output
16	OUT3	Driver Output Channel 3		Output
1	I_{REF}	Current Regulation Reference. Connect a 1% accurate 12kΩ resistor from I_{REF} to GND to set the full-scale current for all the channels in CDR Mode.		Analog Input
29	$\overline{CS}$	SPI Chip Select–Active Low. Internal pullup current.	V_{IO}	Logic Input
28	SCK	SPI Clock Input. Rising edge clocks data into the part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown to GND.	V_{IO}	Logic Input
30	SDI	SPI Data In from Controller. Internal pulldown to GND.	V_{IO}	Logic Input
31	SDO	SPI Data Output.	V_{IO}	Logic Output
7	CNTL0	Control Logic Input. Internal pulldown to GND. To avoid spurious triggering by large noise, it is recommended to connect the pin to GND if not used.	V_{IO}	Logic Input
8	CNTL1	Control Logic Input. Internal pulldown to GND. To avoid spurious triggering by large noise, it is recommended to connect the pin to GND if not used.	V_{IO}	Logic Input
9	CNTL2	Control Logic Input. Internal pulldown to GND. To avoid spurious triggering by large noise, it is recommended to connect the pin to GND if not used.	V_{IO}	Logic Input
10	CNTL3	Control Logic Input. Internal pulldown to GND. To avoid spurious triggering by large noise, it is recommended to connect the pin to GND if not used.	V_{IO}	Logic Input
3	STAT0	Status Logic Output.	V_{IO}	Logic Output
4	STAT1	Status Logic Output.	V_{IO}	Logic Output
11	CRC_EN	Logic Input. Drive CRC_EN logic high to enable cyclic redundancy check on SPI communication. Internal pulldown to GND.	V_{IO}	Logic Input
2	$\overline{FAULT}$	Pulled Logic Low with a Fault Condition. Open-drain output requires an external pullup resistor.		Open Drain Output
27	ENABLE	Enable Pin. HV logic input pin compatible up to V_M. Drive ENABLE logic high to enable device; drive ENABLE logic low to enter low-power sleep mode; Internal pulldown resistor.		Logic Input
—	EP	Exposed Pad. The exposed pad (thermal pad) must be electrically connected to the board GND. For good thermal dissipation, use large ground planes on multiple layers and multiple vias connecting those planes.		GND

Functional Diagrams

Functional Diagram



Detailed Description

The MAX22216/MAX22217 integrate four programmable 36V Half-Bridges. It is primarily intended to drive inductive loads such as on-off solenoid valves, DC motors, proportional valves, bi-stable valves, relays, etc. The MAX22216 is capable of up to $3.2A_{FS}$ per half-bridge, whereas the MAX22217 is capable of up to $1A_{FS}$ per half-bridge. The MAX22216/MAX22217 operate from -40°C to +125°C ambient temperature.

The MAX22216/MAX22217 half-bridges support two different use cases. In the first case, configuration settings can be entered through a serial peripheral interface (SPI) and can be changed any time. Alternatively, settings can be stored into one-time programmable (OTP) registers, which are loaded at power-up. This enables stand-alone operations. Registers are user-programmable. The OTP writing procedure must be executed in a factory under well-controlled temperature and voltage conditions.

Both high-side and low-side single-ended drive operations are supported to accommodate multiple load requirements.

Pairs of half-bridges can also be configured to drive loads in a bridge-tied load (BTL) configuration. Typical examples are proportional solenoid valves, bi-stable valves, or DC motors.

Since settings are completely independent, different types of loads can be driven simultaneously from the same MAX22216/MAX22217 devices. For instance, two single-ended controlled valves and one bi-stable valve in full-bridge configuration can be driven from the same MAX22216/MAX22217.

Channel parallelization is also supported to increase the current capability. For maximum flexibility, two, three, or all four half-bridges can be connected in parallel, resulting in 2X, 3X, and 4X current capability.

Both voltage and current control schemes are supported together with mixed modes.

In voltage mode, two regulation methods are supported and can be configured independently for each drive channel.

- In VDR_DUTY, the user sets the target duty cycle. In this mode, the actual voltage applied to the load directly depends on the V_M voltage supply.
- In VDR Mode (VDRnVDRDUTY), the user sets the target voltage to the load. An internal circuitry senses the supply voltage and compensates the output duty cycle to get the desired voltage.

In current mode (CDR mode), the output current is controlled. The current is internally sensed and fed back to the controller for accurate closed-loop regulation. Proportional and Integral gains can be configured to optimize steady-state error and dynamic performances. The reference current in CDR mode is determined by the resistor connected to the I_{REF} pin. For this reason, an accurate 12kΩ resistor must be connected between pin I_{REF} and GND.

The MAX22216/MAX22217 integrate functions aimed at optimizing solenoid and DC motor drive control, such as:

- Multi-level drive control method (excitation and hold drive with programmable excitation time), resulting in power savings and optimal drive of solenoid valves.
- Programmable voltage/current ramps (RAMP) smooth the activation/deactivation of the valves and hence reduce acoustic noise.
- Programmable dither (DITH) to counteract the effects of stiction and hysteresis by superimposing a small ripple over the DC level.
- A DC motor controller in which the motor is driven in voltage drive mode, the inrush and stall current being limited by an internal limiter circuit.
- A programmable demagnetization voltage (DC_H2L) to ensure accurate and safe control of the demagnetization current (BTL configuration only).

Advanced diagnostic functions are also available to improve system reliability and enable predictive maintenance. In particular, the device features:

- Detection of plunger movement (DPM) aims to detect the movement of the plunger during the excitation phase and report a fault if the plunger gets stuck.
- An inductance measurement circuitry that can be used to detect the status of ON/OFF solenoid valves.
- Reaction time and travel time measurements for diagnostic and predictive maintenance.
- Open-load detection (OL).
- Real-time current monitoring through serial interface (SPI).

Finally, the MAX22216/MAX22217 feature a full set of protections, including overcurrent protection (OCP),

overtemperature protection (OVT), and undervoltage lockout (UVM). Whenever the fault is detected and if it is not masked, the fault indicator pin is asserted, and fault information is logged into a dedicated register.

OPERATING MODES OVERVIEW

Single-Ended Operation

In this configuration, the load is driven in single-ended mode, with the other terminal connected to the positive rail (low-side drive configuration) or to GND (high-side configuration).

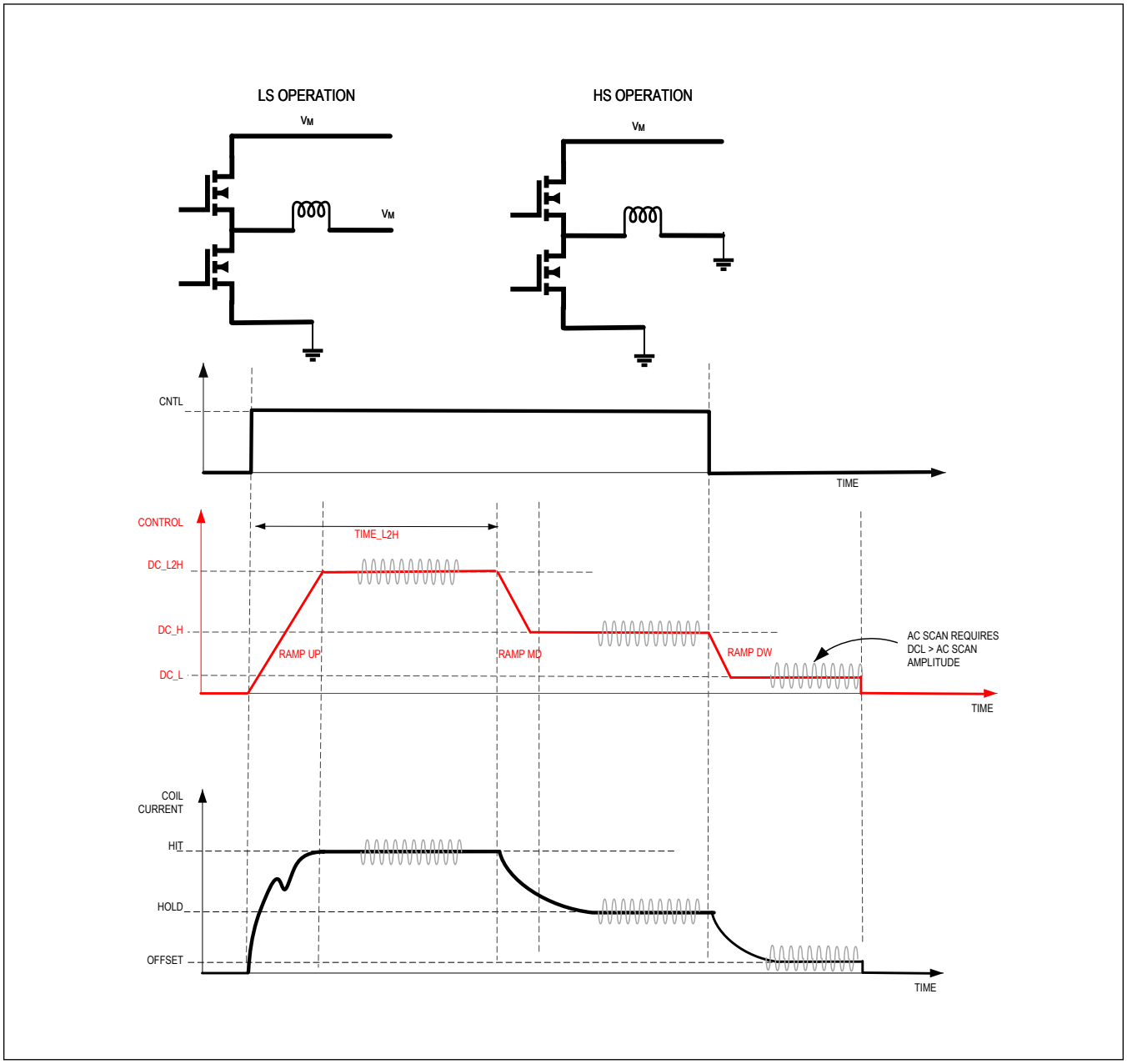


Figure 1. Single-Ended Configuration

Figure 1 shows a typical multilevel drive sequence in single-ended mode. The CNTL signal (namely either the logic input or the corresponding bit in the control register) activates/deactivates the solenoid as shown in Figure 1.

The following parameters are user configurable either with SPI (SPI-based use case) or with OTPs (Stand-alone use case) (see the Register Map section).

Low-Side/High-Side Drive Settings

- Excitation High Level: **DC_L2H[15:0]**
- Hold Level: **DC_H[15:0]**
- Low Level: **DC_L[15:0]** Low-level voltage setting is mainly intended for inductance measurement (AC scan)
- Excitation Time: **TIME_L2H[15:0]**
- Energizing/de-energizing Ramp slope: **RAMP[7:0]**
- AC Scan/Dither Amplitude and Frequency (**U_AC_SCAN[14:0] and F_AC_SCAN[11:0]** global for all the channels)

DC levels settings may refer to voltages, duty cycles, or currents, depending on the desired control strategy. Mixed modes (for instance, DC_L2H in voltage mode and DC_H in current mode) are supported too.

Bridge-Tied Load Operation (Full Bridge)

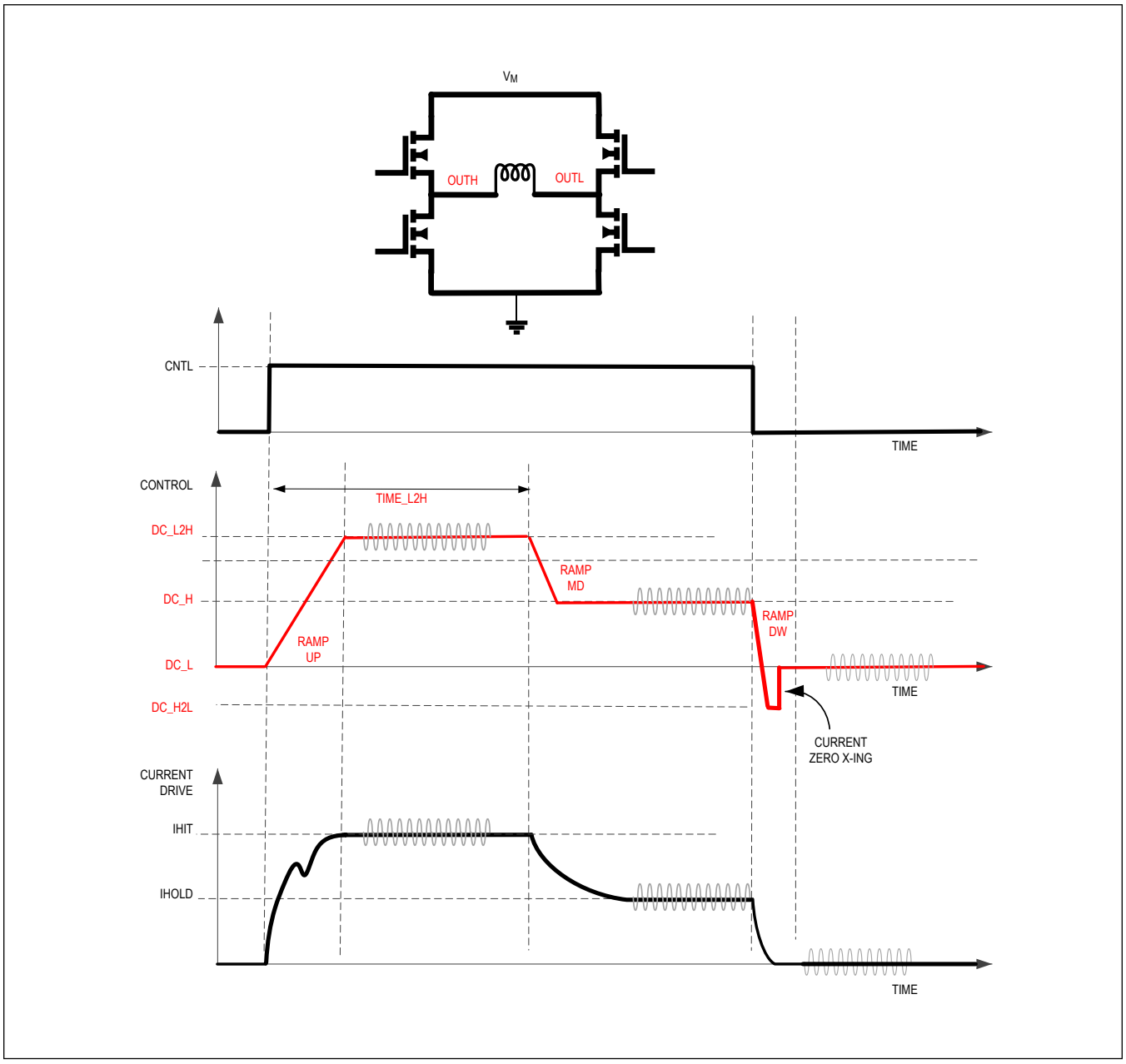


Figure 2. Bridge-Tied Load Configuration

Figure 2 shows a typical multilevel drive sequence for a bridge-tied load solenoid (Bi-stable valves, proportional valves, etc.). The CNTL signal (namely the logic input or the corresponding bit in the control register) activates/deactivates the solenoid as shown in Figure 2.

The following parameters are user configurable either with SPI (a SPI-based use case) or with OTPs (a stand-alone use case) (see the Register Map section).

Bridge-Tied Load Drive Settings

- Excitation High Level: **DC_L2H[15:0]**
- Hold Level: **DC_H[15:0]**
- Demagnetization Voltage: **DC_H2L[15:0]**. It allows to demagnetize the coil by reverting the drive voltage. To avoid inverting the current, DC_H2L is automatically de-asserted once the coil current approaches zero. DC_H2L is global for all the channels.
- Low Level: **DC_L[15:0]** Low-level voltage (normally set to zero)
- Excitation Time: **TIME_L2H[15:0]**
- Energizing/de-energizing Ramp Slope: **RAMP[7:0]**
- AC Scan/Dither Amplitude and Frequency: (**U_AC_SCAN[14:0] and F_AC_SCAN[11:0])** global for all the channels.

With the exception of the demagnetization level (DC_H2L)l, which is programmable in voltage mode only, all the DC level settings may refer to voltages, duty cycles, or currents depending on the desired control strategy. Mixed modes (for instance, DC_L2H in voltage mode and DC_H in current mode) are supported too.

DC Motor Drive

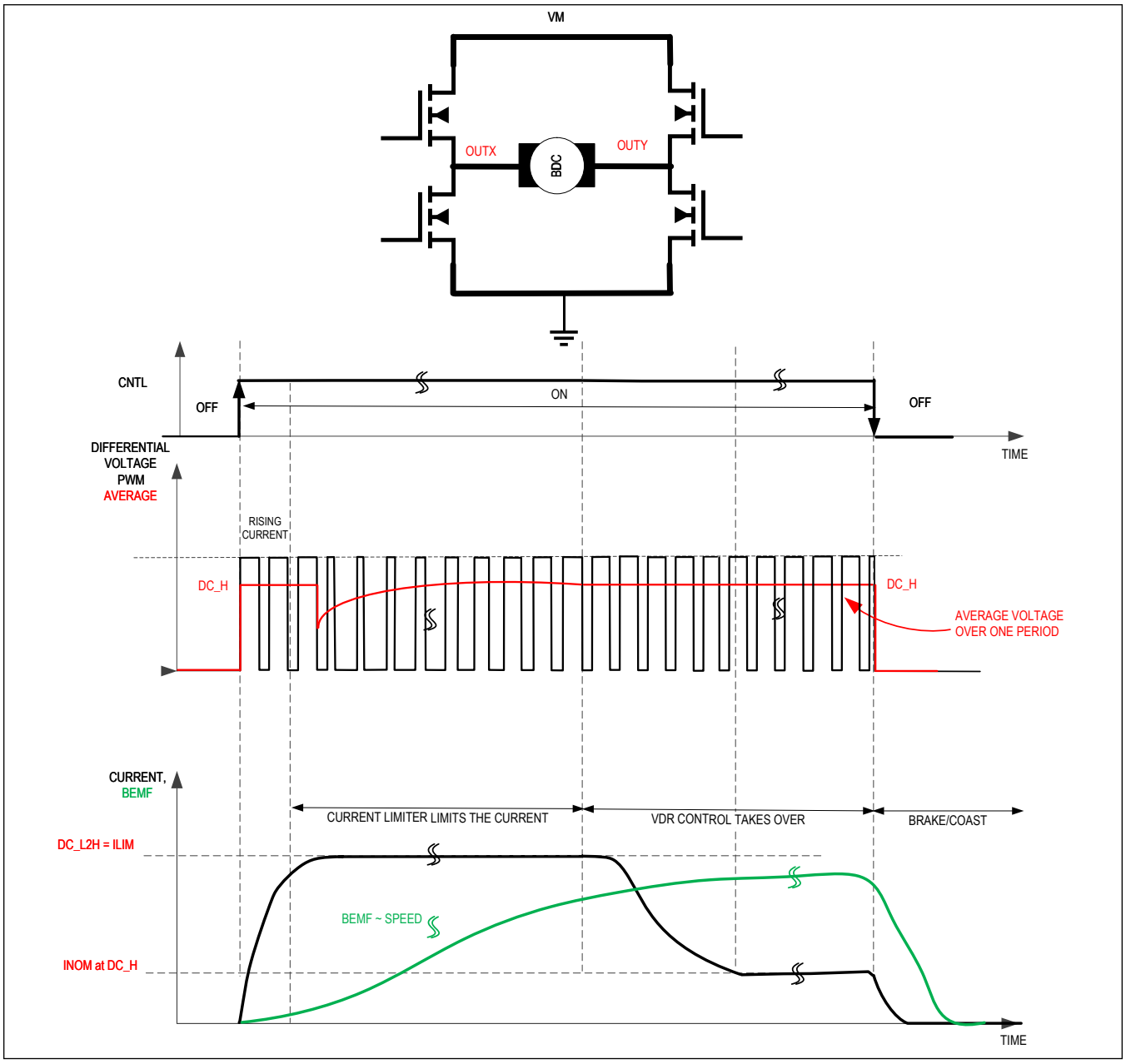


Figure 3. DC Motor

Figure 3 shows the MAX22216/MAX22217 drive signals with reference to a bidirectional DC motor use case (similar drive methods can be implemented for a unidirectional DC motor drive). When the CNTL signal is applied (either from the logic input or via SPI), the controller applies the nominal voltage levels (DC_H) first. If the inrush current during start-up exceeds the programmable current limiter threshold (DC_L2H), the current limiter takes over by reducing the PWM output voltage and effectively limiting the inrush current to a safe level. At the nominal speed of the motor, the BEMF limits the current so that the nominal voltage (DC_H) is automatically applied.

Note that the current limiter is always enabled. In particular, whenever a stall occurs, the limiter limits the stall current to a safe value for the motor and the driver. Once the current exceeds the current limit defined by the DC_L2H register, the loop reduces the voltage applied to the motor, effectively limiting the current to the desired safe value.

The following parameters are user configurable:

Brushed DC Motor Settings

- DC Motor Drive Mode: **CTRL_MODE[1:0] = 10**
- Current Limiter Threshold: **DC_L2H[15:0]**
- Drive Voltage Level: DC_H[15:0]
- Brake Current Level: **TIME_L2H**[15:0]

The MAX22216/MAX22217 feature a current limiter for the motor brake current. This function enables the fastest deceleration of the motor given the overcurrent protection limitations of the device. See the *Brake Current Limiter Function* section for further details. Due to the way the output PWM is created, the actual output frequency is double the set F_PWM. Also, the sine wave generator affects this operating mode only by adding noise at the HiZ state.

DC motor drive can also be used in single-ended mode, but the output will be affected by the CDRs MIN_T_ON (LS will have a minimum voltage and HS will have a maximum voltage), and the BRAKE is not functional.

FUNCTIONAL DESCRIPTION

MAX22216/MAX22217 SPI or OTP Configuration

As shown in the *OPERATING MODES* section, the MAX22216/MAX22217 is a highly configurable device that supports different applications and use cases.

The configuration settings can be input into the MAX22216/MAX22217 in two different ways: through SPI-configuration or through OTP-configuration.

In SPI-configuration, volatile registers must be written through a serial peripheral interface (SPI) after power up.

In OTP-configuration, the user writes one-time programmable (OTP) registers whose content is used as the default configuration setting at power-up. OTP writing must be done in a controlled test setup in the factory. When OTP-configuration is used, the MAX22216/MAX22217 can operate in stand-alone mode with minimal control signals from outside.

Further details are available in the *HOW TO CONFIGURE THE MAX22216/MAX22217* section.

Enable Logic Input (ENABLE)

The enable pin is a V_M-rated logic input pin.

Drive the ENABLE logic low to disable the device. This corresponds status to the lowest power consumption for the device.

Drive the ENABLE logic high to enable the device. When enabled, the ENABLE pin must be held high for at least TEN to complete the power-up sequence and prevent the MAX22216/MAX22217 from entering unpredictable statuses.

A pulldown resistor ensures the MAX22216/MAX22217 is disabled if the Enable pin is not actively driven.

In stand-alone operating mode, the ENABLE pin can possibly be externally connected to the positive rail (V_M). This way, the solenoid valve can be activated/deactivated by simply powering up/down the device (see the *V_M Switching Stand-Alone* section).

Nap Mode and ACTIVE Bit

The ACTIVE bit in the GLOBAL_CFG register activates/deactivates the MAX22216/MAX22217. When ACTIVE = "0" and ENABLE is logic high, the device is in Nap Mode. Power consumption is minimized (see the *Electrical Characteristics* table), the sequencer is disabled, and driver outputs are tri-stated. In SPI-based applications, this corresponds to the default condition at power-up. To enter in normal operation, the ACTIVE bit must be set after the device configuration.

In an OTP-based application, this bit must be programmed high to enable stand-alone operations.

V_{IO} Pin Description (V_{IO})

The V_{IO} voltage is the reference for logic Inputs and output signals. The V_{IO} pin can be configured by writing two bits in the STATUS_CFG[15:0] register.

EN_LDO is the enable bit of the internal regulator.

If EN_LDO = "0" (default), the V_{IO} must be provided from the outside, and V_{IO} is a supply voltage input pin.

If EN_LDO = "1", then an internal linear regulator is turned on and the V_{IO} pin becomes an output (settable at 3.3V or 5V).

In SPI-based applications, the V_{IO} pin is normally configured as an input and connected to the voltage supply of the external controller to enable communication between the MAX22216/MAX22217 and the controller.

In OTP-based applications (stand-alone mode) in which the SPI is not used and wiring must be minimized, the internal linear regulator can be enabled to supply the internal I/O circuitry. The regulator output voltage can be set either at 3.3V or 5V, depending on the selection of the V5_nV3 bit. The regulator can only be activated via the OTP programming functionality and is available after a reboot of the part.

CNTL Pin and CNTL Bits

As shown in *OPERATING MODES OVERVIEW*, a change of the status of the CNTL pin or of the CNTL bit in the STATUS register initiates and ends the sequence (with the exception of the V_M switching stand-alone control, in which the supply voltage itself is used as a command signal; see the *V_M Switching Stand-Alone* section).

The polarity of the CNTL pin can be changed with the CNTL_POL bit in the GLOBAL_CFG configuration register, this does not affect the polarity of the CNTL bits. Set CNTL_POL = "0" for positive polarity (CNTL is active high). Set CNT_POL = "1" for negative polarity (CNTL is active low). In the special case of using CNT_POL = "1" together with a full-bridge configuration, the CNTL pins will not change polarity, but they will change the control channel. For example, the CNTL0 pin will control CH1 output, and the CNTL1 pin will control CH0. The same applies for CH2 and CH3 pairs. As this setting affects only the CNTL pins, all the other settings are the same.

CNTL bit in the STATUS register and CNTL pins are in or-ing configuration. If either the bit or the input signal is active, then the sequencer is enabled. This also means that once the channel is active using one method, it cannot be turned off using the other control method. If the MAX22216/MAX22217 are controlled via SPI, then the CNTL pins must be set as inactive (it is recommended to connect CNTL logic pins to GND to prevent spurious triggering by noise).

Vice versa, if the MAX22216/MAX22217 are controlled only via logic inputs CNTL, then the CNTL bits must be set as inactive (default state).

Hardware Configuration

The MAX22216/MAX22217 provide flexibility. The channel hardware configuration bits CHS[3:0] in the GLOBAL_CFG register must be set to match the hardware configuration of the half bridge of the MAX22216/MAX22217.

Maximum current can be increased by using a parallel half- or full-bridge configuration. As there is no connection between the channels inside the IC, it has to be done on the PCB. A pair of channels can also be configured in full-bridge mode to drive the load differentially (bridge-tied load). Table 1 summarizes all possible hardware configurations. (HB = Half Bridge, FB = Full Bridge).

Table 1. Hardware Configuration

CHS	SUPPORTED CONFIGURATIONS	HARDWARE SETTINGS
0x0	4x Independent half-bridges (HB)	OUT0, OUT1, OUT2, OUT3
0x1	3x Parallel HBs + 1x Independent HB	OUT0 = OUT1 = OUT2, OUT3
0x2	2x Parallel HBs + 2x Independent HBs	OUT0 = OUT1, OUT2, OUT3
0x3	2x Parallel HBs + 2x Parallel HBs	OUT0 = OUT1, OUT2 = OUT3
0x4	4x Parallel HBs	OUT0 = OUT1 = OUT2 = OUT3
0x5	2x Independent Full Bridges (FB)	OUT0 vs OUT1, OUT2 vs OUT3
0x6	1x Independent FB + 2x Independent HBs	OUT0 vs OUT1, OUT2, OUT3
0x7	1x Independent FB + 2x Parallel HB	OUT0 vs OUT1, OUT2 = OUT3

Table 1. Hardware Configuration (continued)

0x8	1x Parallel FB	OUT0 = OUT1 vs OUT2 = OUT3

When channels are parallelized, the MAX22216/MAX22217 uses the configuration settings of the channel with a lower channel index. For instance, for the configuration 0x3 in Table 1, the configuration settings of channel “0” and channel “2” control the parallelized half bridges, whereas the configuration settings of channel “1” and channel “3” are ignored.

Table 2 and Table 3 summarize the active control registers (CFG_) and the active command signal (CNTL_) for each Hardware Configuration. The configuration registers store all the parameters that are used by the sequencer (see the *OPERATING MODES* section), plus other configuration parameters explained in the following paragraphs. Each CFG is controlled by the specific CNTL channel (CFG_0 is controlled by CNTL0), and it controls the output based on channel configuration.

The CNTL signals enable (CNTL = 1) or disable (CNTL = 0) the corresponding channels, as shown in Table 2.

The enable/disable signals can be either hardware-based (logic I/Os) or software-based (CNTL bits in the GLOBAL_CTRL register). HW and SW controls are in OR configuration: if either the logic CNTL input or the corresponding bit in the GLOBAL_CTRL register are logic high, then the channel is enabled. It follows that in SW-based control, the logic input pins must be grounded (logic low). Vice versa, for HW-based control, the control bits must be set to zero (default at power up).

In full-bridge operation, a center-aligned PWM chopping method is used so that the effective PWM frequency is doubled and ripple is minimized. With this technique, a zero voltage across the load corresponds to a 50% duty cycle applied on each side of the bridge-tied load. Moreover, the control signals (CNTLx, CNTLy) determine the configuration registers, as shown in Table 3.

Table 2. Control Table

OUTPUT SETTINGS			ACTIVE CONFIGURATION REGISTER/CONTROL CHANNEL			
CHS[3:0]	**OUTPUT CONFIGURATION**		**CH0 OUTPUT**	**CH1 OUTPUT**	**CH2 OUTPUT**	**CH3 OUTPUT**
0x0	4x Independent HB		CFG_0/CNTL0	CFG_1/CNTL1	CFG_2/CNTL2	CFG_3/CNTL3
0x1	3x Parallel HBs	1x Independent HB	CFG_0/CNTL0			CFG_3/CNTL3
0x2	2x Parallel HBs	2x Independent HBs	CFG_0/CNTL0		CFG_2/CNTL2	CFG_3/CNTL3
0x3	2x Parallel HBs	2x Parallel HBs	CFG_0/CNTL0		CFG_2/CNTL2	
0x4	4x Parallel HBs		CFG_0/CNTL0			
0x5	1x Independent FB	1x Independent FB	see Table 3		see Table 3	
0x6	1x Independent FB	2x Independent HBs	see Table 3		CFG_2/CNTL2	CFG_3/CNTL3
0x7	1x Independent FB	2x Parallel HB	see Table 3		CFG_2 / CNTL2	
0x8	1x Parallel FB		see Table 3			

Table 3. Full-Bridge Control

CHS[3:0]	**BRIDGE CFG**	**CNTLx**	**CNTLy**	**OUTx**	**OUTy**	**FB Status**
0 x 05	OUTx vs OUTy (x, y) = (0,1) or (2, 3)	0	0	HiZ	HiZ	HiZ
		1	0	CFG_x		DRIVEN by CH X
		0	1	CFG_y		DRIVEN by CH Y
		1	1	50% PWM	50% PWM	BRAKE
CHS[3:0]	**BRIDGE CFG**	**CNTL0**	**CNTL1**	**OUT0**	**OUT1**	**FB Status**
0 x 06 or 0 x 07	OUT0 vs OUT1	0	0	HiZ	HiZ	HiZ
		1	0	CFG_0		DRIVEN by CH 0
		0	1	CFG_1		DRIVEN by CH 1
		1	1	50% PWM	50% PWM	BRAKE
CHS[3:0]	**BRIDGE CFG**	**CNTL0**	**CNTL1**	**OUT0 = OUT1**	**OUT2 = OUT3**	**FB Status**

Table 3. Full-Bridge Control (continued)

0 x 08	OUT0 = OUT1 vs OUT2 = OUT3	0	0	HiZ	HiZ	HiZ
		1	0	CFG_0		DRIVEN by CH 0
		0	1	CFG_1		DRIVEN by CH 1
		1	1	50% PWM	50% PWM	BRAKE

HS or LS Single-Ended Configuration

In single-ended mode, the MAX22216/MAX22217 can be configured as an HS driver (load is connected between OUT and GND) or as an LS driver (load is connected between OUT and V_M). The selection bit HSnLS can be written in the CFG_CTRL[15:0] register. Set HSnLS = "1" for the HS operation. Set HSnLS = "0" for the LS operation.

Chopping Frequency and Timebase Configuration

The MAX22216/MAX22217 feature an integrated oscillator that sets the time base of the device and determines the chopping frequency, F_{PWM}.

F_PWM_M[3:0] bits in the GLOBAL_CTRL register set the master PWM frequency, as shown in Table 4.

Table 4. PWM Master Frequency Setting

HEX	**0x0**	**0x1**	**0x2**	**0x3**	**0x4**	**0x5**	**0x6**	**0x7**
F_PWM_M	100	80	60	50	40	30	25	20
HEX	**0x8**	**0x9**	**0xA**	**0xB**	**0xC**			
F_PWM_M	15	10	7.5	5	2.5			

Note: 0xD, 0xE, and 0XF are same as 0x0 (100kHz)

The master chopping frequency can be further divided down individually for each half bridge by setting bits F_PWM[1:0] in the configuration register for that specific channel, as shown in Table 5.

Table 5. Individual PWM Frequency

F_PWM[1:0]		**CHOPPING FREQUENCY OF INDIVIDUAL CHANNEL**
0	0	F_PWM_M
0	1	F_PWM_M/2
1	0	F_PWM_M/4
1	1	F_PWM_M/8

The resulting chopping frequency (F_PWM) is also used as a time base for configuring the timings of the sequencer and/or other functions. Generally, if the PWM frequency is not a requirement of the design, it is recommended to use smaller frequencies, such as 25kHz or 10kHz for increased accuracy. If the channels do not have different PWM frequency requirements, the main frequency can be set in F_PWM_M (PWM master frequency) and the individual channel F_PWM can be left to the default setting of 0x00. Frequencies in the audio range (like 10kHz) might create noise in the solenoid coil.

Slew Rate and Blanking Configuration (SRC)

The slew rate of the rising and falling edges can be controlled by means of two configuration bits in the configuration register (SRC[1:0]). Table 6 shows the possible settings.

Slower edges reduce over/undershooting and ringing and are therefore effective in mitigating electro magnetic emission (EME). On the other hand, slow edges result in higher power consumption and worse VDR control accuracy.

Table 6. Slew-Rate Control

SRC[1:0]	**SLEW-RATE CONTROL**
00	Fast
01	200V/µs

Table 6. Slew-Rate Control (continued)

10	100V/µs
11	50V/µs

Current measurements taken just after the falling edges can be inaccurate as they may be affected by electrical noise and ringing occurring after the commutation. The device automatically inserts a blanking time depending on the slew-rate setting (see the *Electrical Characteristics* table). In addition, the user can configure four additional blanking time, as shown in Table 7. The T_BLANKING bits are stored in the CFG_CTRL register. When in CDR modes, long blanking times limit the MIN_TON and hence the duty cycle at a given PWM frequency (see the *Minimum TON Limitations* section).

Table 7. Blanking Time

T_BLANKING_[1:0]	BLANKING TIME (µs)
00	0
01	0.96
10	1.92
11	2.88

SEQUENCER SETTINGS

Setting the Sequencer Control Mode

As shown in the *Operating Modes*, the sequencer can be configured to address different use cases.

The DC_L2H and DC_H levels can be controlled either in voltage mode or current mode. In addition, to better address DC motor drive applications, the DC_H2L can be configured to set the threshold of the current limiter (see the *Bi-directional DC Motor Drive* section).

Two bits in the configuration register of each individual channel allow selecting the desired control mode, as shown in Table 8.

Table 8. Control Mode Setting

CTRL_MODE[1]	CTRL_MODE[0]	DCL2H	DCH	TYPICAL USE CASES
0	0	VDR	VDR	Solenoid drive
0	1	CDR	CDR	Solenoid drive, Proportional valve
1	0	Current limiter	VDR	Brushed DC motor
1	1	VDR	CDR	Solenoid drive, Proportional valve

A third low level (DC_L) can also be programmed individually for each channel, as explained in *Operating Modes*. DC_L can be controlled only in voltage mode (VDR) together with the sine wave generator. This is mostly intended to be used in single mode operations to allow inductance measurement (see the *Inductance Measurement* section).

For full-bridge configuration, it is possible to demagnetize the coil by applying a reverse demagnetization voltage at the end of the excitation phase (see the *Bridge Tied Load Operation (Full Bridge)* section). The demagnetization voltage can be set by writing the global register DC_H2L[15:0] with a negative value and setting H2L_EN for each individual channel. To avoid current inversion, the demagnetization voltage is automatically de-asserted as soon as the current approaches zero.

It is also possible to set the device so that the reverse demagnetization voltage is applied when the coil is energized and the supply drops below a threshold stored into the VM_THLD_DOWN[3:0] bits of the VM_THRESHOLD register (see the Register Map and *V_M Switching Stand-Alone* section for further details). If this function is enabled, as soon as the supply drops below VM_THLD_DOWN, a reverse voltage equal to DC_H2L is applied so that the coil is quickly demagnetized. The reverse voltage is maintained until the current is zeroed. During the demagnetization transitory, the coil current recirculates back to the supply, causing the V_M voltage to be pumped up. Therefore, the bypass capacitor on V_M must be large enough to absorb the coil energy without exceeding the maximum operating voltage.

SEQUENCER LEVEL SETTINGS

Voltage Drive Regulation (VDR)

DC_L2H, DC_H, and DC_L levels can be configured for VDR mode operation by programming the corresponding configuration registers for each individual channel. VDR is supported for high-side drive, low-side drive, and differential drive bridge-tied load (BTL) configurations.

Two alternative voltage control modes can be selected by means of the VDRnVDRDUTY selection bit in the GLOBAL_CFG register:

When VDRDUTY is selected (VDRnVDRDUTY = "0"), the DC_ levels correspond to the target duty cycle. The average output is proportional to the supply (V_M). The average output voltage is therefore given by

$$V_{OUT} = K_{VDR} \times V_M \times DC\_[15:0]_{DEC}$$

Where K_{VDR} is a constant equal to 30.5µ (see the *Electrical Characteristic* table).

When VDR is selected (VDRnVDRDUTY = "1"), the DC_ levels correspond to the target output voltage. Variations of the supply voltage are internally compensated. The average output voltage is given by:

$$V_{OUT} = K_{VDR} \times 36 \times DC\_ [15:0]_{DEC}$$

The voltage control accuracy is affected by several non-idealities that are not internally compensated. In particular, rise and fall edge mismatch and voltage drop on power FETs can have an impact on the VDR accuracy. In general, better performance can be achieved when fast edges and low PWM chopping frequencies are selected.

The internal PWM generator runs at 25MHz, so the actual resolution of the control depends on the programmed PWM chopping frequency. For instance, if channels run at 30kHz, the PWM resolution is 30kHz/25MHz = 0.12%.

The duty cycle control range is limited depending on the programmed chopping frequency, slew rate settings, and blanking time settings. However, the 100% and 0% (always ON and always OFF) statuses are always supported and mapped as DC_[15:0] = 0x7FFF and DC_[15:0] = 0x0000, respectively.

When in full-bridge configuration, the PWM modulator adopts a center-aligned modulation scheme. Both sides of the coil are PWM-modulated.

$$D_{OUTX} = (1 + D)/2,\ D_{OUTY} = (1\text{-}D)/2$$

$$\text{Duty Cycle} = D = D_{OUTX} - D_{OUTY}$$

Where X and Y are the two generic channels driving the load in full-bridge configuration.

This approach results in doubling the ripple frequency and halving the amplitude of the ripple. When VDR or VDRDUTY equals zero, the two channels output a 50% duty cycle.

CURRENT DRIVE REGULATION (CDR)

Current Drive Regulation (CDR)

DC_L2H, DC_H, and DC_L levels can be configured for CDR Mode operation by programming the corresponding 16 bits configuration registers. CDR is supported for single-ended LS and HS drive and differential BTL configurations.

In DC motor drive mode (CTRL_MODE_[1:0] = "10" in the channel configuration register), the DC_L2H stores the threshold at which the current limiter starts limiting the current either during motor start up or under stall conditions.

When the current drive regulation method is used, a proportional Integral controller controls the current at the desired set point. Current is internally sensed onto the low-side power FET without the need of external shunt resistors. The sensing is bidirectional, so that the MAX22216/MAX22217 can measure both sinking currents (LS drive and Full Bridge modes) and sourcing currents (HS drive Configuration Mode). However, in HS mode, the maximum current that can be accurately measured is less than for the LS and full-bridge modes since excessive currents can turn on the FET body drain diode and affect the accuracy of the measurement.

Under steady conditions, the controlled current can be calculated from the following formulas:

MAX22216	$I_{OUT(mA)} = K_{CDR} \times GAIN \times SNSF \times DC\_[15:0]_{DEC}$
MAX22217	$I_{OUT(mA)} = K_{CDR} \times GAIN \times DC\_[15:0]_{DEC}$

Where

- $DC\_[15:0]_{DEC}$ is the target DC current value (in decimal notation) stored in the corresponding register. To avoid

saturation, we recommend not exceeding DC_[15:0]$_{DEC}$ = 3145 for LS and full-bridge configurations and 1475 for HS configurations (Assuming GAIN = SNSF = 1). In other terms, the maximum full-scale current is 3.2A in LS or full-bridge mode, and 1.5A in HS mode. The maximum bit value for the current is based on the channel control configuration and I_MONITOR scaling of each channel. For more detail, see the *Digital Current Monitor Function* section. If the real current value is set too high, the OCP will trigger (as it is independent of the I_MONITOR), or the IC will heat up too much and trigger the OVT. Always set the I_MONITOR range, taking into consideration the maximum current in the configuration.

- K_{CDR} is a constant typically equal to 1.017mA and 0.34mA, respectively, for the MAX22216 and MAX22217. K_{CDR} directly depends on the external 12kΩ reference resistor connected between the I_{REF} pin (see the *Current Reference* section). For accurate current control, a precise resistor must be used.
- GAIN (see Table 9) is a two bits programmable gain factor (GAIN[1:0] bits into the configuration register).
- SNSF (see Table 9 is a two bits programmable Sense Scaling Factor (SNSF[1:0] bits into the Configuration Register). As shown in Table 9, the SNSF value determines the resistance of the low-side power FET (R_{ON}), which is used as a sense element. A higher resistance of the sensing element results in better accuracy of the control at low currents. This function is only available for the MAX22216.

When multiple half- or full-bridges are used in parallel, the maximum digital reading value multiplies independently of the individual channels GAIN or SNSF settings (as the I_MEASUREMENT will become the sum of the individual channel currents); however, the GAIN/SNSF settings apply to all connected channels based on the main configuration channel; see the *Digital Current Monitor Function* section. For a quality reading of the current, it is recommended to set the GAIN and SNSF based on the worst-case maximum current for the application (including temperature increase in current consumption and MOSFET resistances), while using the smallest range possible for better resolution. If the I_MONITOR value overflows, then the Inductance and Resistance measurements become unreliable. Table 9 shows the scaling factors for the current measurement of one channel (maximum digital current value of 4095) and their effects.

Table 9. Full Scale and Sense Scale

GAIN [1:0]	GAIN	SNSF [1:0]	SNSF	TYP. LS R_{ON} (Ω)	TOTAL FACTOR	MULTIPLIER	MAX CURRENT (A)
00	1	00	1	0.17	1	1.00	4.164615
01	3/4				3/4	0.75	3.12346125
10	2/4				2/4	0.50	2.0823075
11	1/4				1/4	0.25	1.04115375
00	1	01	2/3	0.24	2/3	0.67	2.77641
01	3/4				6/12	0.50	2.0823075
10	2/4				4/12	0.33	1.388205
11	1/4				2/12	0.17	0.6941025
00	1	10	1/3	0.44	1/3	0.33	1.388205
01	3/4				3/12	0.25	1.04115375
10	2/4				2/12	0.17	0.6941025
11	1/4				1/12	0.08	0.34705125

PI Controller

The current loop is based on Proportional Integral (PI) control. Proportional and Integral coefficients can be set individually for each channel. PI control results in optimal current control and tunable time response characteristics.

16 bits Register CFG_P[15:0] and CFG_I[15:0] define the control parameters for each channel. The registers define the Proportional Gain (Kp) and Integral Gain (Ki) characteristics in Q8.8 format.

Figure 4 shows the block diagram of the current control loop.

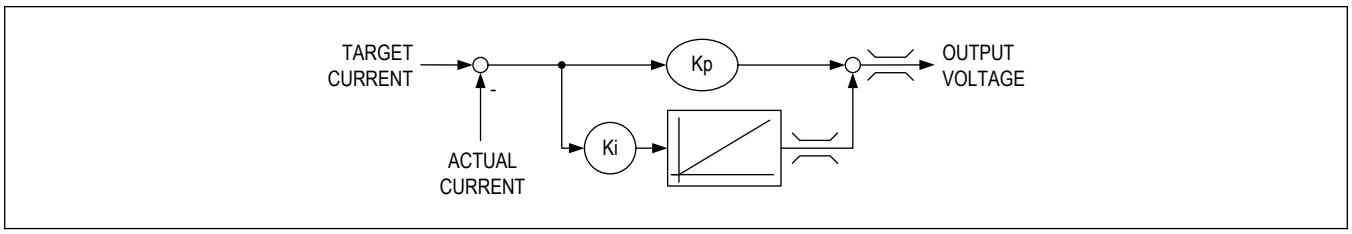


Figure 4. Block Diagram of Current Control Loop

As the output of the IC is affected and limited by the load, it is recommended that a tuning method that takes this into consideration.

Both P and I are 16-bit variables, accepting values from 0 to 65535, which gives a great level of control. It is also recommended to use the opening current and opening time given by the load manufacturer; in this case, they represent DC_L2H and TIME_L2H.

Minimum TON Limitations

For single-ended (HS or LS configurations) CDR operation, a minimum duty cycle of the low-side transistor has to be applied. This is needed to grant a correct measurement of the current. If the PI controller applies a duty cycle below the possible duty cycle, the output value of the PI controller will be overwritten. In this case, the integrator of the PI controller will be frozen unless the calculated values lead to a higher duty cycle on the low-side transistor. This behavior results in a minimal voltage above zero that can be applied in CDR mode in a LS driver configuration and a maximal voltage that is below the V_M supply voltage in a HS driver configuration. The below diagrams indicate the behavior of the LS driver and HS driver configurations.

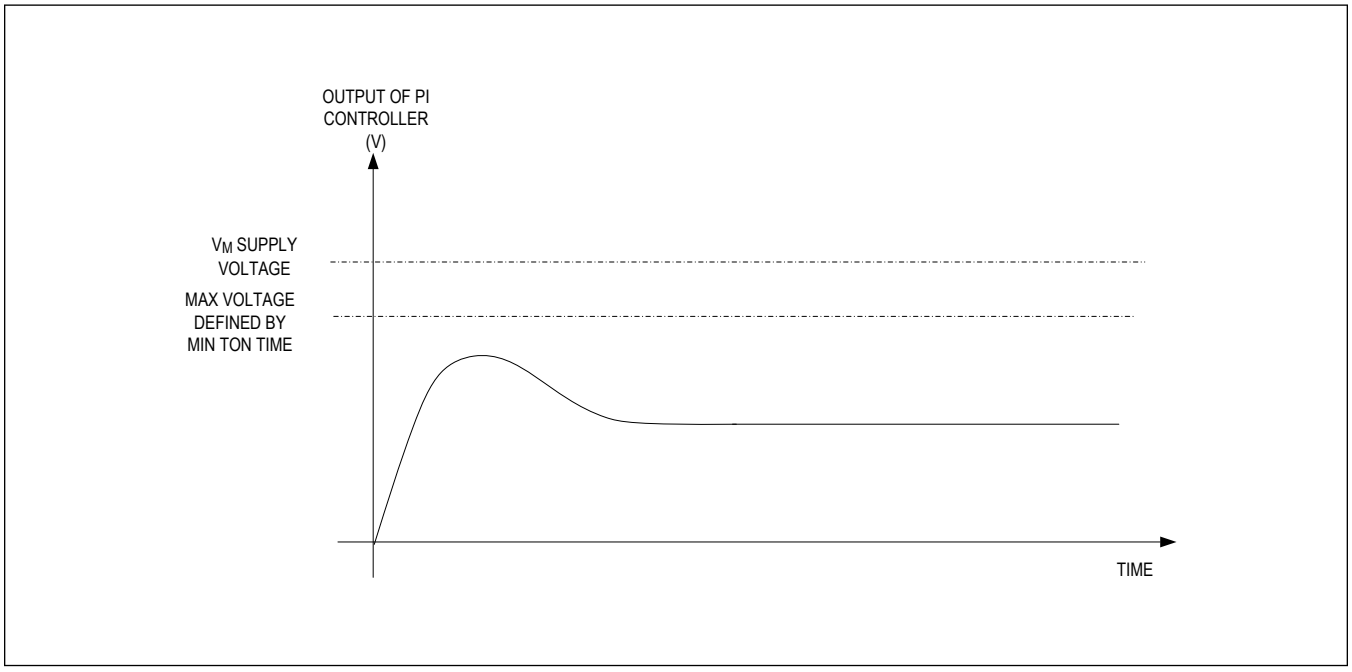


Figure 5. HS Configuration Maximal Voltage Graph

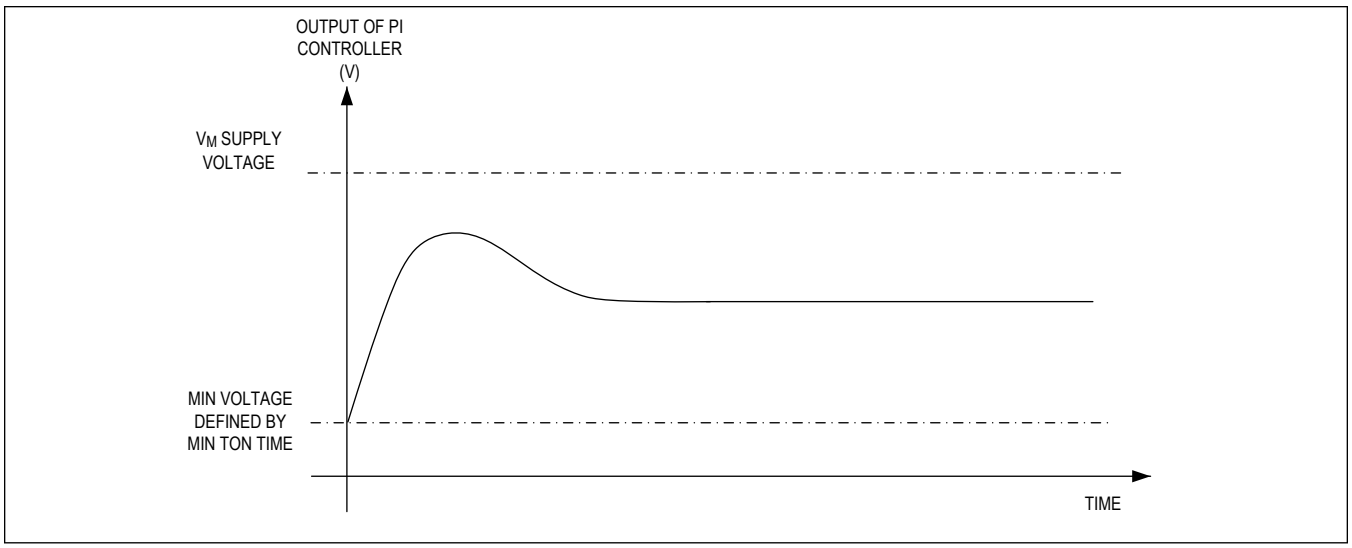


Figure 6. LS Configuration Minimal Voltage Graph

The minimal on-time on the low-side transistor is described by the formula:

$$MIN\_T\_ON = 2 \times (MIN\_TON\_SINGLE\_ENDED + 2^{SLEW\_RATE[1:0]+1} + 24*T\_BLANKING) \times 1/F\_PWM$$

The below formulas define the minimal/maximal voltages resulting from the minimal ON time on the low-side transistor for both the HS and LS driver configurations.

Single-ended LS configuration:

$$V_{MIN} = V_M \times MIN\_T\_ON \times F\_PWM$$

Single-ended HS configuration:

$$V_{MAX} = V_M \times (1 - MIN\_T\_ON \times F\_PWM)$$

To regulate a current in the single-ended configuration, the applied voltage in a steady state should not be too close to the resulting voltage constraint (V_{MIN} in the LS driver configuration, V_{MAX} in the HS driver configuration).

Current Reference

The user must connect a precise 12kΩ resistor between the I_{REF} pin and GND to set the reference current of the internal ADC. The MAX22216/MAX22217 reads the current flowing through the resistor by enforcing a constant voltage of about 0.9V on the I_{REF} pin. Therefore, the I_{REF} current is about

$$I_{REF}(A) = 0.9V/12k\Omega = 75\mu A$$

The current control accuracy directly depends on the I_{REF} current accuracy. Therefore, it is recommended to use 1% or more accurate resistors.

Setting the Excitation Time (TIME_L2H)

For solenoid drive operation, one 16-bit register allows the configuration of the excitation time (TIME_L2H) for each individual channel according to the following formula:

$$TIME\_L2H(s) = \frac{TIME\_L2H[15:0]_{DEC}}{F\_PWM}$$

in which F_PWM is the chopping frequency of the individual channel (see the *Setting the Chopping Frequency (FPWM)* section).

The TIME_L2H determines the per-programmed excitation time. The actual excitation time can be shortened and the power dissipation can be further reduced by using the automatic HIT to HOLD commutation function, which is based on the Detection of Plunger Movement (DPM) function (see the *Detection of Plunger Movement (DPM)* section).

If TIME_L2H[15:0] = 0xFFFF, the excitation level DC_L2H is applied continuously.

For Brushed DC Motor drive operation (CTRL_MODE[1:0] = 10), the content of this register assumes a different meaning and determines the limiter current threshold during braking operation. This function is explained in detail in the *Brake Current Limiter Function* section.

Setting the Ramp Slopes

Slowing down the rising/falling edges of the current in an ON/OFF solenoid valve smooths the mechanical movement of the plunger into an ON/OFF solenoid valve and reduces the acoustic clicking noise during activation/deactivation of the valve. Moreover, it also helps reducing over-/under-shoots of the current when the PI-based current drive regulation (CDR mode) is used. The RAMP function generates controlled ramps among the excitation, hold, and off levels. Eight bits in the channel configuration register (RAMP[7:0]) set the desired slew rates. Bits RDWE, RMDE, and RUPE enable/disable the function, respectively, for RAMP DW, RAMP MD, and RAMP UP (see the *Operating Modes* section). The ramp control is supported both in voltage and current drive modes. In VDR mode, the RAMP function ramps up/down the voltage applied to the load until the setpoint is reached. The voltage slew rate is approximatively given by the following formula:

$$\text{RAMP SLEW RATE [V/ms]} = K_{VDR} \times 36V \times (\text{RAMP[7:0]}_{DEC} + 1) * F\_PWM(kHz)$$

For instance, if the chopping frequency is 25kHz, the ramp-up slew rate can be configured from 0.4V/ms to 102V/ms. In VDRDUTY mode, the RAMP function ramps up/down the output duty cycle until the setpoint is reached. The voltage slew rate is approximatively given by the following formula:

$$\text{RAMP SLEW RATE [V/ms]} = K_{VDR} \times V_M \times (\text{RAMP[7:0]}_{DEC} + 1) * F\_PWM(kHz)$$

In CDR mode, the RAMP function ramps up/down the load current until the setpoint is reached. The current slew rate is approximatively given by the following formula: MAX22216 RAMP_SLEW_RATE (mA/ms) = K_{CDR} x GAIN x SNSF x $(\text{RAMP[7:0]}_{DEC} + 1)$ x F_PWM(kHz) MAX22217 RAMP_SLEW_RATE (mA/ms) = K_{CDR} x GAIN x $(\text{RAMP[7:0]}_{DEC} + 1)$ x F_PWM(kHz) For instance, if F_PWM = 25kHz and GAIN = SNSF = 1, the Slew Rate of MAX22216 can be configured from 25.425mA/ms to 6508.8mA/ms. It must be noted that the maximum slew rate achievable in CDR mode can be limited by system parameters. In particular, for inductive loads, the maximum slew rate cannot exceed the theoretical maximum equal to V_M/I_{LOAD}.

Enabling the Sine Wave Generator for Dithering or Inductance Measurement

The MAX22216/MAX22217 integrate a sine wave generator, which creates a sine wave signal with programmable frequency and amplitude.

The purpose of the sine wave generator is twofold:

1. It can be used to add dithering to the DC voltage or current in order to overcome static friction and hysteresis problems, which in particular affect proportional valves.
2. It can be used as an AC scan signal to measure the coil inductance and detect the on/off status of the solenoid valve for diagnostic purposes.

The DITH_EN and LMEAS_EN bits in the configuration register of each individual channel activate/deactivate either the dithering or the inductance measurement function. For the dithering function, the sine wave is superimposed onto the DC_H level with added noise at the DC_L level. For the inductance measurement function, it can be set to superimpose the sine wave onto DC_L2H and/or DC_H levels, while it is always superimposed on the DC_L level.

The sine wave generator starts after the first use of the channel. Table 10 summarizes how the function is activated and onto which DC levels the sine wave signal is applied.

- In case the sine wave is used for dithering (DITH_EN = "1", LMEAS_EN = "0"), the AC signal is superimposed onto the DC_H (hold) level and added noise at the DC_L (low) level. Both voltage and current control modes are supported. The main use of this function is to get rid of friction in proportional valves.
- In case the sine wave is aimed to measure the inductance for diagnostic purposes (LMEAS_EN = "1", DITH_EN = X), then the AC voltage sine wave is superimposed only if the DC level is controlled in voltage mode (VDR). The inductance measurement can possibly be done in every sequencer phase (DC_H2L, DC_H, and DC_L). Selection bits are available to enable/disable the measurement for the corresponding phase, as discussed in detail in the *Inductance Measurement* section. The primary use of the inductance measurement function is to detect the status of ON/OFF solenoid valves.

Table 10. Dither and Inductance Measurement Table

FUNCTION	ACTIVATION BITS	DESCRIPTION	CONTROL MODES	DRIVER PHASES	MAIN TARGET APPLICATION
Sine Off	DITH_EN = 0 LMEAS_EN = 0	Sine wave generator disabled			
Dither	DITH_EN = 1 LMEAS_EN = 0	AC current/voltage superimposed onto the DC current/voltage level	• **Supported both in CDR and VDR modes.** • AC SCAN amplitude can be either a current or a voltage, depending on the DC_H setting	DC_H and noise at the DC_L level	Proportional valves
Inductance Measurement	LMEAS_EN = 1 DITH_EN = don't care	• AC voltage superimposed onto the DC voltage level • AC current is measured for inductance measurement	• **VDR mode only**. • If CDR control is set, the sine wave generator is automatically disabled	DC_L always, DC_L2H, and DC_H selectable (L_MEAS_L2H, L_MEAS_H)	On/Off valves

Dithering enables a small level of noise at the DC_L level that can be used (together with the RAMP_SLEW_RATE control) to lower the impact of the valve armature onto the valve seal and prevent a sticky plunger in some applications. It is recommended to disable the function once the valve is closed. (right after turning off the channel), otherwise some valves may not close properly or heat up while not in use.

During the inductance or resistance measurements, the IND flag can be triggered when the channel turns off (depending on line noise and valve) due to the functionality of IAC_THLD when measuring the DC_L phase. In the case where the IND Flag is triggered continuously on the DC_L level (if it reappears after clearing, this usually happens when IAC_THLD is not 0), it is recommended to disable LMEAS_EN while the channel is off (if LMEAS is turned off before the channel, the IND flag should not appear when turning off the channel) or to limit the readings using L_NBR_CALC and clear the flag. The IND flag triggers when the channel is turned on due to the coil transient response; to counter this, use the L_MEAS_WCYCLES to create a delay in the inductance measurement readings. Similarly, if it does not set RES_THLD before turning on the channel (while LEAS_EN is in use), the RES Flag will trigger, as the standard value for RES_THLD is 0. Resistance measurements might also be affected by the transient response in some cases.

Setting the Sine Wave Generator

The sine wave amplitude and frequency can be configured as global parameters.

The sine wave frequency can be set by programming the global F_AC_SCAN register as shown in the formula below.

$$\text{Sine Wave Frequency (Hz)} = F\_PWM\_M \times (F\_AC\_SCAN[11:0]_{DEC}/65535)$$

The sine wave generator amplitude can be set by programming the global U_AC_SCAN register. Depending on the control mode, the amplitude is set as described below.

VDRDUTY	$VOUT\_AC\ (V) = K_{VDR} \times V_M \times U\_AC\_SCAN[14:0]_{DEC}$
VDR	$VOUT\_AC\ (V) = K_{VDR} \times 36 \times U\_AC\_SCAN\ [14:0]_{DEC}$
CDR MAX22216	$IOUT\_AC\ (mA) = K_{CDR} \times GAIN \times SNSF \times U\_AC\_SCAN[14:0]_{DEC}$
CDR MAX22217	$IOUT\_AC\ (mA) = K_{CDR} \times GAIN \times U\_AC\_SCAN[14:0]_{DEC}$

See the *CURRENT DRIVE REGULATION (CDR)* and *VOLTAGE DRIVE REGULATION (VDR)* sections for details about CDR and VDR parameters.

Brake Current Limiter Function

As shown in *OPERATING MODES OVERVIEW*, the MAX22216/MAX22217 can be used to drive a bidirectional DC motor in full-bridge configuration (CTRL_MODE[1:0] = 10).

To stop a running motor, the BRAKE condition has to be enforced (CNTL0 = CNTL1 = "1") (see Table 3 in the *Hardware Configuration* section). During brake, both sides of the load are driven with a 50% duty cycle, causing the load to be virtually shorted so that the deceleration begins.

Because the BEMF voltage gets virtually shorted, the brake current can be very high and limited only by the motor resistance. This causes the MAX22216/MAX22217 overcurrent protection to be triggered and the device to outputs to be tri-stated. To overcome the problem, the MAX22216/MAX22217 feature a brake current limiter function that allows the fastest deceleration given the current limit constraint.

If this function is triggered, the content of the CFG_L2H_TIME register (namely bits TIME_L2H[15:0]) sets the upper limit of the brake current (IBRAKE_LIM). Whenever the current amplitude exceeds the IBRAKE_LIM (see the formulas below), a current control loop is triggered, and the brake current is limited to the desired value, which is given by:

MAX22216	$I\_BRAKE\_LIM(mA) = K_{CDR} \times GAIN \times SNSF \times TIME\_L2H[15:0]_{DEC}$
MAX22217	$I\_BRAKE\_LIM(mA) = K_{CDR} \times GAIN \times TIME\_L2H[15:0]_{DEC}$

In particular, when TIME_L2H[15:0] = "0", the driver enforces HiZ (coast).

The CFG_L2H_TIME register of the channel with the lower channel count is used for this function, so only the first half of the register creates the BRAKE: 0x0001 to 0x7FFF.

DIAGNOSTIC FUNCTIONS AND STATUS MONITOR

Digital Current Monitor Function

The internally sensed current is sampled at the PWM frequency and stored into Read Only registers (I_MONITOR[15:0]). The user can read real time the I_MONITOR value via SPI for diagnostic and/or control purposes. During SPI read/write operations, the content of these registers is held. The digital current monitor function is available even in voltage drive modes (VDR or VDRDUTY). Similarly to what is described in the *CURRENT DRIVE REGULATION* section, the actual value of the current can be decoded using the following formulas:

MAX22216	$I_{MONITOR}(mA) = K_{CDR} \times GAIN \times SNSF \times I\_MONITOR[15:0]_{DEC}$
MAX22217	$I_{MONITOR}(mA) = K_{CDR} \times GAIN \times I\_MONITOR[15:0]_{DEC}$

The maximum digital value of the ADC for each individual channel is ±4095 (13 bits signed). For each parallel configuration, this maximum digital value is multiplied by the number of parallel systems (full- or half-bridge), but if one of the channels overflows (the current exceeds the maximum measurable current), the I_MONITOR shows the maximum possible measured value for that configuration.

I_MONITOR has to store the sum of up to 4 signed channel measurements (so it needs at least 15 bits); for this reason, it is stored in a 16-bit register. In the case of parallel channel configurations, the I_MONITOR will appear only in the Diagnostics of the main control channel. All the other diagnostics are channel-dependent, even in parallel channel configurations. Table 11 shows the maximum I_MONITOR digital value for each channel configuration.

Table 11. I_MONITOR ADC Max Value - Dec

CHS[3:0]	CONFIGURATION	CH0	CH1	CH2	CH3
0x0	4xIHB	4095	4095	4095	4095
0x1	3xPHB, 1xIHB	12287			4095
0x2	2xPHB, 2xIHB	8191		4095	4095
0x3	2xPHB, 2xPHB	8191		8191	
0x4	4xPHB	16383			
0x5	1xIFB, 1xIFB	4095		4095	
0x6	1xIFB, 2xIHB	4095		4095	4095
0x7	1xIFB, 2xPHB	4095		8191	
0x8	1xPFB	8191			

In the case of a full-bridge configuration, the secondary channel I_MONITOR shows the negative current flowing through it.

In the case of parallel half-bridges, the summed current will appear on the I_MONITOR of each channel, but for ease of use, it is recommended to use the I_MONITOR on CH0 (0x45). In full-bridge configurations, the main I_MONITOR channel is CH0 (0x45) or CH2 (0x57), and in parallel full-bridge the main I_MONITOR is on CH0 (0x45).

PWM Duty Cycle Monitor Function

16 bits register PWM_DUTY reports a real-time digital representation of the duty cycle applied to the load. This information is particularly useful in current drive regulation (CDR) to monitor the actual duty cycle applied to the load and detect possible anomalies.

Digital V_M Supply Voltage Monitor

The supply voltage (V_M) is internally measured and digitized. The user can monitor the real-time supply voltage by reading the VM_MONITOR[15:0] register via SPI. This information can be decoded using the following formula:

$$VM(V) = K_{VM} \times VM\_MONITOR[15:0]_{DEC}$$

Where K_{VM} = 9.73mV typical.

Inductance Measurement Overview

The sine wave voltage generator (see the *Enabling the Sine Wave Generator* and *Setting the Sine Wave Generator* sections) can be used to indirectly estimate the solenoid inductance by measuring the AC current induced by the AC scan voltage. The value of the inductance is, at first order, inversely proportional to the air gap. Therefore, the measurement of the inductance provides a sensor-less estimate of the spool displacement inside the valve. When driving ON/OFF valves, this technique can be used as a diagnostic tool to assess whether the valve is open or closed (see the *Status Monitor (STAT)* section).

This function is supported in both VDR and VDR_DUTY modes, although VDR is normally recommended as it is less sensitive to supply variations. The function is not supported in CDR Mode.

The inductance measurement activated the I_AC readings, which measure the current AC wave amplitude and the current median level of the output. For the I_AC measurement, it is important to consider that the IC filters the read signal around the Sine Wave Generator frequency. This means that it does not see a lot of higher-frequency noise at the output, which can create a measurement bias. Both the I_AC measurement and the average bias are usually very stable.

The MAX22216/MAX22217 measure the AC current generated by the scan AC sine wave voltage and store the result in the read-only register I_AC[15:0].

The AC current value in Amperes is given by:

MAX22216	$I\_AC\ (mA) = K_{CDR} \times GAIN \times SNSF \times I\_AC[15:0]_{DEC}$
MAX22217	$I\_AC\ (mA) = K_{CDR} \times GAIN \times I\_AC[15:0]_{DEC}$

A rough calculation of the solenoid inductance in Henry is then given by:

$$L[H] = \frac{U\_AC\_SCAN}{2\pi \times F\_AC\_SCAN \times I\_AC}$$

in which U_AC_SCAN and F_AC_SCAN are, respectively, the amplitude and frequency of the AC voltage scan signal. The actual inductance of the valve can significantly differ from what is predicted by this formula. First, the simple L+R model assumed for the calculation is really a rough approximation of the electrical model of a solenoid, in which many parameters play a role (coil saturation, eddy currents, magnetic hysteresis, load effects, etc.). Secondarily, similarly to what was discussed regarding the VDR mode generating the DC levels (see the *VOLTAGE DRIVE REGULATION (VDR)* section), the generation of the AC scan voltage is affected by errors, especially when high chopping frequencies and slow PWM edges are used. Nevertheless, the measurement of the absolute value of the I_AC current has been found to be a good indicator to determine whether the plunger is in the ON or OFF position, making the method reliable for valves in which the I_AC in the two statuses are well separated.

For HS or LS drives (single-ended operation), the superimposed AC signal amplitude must be less than the applied DC level. To measure the inductance when the coil is de-energized, the user must enforce a DC level (DC_L) small enough to ensure the solenoid does not change its status but large enough to superimpose enough AC signal for the measurement.

Setting the Inductance Measurement

Two 16 bits registers (CFG_IND_0 [15:0] and CFG_IND_1[15:0]) store the configuration parameters for the inductance measurement (or, better said, the I_AC measurement) function for each individual channel.

As mentioned in the *Enabling the Sine Wave Generator for Dithering or Inductance Measurement* section, the bit L_MEAS_EN enables the function.

It is required that the I_AC measurement starts only after the drive voltage has settled down to the pre-programmed DC level. By writing L_MEAS_WCYCLES, the user can set a delay from the change of the DC level to the actual start of the I_AC measurement. This delay is expressed in the number of AC scan periods.

The I_AC measurement is the average of multiple measurements on consecutive scan periods. By writing the L_NBR_CALC bits, the user can set the duration of the measurement. Such a duration is expressed in the number of AC scan periods.

In some applications, the solenoid is intentionally overdriven during the excitation time (TIME_L2H), causing the coil to saturate. When this occurs, the inductance measurement becomes unreliable and misleading. The L_MEAS_L2H bit allows to inhibit the AC signal and any inductance measurement during the excitation time. Similarly, the L_MEAS_H bit allows to disable the inductance measurement during the hold phase (level H) if the coil saturates during said phase. Measurements performed during the OFF phase (or DC_L phase) are generally more reliable.

The IAC_THLD[11:0] bits set the threshold, which can be used for diagnostic purposes or to detect the status of the valve.

After the completion of the measurement, the content of the I_AC[11:0] register is compared with the content of the IAC_THLD[11:0] register.

If, as a result of the comparison, a fault is detected, the flag bit IND in the FAULT register is set.

While in DC_L2H or DC_H phase, the Fault is signaled out if the measured I_AC amplitude is found larger than the threshold. Vice versa, while in DC_L phase, a Fault is signaled out if the measured I_AC is found smaller than the threshold. Table 12 summarizes the fault conditions.

Table 12. Inductance Measurement Fault Detection

PHASE	CONDITION	IND FAULT	DESCRIPTION
DC_L2H DC_H	I_AC > IAC_THLD	1	A fault gets signaled out if the measured amplitude of the AC signal is larger than the configured IAC_THLD
DC_L	I_AC < IAC_THLD	1	A fault gets signaled out if the measured amplitude of the AC signal is smaller than the configured IAC_THLD

The comparison between I_AC and IAC_THLD can also be used to monitor the status of the valve.

The MAX22216/MAX22217 can be configured in such a way that the STT[3:0] bits in the STATUS register and/or the STAT0, STAT1 output pins of the MAX22216/MAX22217 directly reflect the result of the comparison, as shown in Table 13. This is discussed in more detail in the next paragraphs.

Table 13. STATUS Monitor Based on Inductance Measurement

OUTPUT STATUS BITS/PINS	STT[3:0] BITS STAT0, STAT1 PINS
I_AC > IAC_THLD	0
I_AC <IAC_THLD	1

Detection of Plunger Movement (DPM) - Overview

The detection of plunger movement (DPM) function senses the local dip of the current caused by the BEMF, which is generated by the plunger movement when the valve is activated. This detection is active during the entire TIME_L2H excitation time.

This function is available both in voltage mode (VDR) and in current mode (CDR).

In VDR mode, the plunger movement can be reliably detected in the entire TIME_L2H excitation time.

In CDR mode, once the excitation level (DC_L2H) has been reached, the internal control loop counteracts the BEMF perturbation in an attempt to stabilize the current, which makes the plunger movement detection problematic. For this reason, the DPM function in CDR is more reliable when the BEMF dip occurs during the excitation current ramp-up.

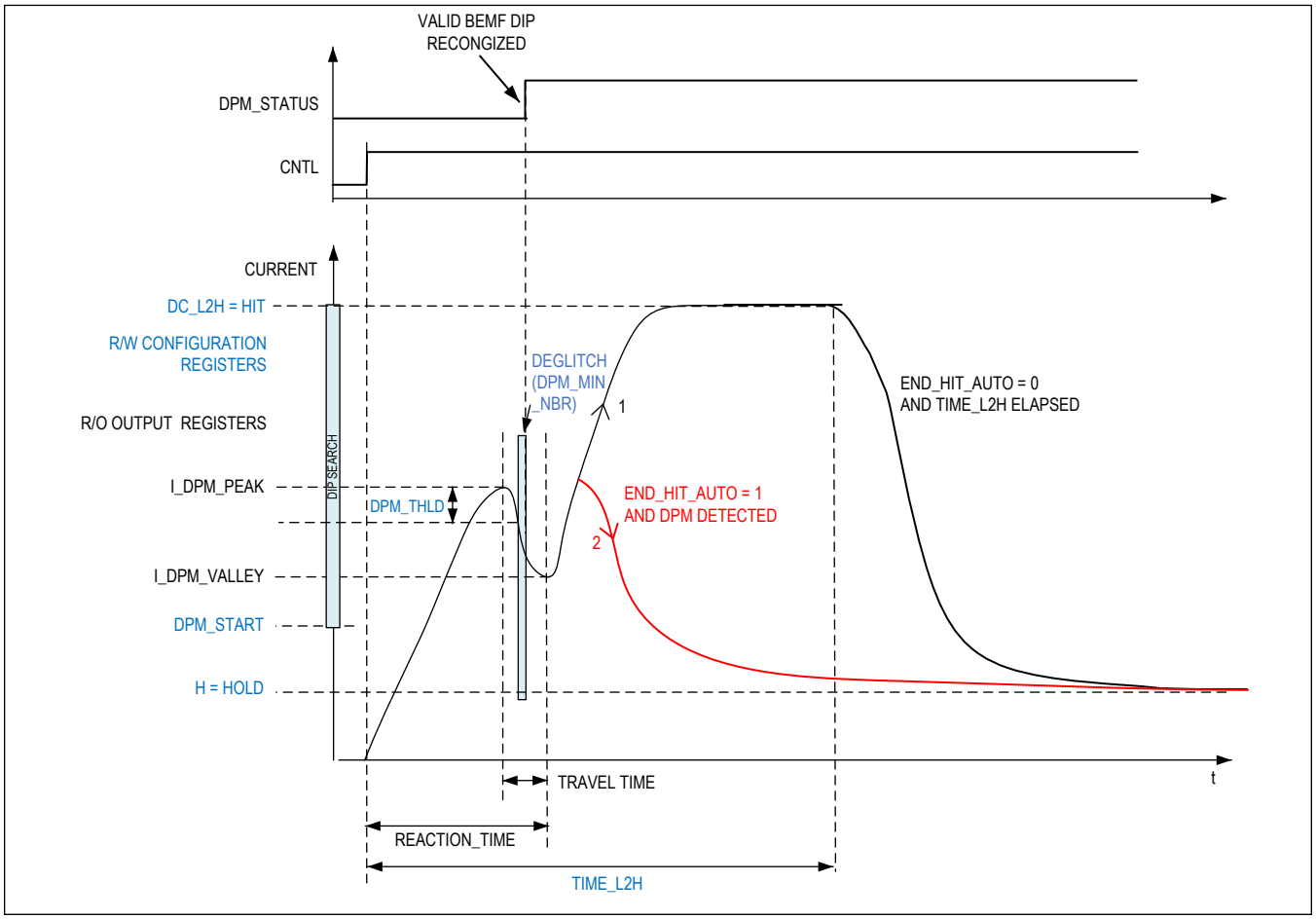


Figure 7. Detection of Plunger Movement

Figure 7 shows the typical current signature of a properly working solenoid valve. The algorithm works on the rising edge of the current only (valve activation). DPM_START and DPM_THLD are current thresholds used to reduce noise and lower false triggers and errors.

When a current depth larger than DPM_THLD occurs, a valid plunger movement is detected and DPM_STATUS is triggered. After the end of the dip, the DPM calculates the TRAVEL_TIME and the REACTION_TIME.

If the END_HIT_AUTO bit is set logic low, then the sequencer increases the current/voltage up to DC_L2H level and switches to DC_H only when TIME_L2H has elapsed.

If the END_HIT_AUTO bit is set logic high, then as soon as the DPM confirms a valid plunger movement, the sequencer automatically enforces the DC_H setpoint, resulting in significant power savings.

The amplitude of the dip and its relative position along the current rising edge are useful indications of the status and aging of the valve.

When activated, the DPM function implemented in the MAX22216/MAX22217 outputs the four parameters (I_DPM_PEAK, I_DPM_VALLEY, REACTION_TIME, and TRAVEL_TIME) that are stored in the corresponding Diagnostic Read Only registers of each individual channel and can be used to analyze the status of the solenoid.

With reference to Figure 7,

1. I_DPM_PEAK[15:0] represents the local maximum of the current (local peak) during the excitation phase.
2. I_DPM_VALLEY[15:0] represents the local minimum of the current (local valley) during the excitation phase.
3. REACTION_TIME[15:0] represents the time interval expressed in the number of PWM periods from the ON command to the local minimum of the current.
4. TRAVEL_TIME[15:0] represents the time interval expressed in the number of PWM periods from the local maximum to the local minimum of the current.

A drift of these parameters is a symptom of the aging of the valve and indicates the need for preventive maintenance of the valve during its operating life. The REACTION_TIME and TRAVEL_TIME can be calculated using the following formula:

REACTION_TIME (ms) = REACTION_TIME[15:0]/F_PWM
TRAVEL_TIME (ms) = TRAVEL_TIME[15:0]/F_PWM

I_DPM_PEAK and I_DPM_VALLEY are numeric representations of the currents. The actual values can be calculated using the formulas below.

MAX22216	$I\_DPM\_(mA) = 8 \times K_{CDR} \times GAIN \times SNSF \times I\_DPM\_[11:0]_{DEC}$
MAX22217	$I\_DPM\_(mA) = 8 \times K_{CDR} \times GAIN \times I\_DPM\_[11:0]_{DEC}$

When the sequencer starts and if the DPM function is enabled, the algorithm first searches for I_DPM_PEAK and updates the resister once the peak is found.

Afterwards, the I_DPM_VALLEY, the REACTION_TIME, and the TRAVEL_TIME registers get written when either the current has risen back to the local maximum level or the TIME_L2H has elapsed. This ends DPM detection.

Setting the Detection of Plunger Movement

Several parameters can be configured independently for each individual channel to configure and tune the DPM algorithm. They are stored in two 16 bits registers named CFG_DPM0[15:0] and CFG_DPM1[15:0]. (See the Register Map section.)

The DPM_EN bit into CFG_DPM1[15:0] is the enable bit. Set this bit high to enable the DPM function for that specific channel.

As shown in Figure 7, the algorithm starts searching for the BEMF dip above a programmable current level given by,

MAX22216	$DPM\_START(mA) = 64 \times K_{CDR} \times GAIN \times SNSF \times DPM\_START[7:0]_{DEC}$
MAX22217	$DPM\_START(mA) = 64 \times K_{CDR} \times GAIN \times DPM\_START[7:0]_{DEC}$

in which DPM_START[7:0] is an 8 bitfield into the CFG_DPM1 register.

As soon as the local maximum of the current I_DPM_PEAK is detected, it is stored in the corresponding R/O register. The algorithm then compares the subsequent dip caused by the plunger movement with a programmable threshold, which can be set by writing the DPM_THLD[11:0] bit field in the CFG_DPM0 register. Current thresholds are given by,

MAX22216	$DPM\_THLD(mA) = 8 \times K_{CDR} \times GAIN \times SNSF \times DPM\_THLD[11:0]_{DEC}$
MAX22217	$DPM\_THLD(mA) = 8 \times K_{CDR} \times GAIN \times DPM\_THLD[11:0]_{DEC}$

The user can set a deglitch time to avoid a false BEMF dip being detected. The deglitch time is set in the number of PWM cycles and is equal to:

$$DPM\_DEGLITCH = 2 \times DPM\_MIN\_NBR[3:0]_{DEC} \times 1/FPWM$$

in which DPM_MIN_NBR[3:0] is a 4 bits bitfield into into the CFG_DPM1 register.

If the current drops from the peak more than the DPM_THLD for longer than the DPM_DEGLITCH, then a valid BEMF dip is detected, meaning that the valve is working properly.

As soon as a valid BEMF dip has been recognized, the algorithm starts searching the local valley (the local minimum in the current profile). When the local valley is found, its value is stored into the I_DPM_VALLEY register. Moreover, the DPM_STATUS bit in the STATUS register is set. Since the STATUS bit is cleared every time the valve is deactivated (CNTL goes low), the DPM_STATUS bit is informative on whether the valve has been properly activated (see the

STATUS section).

Vice versa, in case if no valid BEMF dip has been recognized during the whole DC_H2L time interval (Hit or Excitation time), then the DPM_STATUS bit remains low and the DPM_FAULT bit is set and can possibly be signaled out (see the *FAULT* section).

Finally, it is also possible to configure the MAX22216/MAX22217 so that the sequencer ends the excitation phase (HIT) as soon as a valid BEMF dip is detected. Two bits in CFG_DPM1 control this function: END_HIT_AUTO and END_HIT_HIZ_AUTO.

- Set END_HIT_AUTO = "1" to enable the automatic DC_H2L to DC_H switchover once a valid BEMF dip is detected and the current has risen back to the local maximum level (I_DPM_PEAK). This is shown with the red curve into the *Detection of Plunger Movement (DPM)*.
- Set END_HIT_HIZ_AUTO = "1" to enable the automatic DC_H2L to HiZ (High Impedance) switchover once a valid BEMF dip is detected and the current has risen back to the local maximum level. If no BEMF dip is detected, the drive phase will switch to HiZ when the TIME_L2H elapses.

The END_HIT_AUTO or the END_HIT_HIZ_AUTO dramatically improves the drive efficiency in latched valve applications.

Resistance Measurement

The MAX22216/MAX22217 can be configured to calculate the equivalent resistance of the coil. As the resistance is expected to increase when the coil temperature increases, this function enables an indirect measurement of the solenoid or motor temperature.

To enable the function, the inductance measurement must be enabled (see the *Setting the Inductance Measurement* section). If the inductance measurement is not required and only the resistance measurement is needed, the user can simply set the AC_SCAN amplitude to zero so that only a DC level is applied to the load.

The resistance measurement is performed by dividing the average voltage and average current applied to the load during the inductance measurement (see the *Setting the Inductance Measurement* section). The measured resistance for each individual channel can be read by accessing the RES[15:0] bits via SPI.

The resistance measurement formula is:

$$R = R[15:0] \times (K_R/(SNSF * GAIN))$$

Where K_R = 8.43mΩ.

The user can set a resistance threshold by writing the RES_THLD[15:0] bits into the configuration registers.

If the calculated resistance exceeds the RES_THLD value, then the MAX22216/MAX22217 set the RES status bit into the STATUS register. Moreover, the RES_ bit in the FAULT register can be set, and a fault can possibly be signaled out (see the *PROTECTIONS AND FAULT INDICATOR* section).

Setting the Status Monitor

The MAX22216/MAX22217 allow monitoring the channel status either by reading the STT[3:0] bits into the STATUS register via SPI or by observing the STAT0 and STAT1 logic output pins. The status monitor function can be configured by writing the Global Register STATUS_CFG[15:0].

Status information is mapped onto the STAT0 and STAT1 output pins according to Table 14, in which CHS determines the Hardware configuration (see the *Setting the Hardware Configuration* section), and STAT_SEL0 and STAT_SEL1 are two selection bits in the STATUS_CFG register.

Note that if a channel is configured in a full-bridge configuration (FB), the status pins output the logical OR of the STT_ bits of the corresponding channels in all modes except for PWM monitoring. When PWM monitoring is selected, the STAT_ pin outputs the PWM signal of the half bridge with the lower channel count. The polarity of the STAT pins can be changed with the STAT_POL bit in the GLOBAL_CFG register.

The MAX22216/MAX22217 can be configured to output different types of information. Table 15 summarizes all the possible settings. Three STAT_FUN[2:0] bits into the STATUS_CFG register permit the selection of the desired function.

STAT_FUN 0x0: ON/OFF Status is detected based on the inductance measurement. This is achieved by comparing the internally measured I_AC with a user-configurable threshold, IAC_THLD. This threshold can be programmed individually

for each channel. (See the *Inductance Measurement* section).

STAT_FUN **0x1:** The STAT pins act as PWM Monitor outputs. In this configuration, a low-voltage replica of the PWM signal applied to the load is output on the status pin (STAT) for monitoring purposes. In particular, if MAX22216/MAX22217 are configured in CDR mode, the STAT signal can be processed by an external processor to detect stall conditions, load or supply disconnections, or any abrupt changes in the load conditions causing an abnormal duty cycle variation.

STAT_FUN **0x2:** STT bits are set (and hence the STAT pin outputs a logic high value) every time the Coil resistance exceeds a pre-programmed threshold (RES_THLD). (See the *Resistance Measurement* section).

STAT_FUN **0x3:** ON/OFF Status is detected based on the detection of plunger movement. When this configuration is used, the STT bit is cleared (and hence the STAT pins are de-asserted) every time the channel is OFF (i.e., CNTL = 0). When a valid BEMF dip is detected during the excitation phase, the STT bit is set (and hence the STAT pin is asserted).

STAT_FUN **0x4:** In this configuration, the STT bits are set and the STAT pins are asserted when the part is supplied (V_M greater than UVLO) and cleared when the V_M drops (V_M less than UVLO). This stat is mainly used to show that the IC is within a functional voltage range, so it can also be controlled using VM_THLD_DOWN or a combination of VM_THLD_DOWN and VM_THLD_UP, presented in more detail in the *V_M Switching Stand-Alone* section.

STAT_FUN **0x5:** the STT bits are set and the STAT pins asserted when the coil current from the I_MONITOR is higher than a programmable DC current threshold (IDC_THLD). The IDC_THLD can be programmed individually for each channel by writing the 16 bits CFG_IDC_THLD[15:0] register. In full-bridge configuration, the IDC_THLD must be set on both channels. In comparison, in parallel full bridge, it must be set only on CH0 and CH1, while triggering both STAT pins independent of STAT_SEL. In parallel configurations, the IDC_THLD must be set based on the sum of currents on all channels, but only on the main control channel, and it will trigger the STAT on all connected channels. The threshold is given by

MAX22216	IDC_THLD (mA) = K_{CDR} x GAIN x SNSF x IDC_THLD[15:0]$_{DEC}$
MAX22217	IDC_THLD (mA) = K_{CDR} x GAIN x IDC_THLD[15:0]$_{DEC}$

See also *STAT Monitor - Single-Ended Diagrams* and *STAT Monitor - Differential Diagrams* for a visual representation of the status monitor function.

Table 14. STAT Logic Output Pin Selection

CHS	CONFIGURATION SETTING	STAT0	STAT1
0x0	4x Independent HB	STT0 if STAT_SEL(0) = 0 STT1 if STAT_SEL(0) = 1	STT2 if STAT_SEL(1) = 0 STT3 if STAT_SEL(1) = 1
0x1	3x Parallel HB 1x Independent HB	STT0=STT1 = STT2	STT3
0x2	2x Parallel HB 2x Independent HB	STT0 = STT1	STT2 if STAT_SEL(1) = 0 STT3 if STAT_SEL(1) = 1
0x3	2x Parallel HB 2x Parallel HB	STT0 = STT1	STT2 = STT3
0x4	4x Parallel HB	STT0 = STT1 = STT2 = STT3	-
0x5	1x Independent FB 1x Independent FB	STT0 in PWM monitoring (STT0 OR STT1) all other modes	STT2 in PWM monitoring (STT2 OR STT3) all other modes
0x6	1x Independent FB 2x Independent HB	STT0 in PWM monitoring (STT0 OR STT1) all other modes	STT2 if STAT_SEL(1) = 0 STT3 if STAT_SEL(1) = 1
0x7	1x Independent FB 2x Parallel HB	STT0 in PWM monitoring (STT0 OR STT1) all other modes	STT2 = STT3
0x8	1x Parallel FB	STT0 if STAT_SEL(0) = 0 STT1 if STAT_SEL(0) = 1	STT0 if STAT_SEL(0) = 0 STT1 if STAT_SEL(0) = 1

Table 15. Multifunction Status Pin

STAT_FUN	FUNCTION	CONDITION	STAT STAT_POL = "0"	STAT STAT_POL = "1"	STT BITS
0x0	Status detection based on the inductance measurement	if IAC > IAC_THLD	Low	High	"0"
		if IAC < IAC_THLD	High	Low	"1"
0x1	PWM monitor	-	PWM	$\overline{PWM}$	n/a
0x2	Status detection based on resistance measurement	if RES < RES_THLD	Low	High	"0"
		if RES > RES_THLD	High	Low	"1"
0x3	Status detection based on successful plunger movement (DPM)	if CNTL = Low or CNTL = HIGH but DPM not detected	Low	High	"0"
		if CNTL = HIGH and DPM is detected	High	Low	"1"
0x4	Status detection based on V_M detection	if V_M < UVLO	Low	High	"0"
		if V_M > UVLO	High	Low	"1"
0x5	Status detection based on I_MONITOR measurement	if I_MONITOR < IDC_THLD	Low	High	"0"
		if I_MONITOR> IDC_THLD	High	Low	"1"

STAT Monitor - Single-Ended Diagrams

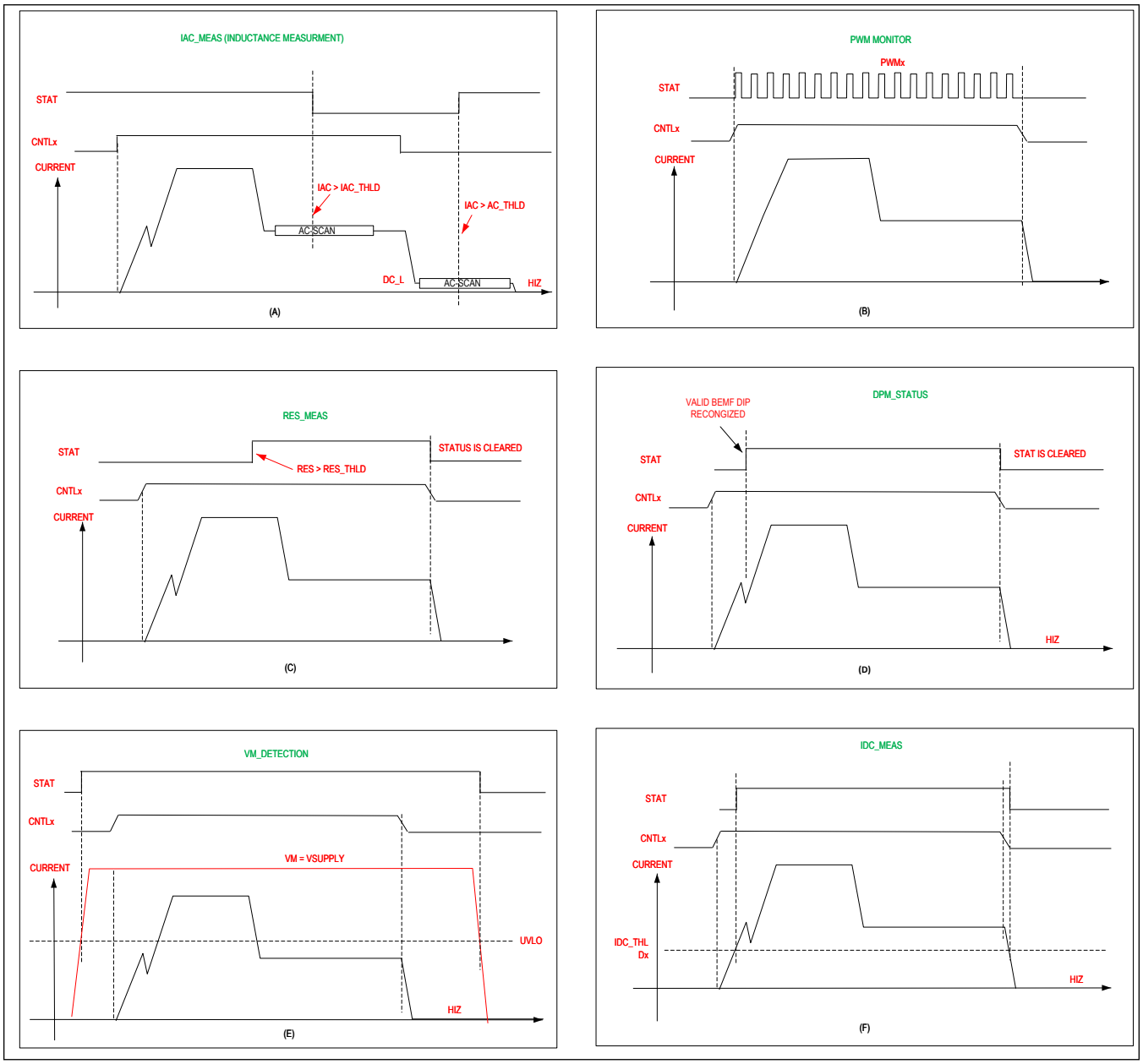


Figure 8. STATUS Output Monitor Pin - Single Ended

STAT Monitor - Differential Diagrams

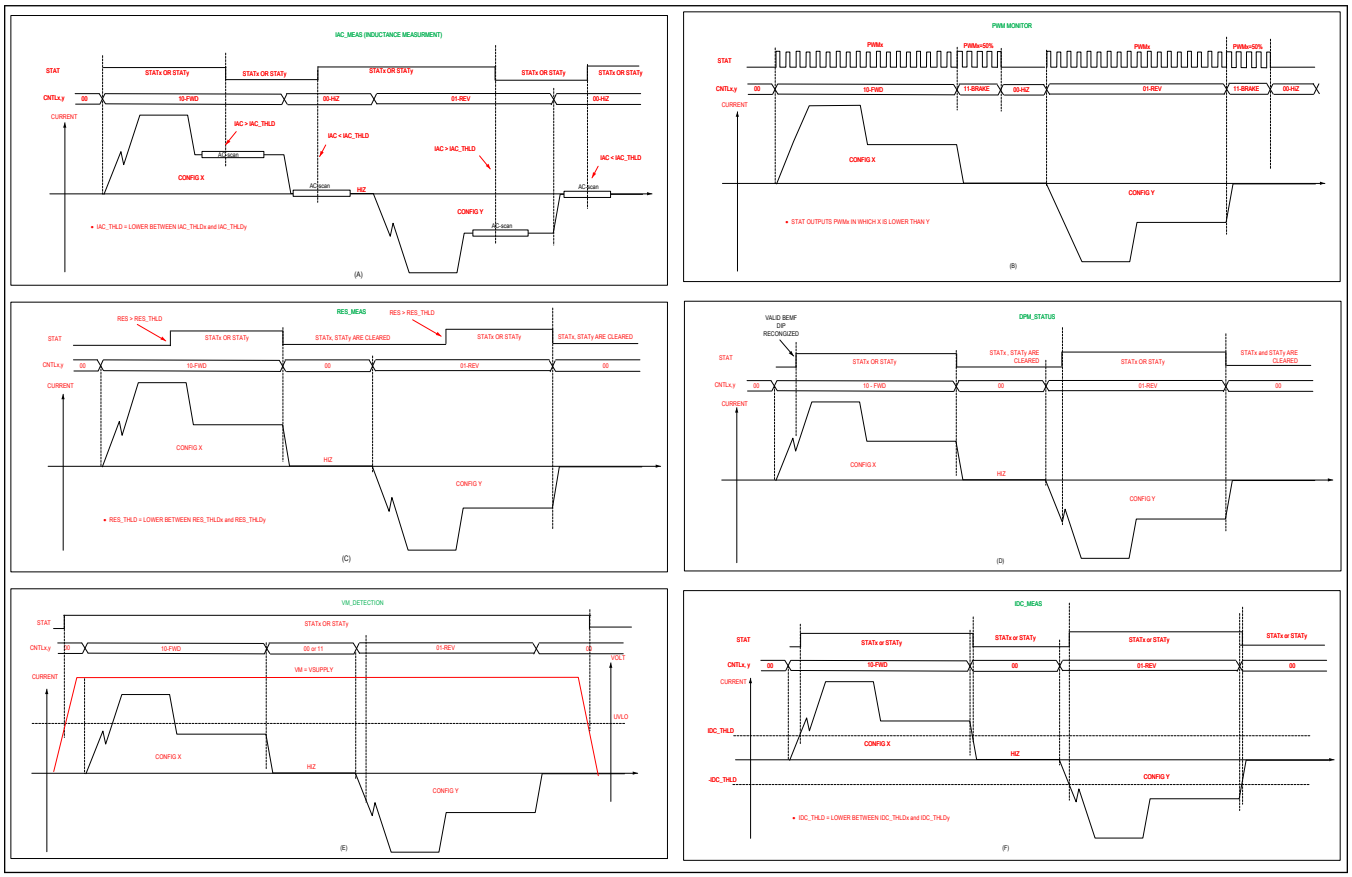


Figure 9. STATUS Output Monitor Pin - Differential

PROTECTIONS AND FAULT INDICATOR

Protections and Fault Indicator Pin ($\overline{\text{FAULT}}$)

The MAX22216/MAX22217 feature a full set of protections and diagnostic functions. These include:

1. Undervoltage lockout (UVM)
2. Overcurrent protection (OCP)
3. Overtemperature protection (OVT)
4. Open-load detection (OL)
5. "Hit current not reached" detection (HHF)
6. Communication error detection (COMER)
7. Detection of plunger movement fault (DPM)
8. Inductance measurement (IND)
9. Load resistance fault (RES)

Every time a fault occurs, the corresponding global bit in the R/O STATUS register is set.

Fault events are also logged into two R/O 16 bits fault registers named FAULT0[15:0] and FAULT1[15:0] for diagnostic purposes. Dedicated flag bits for each channel are available for OCP, OL, HHF, DPM, IND, and RES faults so that the user can determine which of the channels failed. The fault registers are "Write one to clear registers". The user can read back the registers via SPI and decide to clear each individual fault flag by writing "1" to the corresponding bit. Alternatively, the fault registers can be cleared by driving the ENABLE pin logic low or by powering off the device (power

cycling).

An active low open-drain fault indicator pin ($\overline{FAULT}$) is available to signal out the fault condition for each of the above mentioned faults, with the exception of the IND and RES faults.

Faults can be masked by setting high the corresponding mask bit in the 16 bits global register GLOBAL_CFG[15:0] register. When masked, the fault event does not activate the FAULT pin, so the external controller does not receive any interrupts. The mask bits are listed in the Table 16. The default value is zero.

Table 16. Mask Bits

FAULT	MASK BIT
UVM	M_UVM
OCP	M_OCP
OVT	M_OVT
OL	M_OLF
HHF	M_HHF
DPM	M_DPM
COMER	M_COM

Two bits in the STATUS_CFG register (STRETCH_EN[1:0]) can be used to stretch the duration of the fault signal following an undervoltage (UVM) or an overtemperature (OVT) fault detection, as shown in Table 17. This function ensures the $\overline{FAULT}$ pin is kept active (logic low) for a minimum time interval (stretch time) after the fault occurrence. Whenever the $\overline{FAULT}$ pin is used to drive an external LED (for instance, in stand-alone use cases), setting a long stretch time allows visual observation of the fault event.

Table 17. Stretch Enable

STRETCH_EN	STRETCH TIME
00b	No stretch
01b	1s
10b	2s
11b	3s

Undervoltage Lockout (UVM)

If at any time the voltage on the V_M pin falls below the undervoltage lockout threshold (about +4V typ), all channels are tri-stated, the internal charge pump is disabled, and the UVM bits in the fault register and in the STATUS register are set. The content of the logic registers is preserved until V_{DD} falls below the digital power-on reset (POR) threshold. When this happens (typically at V_{DD} = 1.0V), all registers are reset to their default values.

The output of the UVLO comparator activates the $\overline{FAULT}$ indicator pin if it is not masked.

On the $\overline{FAULT}$ pin, the user can choose to output either the non-latched information of the UVLO comparator or the latched UVM bit information from the register map (see Figure 10).

Moreover, in the former case, the user can set a minimum $\overline{FAULT}$ assertion time (Stretch Time; see the *Protections and Fault Indicator Pin (FAULT)* section).

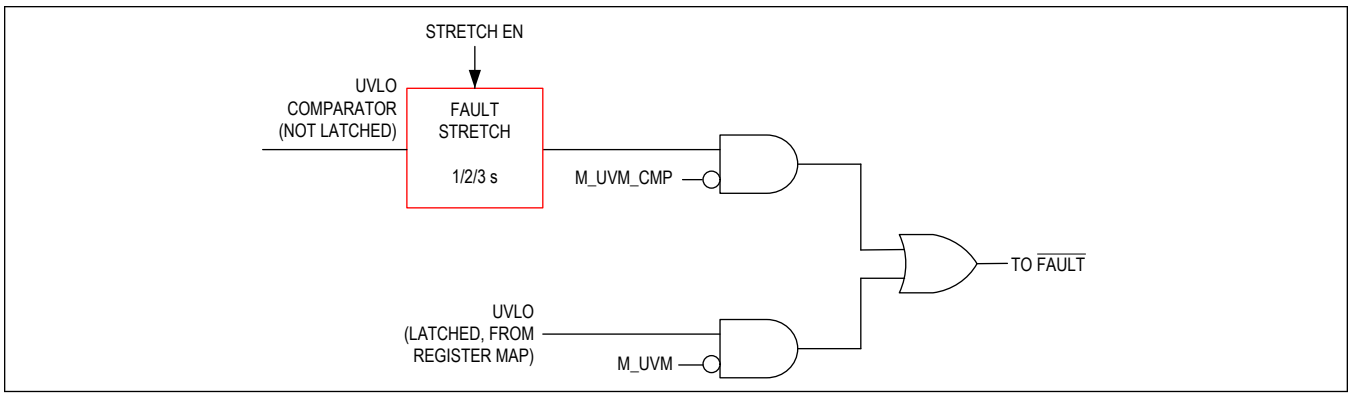


Figure 10. Fault Output Schematic

Overcurrent Protection (OCP)

The overcurrent protection protects the device from short-circuits of the driver outputs to the rails (V_M and GND) or across the load. When the output current exceeds OCP thresholds (see the *Electrical Characteristic* table), then the corresponding channel is automatically tri-stated, the global OCP bit in the STATUS register as well as the individual OCP_ bit in the $\overline{FAULT}$ register are set, and the $\overline{FAULT}$ output is asserted (if not masked). Writing one to the fault register clears the flag and de-asserts the $\overline{FAULT}$ output but does not turn on the failed channel. Once the flag is cleared, normal operations are resumed by turning the failed channel off in the status register. In bridge-tied load or parallel configurations, all the channels that form the full bridge or the parallel configuration must be turned off to resume normal operation.

Open-Load Detection During Channel OFF (OL)

The OL_EN bit in the CFG_CTRL register enables or disables the open-load detection (OL) function. When this function is enabled, whenever the channel is tri-stated, a small source/sink current pulls the output node (I_{OL_LS}, I_{OL_HS}).

In single-ended configuration, if the voltage on the output pin is found to be less than V_{OL_LS} for low-side configuration or greater than V_{OL_HS} for high-side configuration, then an open-load condition is detected.

In full-bridge configuration, for the open-load detection to work properly, both channels must have open-load enabled, and the bridge must have one output configured as low-side (HSnLS_x = 0) and the other output as high-side (HSnLS_y = 1). The open-load condition is detected if both sides detect an open-load condition, and it will appear as OLF for both channels at the same time. In the case of parallel full-bridges, open-load detection has to be set on all channels, and two channels on the same side of the full-bridge have to be set to HSnLS (CH0 and CH1 or Ch2 and CH3). The OLF will appear for all channels at the same time.

If multiple channels are configured in parallel, even if the channels are connected via the PCB, the open-load detection will work independently for each of the channels connected in parallel. Generally, it is recommended use open-load detection only on the main control channel. In the case of using parallel half-bridges together with the HSnLS, if there is a need of open-load detection on all channels, each channel has to be individually set to HSnLS.

In all the cases, a relatively long deglitch time (t_{OL} = 200µs typ) starting from the enabling of the function ensures the output has settled down before the open-load condition is checked.

When an open-load condition is detected, the corresponding bit in the fault register as well as the OLF bit in the STATUS register are set. The $\overline{FAULT}$ output pin is also asserted if it is not masked.

Overtemperature Protection (OVT)

If the die temperature exceeds safe limits, all outputs are disabled. The OVT flag bit in the $\overline{FAULT}$ and STATUS registers is set, and the $\overline{FAULT}$ pin is driven low if not masked.

Once the die temperature has fallen to a safe level, operation automatically resumes. The $\overline{FAULT}$ pin is released after the stretch time (see the *Protection and Fault Indicator* section), but the flag bit remains set to '1' until the fault register is write to one.

"HIT Current not Reached" Flag (HHF)

In CDR mode, the user can monitor whether the preprogrammed HIT current level is reached. This diagnostic tool can be enabled by setting the bit HHF_EN_ to "1" in the CFG_CTRL register. If the target current is not reached at the end of TIME_L2H, then the individual HHF flag bit in the Fault register as well as the global HHF bit in the STATUS register are set. The $\overline{FAULT}$ indication pin is asserted if not masked. Note that this fault does not tri-state the driver. The flag bit is cleaned up when the fault register is write to one.

HOW TO CONFIGURE THE MAX22216/MAX22217

SPI Description

The MAX22216/MAX22217 feature a 10MHz capable serial peripheral interface (SPI) with cyclic redundancy check control (CRC) control. The CRC control is optional and can be activated by driving logic high the pin CRC_EN.

The SPI supports daisy-chain connections so that multiple devices can be controlled from a single SPI. SDI input is clocked in on the rising edge of the SCK signal. Data output on SDO is clocked out on the falling edge of the SCK signal.

The SPI transfers are byte-oriented.

SPI transactions without CRC error detection.

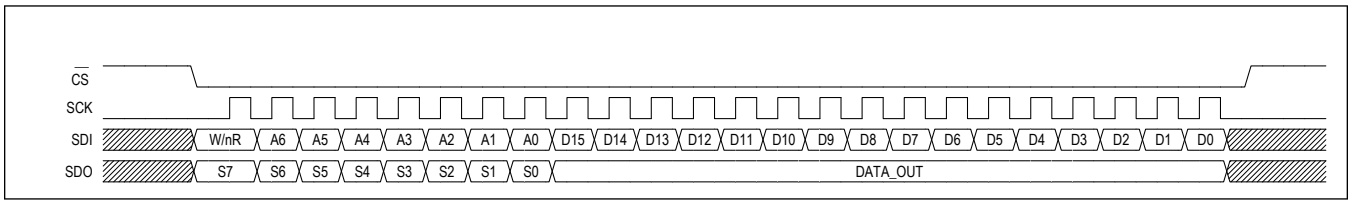


Figure 11. SPI Datagram without CRC

The SPI input data transfer consists of a 24 bit word: 8 bits for the address and a W/R bit plus 16 bits of data.

SPI transactions with CRC error detection.

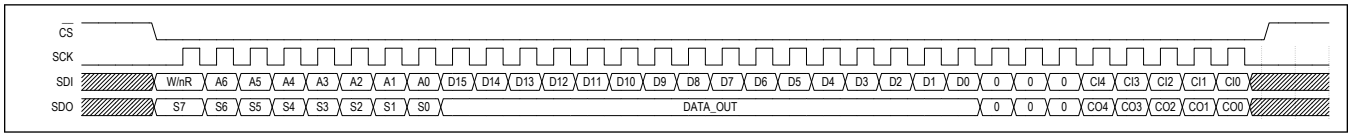


Figure 12. SPI Datagram with CRC

The SPI input data transfer consists of 32 bits: 8 bits for the address and W/R bit, 16 bits of data, and 8 bits of FCS. The CRC error detection is just enabled if the CRC_EN pin is high.

For more information about CRC error detection, see the *CRC Error Detection on the Serial Interface* section.

SPI Data

The SPI bitfields are the following:

- W/nR: Is 1 for a Write command, and it is 0 for a Read command.
- A[6:0]: Address
- D[15:0]: Input data (can be X for a read)
- S[7:0]: Status data
  - S[7] - OVT
  - S[6] - OCP
  - S[5] - OLF
  - S[4] - COMER
  - S[3] - UVM
  - S[2] - DPM

- S[1] - STAT1
- S[0] - STAT0

- DATA_OUT: Output data (it depends on the previous command).
  - If the previous command was a write, DATA_OUT will contain the D[15:0] data sent in the previous command.

    If the previous command was a read, DATA_OUT will contain the register map data at the A[6:0] address sent in the previous command.

A read access request uses dummy write data. Read data is transferred back to the master with subsequent read or write access. Hence, reading multiple registers can be done in a pipelined fashion.

Example:

ACTION	DATA SENT ON SDI	DATA RECEIVED ON SDO
Read register 0x21 (send command)	0x21XXXX	0xSS, unused_data
Read register 0x21 (receive data)	0x21XXXX	0xSS, data_register_21
Write 0x1234 to register 0x10	0x901234	0xSS, data_register_21
Write 0x5678 to register 0x10	0x905678	0xSS1234

SS - Status data

CRC Error Detection on the Serial Interface

CRC error detection on the serial interface CRC error detection of the serial data can be enabled to minimize incorrect operation/misinformation due to data corruption of the SDI/SDO signals.

The CRC Error Detection can be enabled by setting the CRC_EN input logic high.

If error detection is enabled, then the MAX22216/MAX22217:

1. Performs error detection on the SDI data that it receives from the controller, and
2. Calculates a CRC on the SDO data and appends a check byte to the SDO diagnostics/status data that it sends to the controller.

This ensures that both the data that it receives from the controller (setting/configuration) and the data that it sends to the controller (diagnostics/status) have a low likelihood of undetected errors. Setting the CRCEN input high enables CRC error detection. A CRC Frame Check Sequence (FCS) is then sent along with each serial transaction. The 5-bit FCS is based on the generator polynomial X5 + X4 + X2 + 1 with a CRC starting value = 11111. When CRC is enabled, the MAX22216/MAX22217 expect a check byte appended to the SDI program/configure data that it receives. The check byte has the following format:

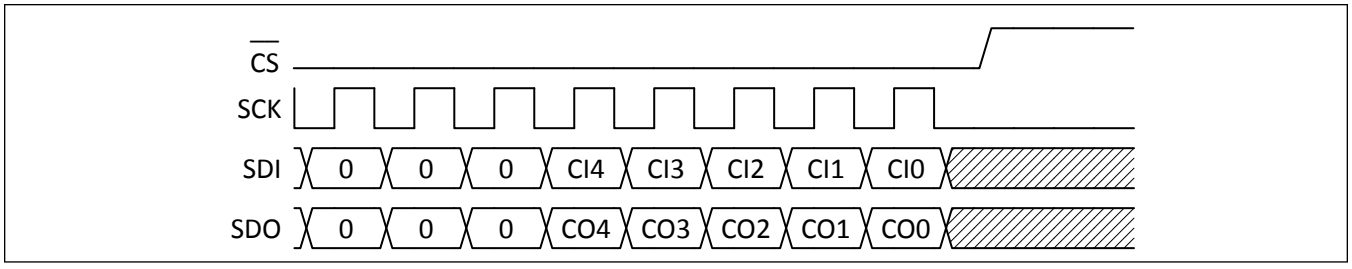


Figure 13. CRC byte

The five FCS bits (CIx / COx) are calculated on all the data sent in one SPI command, including the three “0” in the MSBs of the check byte. Therefore, the CRC is calculated from 19 bits. CI0 is the LSB of the FCS. The MAX22216/MAX22217 verify the received FCS. If no error is detected, the MAX22216/MAX22217 changes configuration per the SDI data. If a CRC error is detected, then the MAX22216/MAX22217 do not change the configuration. Instead, the MAX22216/MAX22217 set the COMER bit of the status byte of the next SPI transmission high.

If multiple MAX22216/MAX22217 are connected in a daisy chain, the FCS bits for a specific MAX22216/MAX22217 in a chain are calculated just on the data that has been sent to this specific MAX22216/MAX22217. Each MAX22216/

MAX22217 in a daisy chain is sent an FCS byte calculated independently from the data that has been sent to the other MAX22216/MAX22217. CRC error detection has to be consistently enabled or disabled within a daisy chain of the MAX22216/MAX22217.

One-Time Programmable (OTP)

The configuration settings can be programmed as power-on default by writing one-time programming registers (OTPs). The user can write OTPs registers in production according to his specific needs and verify their content by reading them back through SPI. Once the configuration settings are written into OTP registers, the MAX22216/MAX22217 can be operated by means of logic input signals (CNTL) without the need of SPI control. This operating mode is referred as “stand-alone mode”.

The default values of every functional register in the RegMap can possibly be written in the OTP Memory bank. Typically, for stand-alone applications, only a subset of RegMap registers needs to be OTP programmed.

To enter OTP programming mode, the specific SPI command 0xF12A7 needs to be issued (see the *OTP Programming* section). This command gives access to the OTP Controller registers: OTP_CONTROL(0x68), OTP_STATUS (0x69), OTP_DATA0 (0x7A), OTP_DATA1 (0x7B), and OTP_ADDR (0x7C). Similarly to the functional register case, the SPI transfer to the OTP controller register consists of a 24-bit word: 8 bits for the address and the W/R bit plus 16 bits of data.

OTP Programming

The OTP writing procedure must be executed in a controlled environment. It is normally operated in a factory under well-controlled temperature and voltage conditions.

For safe OTP writing, the following conditions must be fulfilled:

Programming Temp: 25°C ± 10°C

Programming Voltage (V_M): 8.7 ± 0.13V (1.5%)

The OTP writing procedure is as follows:

1. Power up the MAX22216/MAX22217 with V_M at the programming voltage (8.7V).
2. Drive CRC_EN = 0.
3. Activate the device by setting high the bit ACTIVE in the GLOBAL_CFG register (0x01). All the remaining bits can be set at zero.
4. To enter the OTP programming mode, send an SPI command equal to 0xFD12A7.
5. To send a second SPI command 0xF8001B to prepare the OTP controller.
6. Write the address of the functional register that you want to program into the OTP_ADDR register (0x7C).
7. Write the Least Significant Data Byte into the OTP_DATA0 register (0x7A). This will become the Least Significant Data Byte Default value at power-up for that specific register.
8. Write the Most Significant Data Byte into the OTP_DATA1 register (0x7B). This will become the Most Significant Data Byte Default value at power-up for that specific register.
9. To start programming, write the Start Programming bit (SRT_PROG) of the register OTP_CONTROL (0x68) with the remaining bits set at zero.
10. Poll the register OTP_STATUS (0x69) until you see the DONE bit equal to one. If you find other bits equal to one, it means that something failed during programming, and hence the OTP content is corrupted.
11. If everything is ok, repeat steps 6–10 for the next Functional Register that you want to program. If a problem occurs at step 8, you can retry the procedure (steps 6–10) for the same Functional Register (see Note 1).
12. To verify if the whole process was successful, do a power cycle and read back the default values of the Functional Registers that you have programmed. In case of errors, you can re-program the failed register by repeating steps 6–10 (see Note 1).

Note 1: When a writing cycle (steps 6-10) does not succeed and failures are found at step 10 or step 12, one register of the OTP memory bank becomes unusable. Since the size of the OTP memory bank is limited, you have a limited number of extra OTP write cycle attempts, including successful and unsuccessful attempts.

It is also possible to "lock" the OTP memory bank and avoid further attempts to write OTPs. Once all records' data have been written, the user can write a record with MTP_ADDR = 0x41 and MTP_DATA = 0xA5A5 and reboot the device. Doing that, no further programming session of the part will be possible. This prevents the final user from modifying the factory-programmed settings.

Wake-Up Time for OTP Download at Power-Up

At power-up, the content of the OTP memory bank must be downloaded into the volatile register bank.

The total wake-up time (T_{WU}) is the sum of a fixed contribution and a variable contribution. The variable contribution is due to the download of the OTP memory and depends on the total number of OTP registers that have been pre-programmed. In formula:

$$T_{WU} = T_{FW} + T_{VWU} \times N_{OTP}$$

Where T_{FW} denotes the fixed wake-up time and T_{VWU} denotes the variable wake-up time (see the *Electrical Characteristic* table), and N_{OTP} is the number of RegMap registers whose default value has been pre-programmed into OTP registers.

Register Map

FUNCTIONAL REGISTERS

Functional registers can be addressed directly via SPI.

The default values of these registers can be written in non-volatile memory (OTP) (see the OTP Programming section).

ADDRESS	NAME	MSB							LSB
GLOBAL REGISTERS									
0x00	GLOBAL_CTRL[15:8]	–	–	–	–	–	–	–	–
	GLOBAL_CTRL[7:0]	F_PWM_M[3:0]				CNTL3	CNTL2	CNTL1	CNTL0
0x01	GLOBAL_CFG[15:8]	ACTIVE	M_OVT	M_OCP	M_OLF	M_HHF	M_DPM	M_COMF	M_UVM
	GLOBAL_CFG[7:0]	CNTL_POL	STAT_POL	–	VDRnVDRDUTY	CHS[3:0]			
0x02	STATUS[15:8]	–	STT3	STT2	STT1	STT0	MIN_T_ON	RES	IND
	STATUS[7:0]	OVT	OCP	OLF	HHF	DPM	COMER	UVM	RFU
0x03	STATUS_CFG[15:8]	–	–	–	–	–	–	M_UVM_CMP	V5_nV3
	STATUS_CFG[7:0]	EN_LDO	STRETCH_EN[1:0]		STAT_SEL1	STAT_SEL0	STAT_FUN[2:0]		
0x04	DC_H2L[15:8]	DC_H2L[15:8]							
	DC_H2L[7:0]	DC_H2L[7:0]							
0x05	VM_MONITOR[15:8]	–	–	–	VM_MONITOR[12:8]				
	VM_MONITOR[7:0]	VM_MONITOR[7:0]							
0x06	VM_THRESHOLD[15:8]	–	–	–	–	–	–	–	–
	VM_THRESHOLD[7:0]	VM_THLD_UP[3:0]				VM_THLD_DOWN[3:0]			
0x07	F_AC[15:8]	–	–	–	–	F_AC_SCAN[11:8]			
	F_AC[7:0]	F_AC_SCAN[7:0]							
0x08	U_AC_SCAN[15:8]	–	U_AC_SCAN[14:8]						
	U_AC_SCAN[7:0]	U_AC_SCAN[7:0]							
CONFIGURATION REGISTERS CH 0									
0x09	CFG_DC_L2H[15:8]	DC_L2H_0[15:8]							
	CFG_DC_L2H[7:0]	DC_L2H_0[7:0]							
0x0A	CFG_DC_H[15:8]	DC_H_0[15:8]							
	CFG_DC_H[7:0]	DC_H_0[7:0]							
0x0B	CFG_DC_L[15:8]	DC_L_0[15:8]							
	CFG_DC_L[7:0]	DC_L_0[7:0]							
0x0C	CFG_L2H_TIME[15:8]	TIME_L2H_0[15:8]							
	CFG_L2H_TIME[7:0]	TIME_L2H_0[7:0]							
0x0D	CFG_CTRL0[15:8]	CTRL_MODE_0[1:0]		HHF_EN_0	OL_EN_0	H2L_EN_0	RDWE_0	RMDE_0	RUPE_0
	CFG_CTRL0[7:0]	RAMP_0[7:0]							
0x0E	CFG_CTRL1[15:8]	–	–	–	–	–	HSnLS_0	F_PWM_0[1:0]	

ADDRESS	NAME	MSB							LSB
	CFG_CTRL1[7:0]	T_BLANKING_0[1:0]		SLEW_RATE_0[1:0]		GAIN[1:0]		SNSF[1:0]	
0x0F	CFG_DPM0[15:8]	–	–	–	–	DPM_THLD_0[11:8]			
	CFG_DPM0[7:0]	DPM_THLD_0[7:0]							
0x10	CFG_DPM1[15:8]	–	DPM_EN_0	END_HIT_TO_HIZ_AUTO_0	END_HIT_AUTO_0	DPM_MIN_NBR_0[3:0]			
	CFG_DPM1[7:0]	DPM_START[7:0]							
0x11	CFG_IDC_THLD[15:8]	IDC_THLD_0[15:8]							
	CFG_IDC_THLD[7:0]	IDC_THLD_0[7:0]							
0x12	CFG_R_THLD[15:8]	RES_THLD_0[15:8]							
	CFG_R_THLD[7:0]	RES_THLD_0[7:0]							
0x13	CFG_IND_0[15:8]	–	–	–	–	DITH_EN_0	L_MEAS_EN_0	L_MEAS_L2H_0	L_MEAS_H_0
	CFG_IND_0[7:0]	L_MEAS_WCYCLES_0[3:0]				L_NBR_CALC_0[3:0]			
0x14	CFG_IND_1[15:8]	–	–	–	–	IAC_THLD_0[11:8]			
	CFG_IND_1[7:0]	IAC_THLD_0[7:0]							
0x15	CFG_P[15:8]	CFG_P_0[15:8]							
	CFG_P[7:0]	CFG_P_0[7:0]							
0x16	CFG_I[15:8]	CFG_I_0[15:8]							
	CFG_I[7:0]	CFG_I_0[7:0]							
CONFIGURATION REGISTERS CH 1									
0x17	CFG_DC_L2H[15:8]	DC_L2H_1[15:8]							
	CFG_DC_L2H[7:0]	DC_L2H_1[7:0]							
0x18	CFG_DC_H[15:8]	DC_H_1[15:8]							
	CFG_DC_H[7:0]	DC_H_1[7:0]							
0x19	CFG_DC_L[15:8]	DC_L_1[15:8]							
	CFG_DC_L[7:0]	DC_L_1[7:0]							
0x1A	CFG_L2H_TIME[15:8]	TIME_L2H_1[15:8]							
	CFG_L2H_TIME[7:0]	TIME_L2H_1[7:0]							
0x1B	CFG_CTRL0[15:8]	CTRL_MODE_1[1:0]		HHF_EN_1	OL_EN_1	H2L_EN_1	RDWE_1	RMDE_1	RUPE_1
	CFG_CTRL0[7:0]	RAMP_1[7:0]							
0x1C	CFG_CTRL1[15:8]	–	–	–	–	–	HSnLS_1	F_PWM_1[1:0]	
	CFG_CTRL1[7:0]	T_BLANKING_1[1:0]		SLEW_RATE_1[1:0]		GAIN[1:0]		SNSF[1:0]	
0x1D	CFG_DPM0[15:8]	–	–	–	–	DPM_THLD_1[11:8]			
	CFG_DPM0[7:0]	DPM_THLD_1[7:0]							
0x1E	CFG_DPM1[15:8]	–	DPM_EN_1	END_HIT_TO_HIZ_AUTO_1	END_HIT_AUTO_1	DPM_MIN_NBR_1[3:0]			
	CFG_DPM1[7:0]	DPM_START[7:0]							
0x1F	CFG_IDC_THLD[15:8]	IDC_THLD_1[15:8]							
	CFG_IDC_THLD[7:0]	IDC_THLD_1[7:0]							

ADDRESS	NAME	MSB							LSB
0x20	CFG_R_THLD[15:8]	RES_THLD_1[15:8]							
	CFG_R_THLD[7:0]	RES_THLD_1[7:0]							
0x21	CFG_IND_0[15:8]	–	–	–	–	DITH_EN_1	L_MEAS_EN_1	L_MEAS_L2H_1	L_MEAS_H_1
	CFG_IND_0[7:0]	L_MEAS_WCYCLES_1[3:0]				L_NBR_CALC_1[3:0]			
0x22	CFG_IND_1[15:8]	–	–	–	–	IAC_THLD_1[11:8]			
	CFG_IND_1[7:0]	IAC_THLD_1[7:0]							
0x23	CFG_P[15:8]	CFG_P_1[15:8]							
	CFG_P[7:0]	CFG_P_1[7:0]							
0x24	CFG_I[15:8]	CFG_I_1[15:8]							
	CFG_I[7:0]	CFG_I_1[7:0]							
CONFIGURATION REGISTERS CH 2									
0x25	CFG_DC_L2H[15:8]	DC_L2H_2[15:8]							
	CFG_DC_L2H[7:0]	DC_L2H_2[7:0]							
0x26	CFG_DC_H[15:8]	DC_H_2[15:8]							
	CFG_DC_H[7:0]	DC_H_2[7:0]							
0x27	CFG_DC_L[15:8]	DC_L_2[15:8]							
	CFG_DC_L[7:0]	DC_L_2[7:0]							
0x28	CFG_L2H_TIME[15:8]	TIME_L2H_2[15:8]							
	CFG_L2H_TIME[7:0]	TIME_L2H_2[7:0]							
0x29	CFG_CTRL0[15:8]	CTRL_MODE_2[1:0]		HHF_EN_2	OL_EN_2	H2L_EN_2	RDWE_2	RMDE_2	RUPE_2
	CFG_CTRL0[7:0]	RAMP_2[7:0]							
0x2A	CFG_CTRL1[15:8]	–	–	–	–	–	HSnLS_2	F_PWM_2[1:0]	
	CFG_CTRL1[7:0]	T_BLANKING_2[1:0]		SLEW_RATE_2[1:0]		GAIN[1:0]		SNSF[1:0]	
0x2B	CFG_DPM0[15:8]	–	–	–	–	DPM_THLD_2[11:8]			
	CFG_DPM0[7:0]	DPM_THLD_2[7:0]							
0x2C	CFG_DPM1[15:8]	–	DPM_EN_2	END_HIT_TO_HIZ_AUTO_2	END_HIT_AUTO_2	DPM_MIN_NBR_2[3:0]			
	CFG_DPM1[7:0]	DPM_START[7:0]							
0x2D	CFG_IDC_THLD[15:8]	IDC_THLD_2[15:8]							
	CFG_IDC_THLD[7:0]	IDC_THLD_2[7:0]							
0x2E	CFG_R_THLD[15:8]	RES_THLD_2[15:8]							
	CFG_R_THLD[7:0]	RES_THLD_2[7:0]							
0x2F	CFG_IND_0[15:8]	–	–	–	–	DITH_EN_2	L_MEAS_EN_2	L_MEAS_L2H_2	L_MEAS_H_2
	CFG_IND_0[7:0]	L_MEAS_WCYCLES_2[3:0]				L_NBR_CALC_2[3:0]			
0x30	CFG_IND_1[15:8]	–	–	–	–	IAC_THLD_2[11:8]			
	CFG_IND_1[7:0]	IAC_THLD_2[7:0]							
0x31	CFG_P[15:8]	CFG_P_2[15:8]							
	CFG_P[7:0]	CFG_P_2[7:0]							

ADDRESS	NAME	MSB							LSB
0x32	CFG_I[15:8]	CFG_I_2[15:8]							
	CFG_I[7:0]	CFG_I_2[7:0]							
CONFIGURATION REGISTERS CH 3									
0x33	CFG_DC_L2H[15:8]	DC_L2H_3[15:8]							
	CFG_DC_L2H[7:0]	DC_L2H_3[7:0]							
0x34	CFG_DC_H[15:8]	DC_H_3[15:8]							
	CFG_DC_H[7:0]	DC_H_3[7:0]							
0x35	CFG_DC_L[15:8]	DC_L_3[15:8]							
	CFG_DC_L[7:0]	DC_L_3[7:0]							
0x36	CFG_L2H_TIME[15:8]	TIME_L2H_3[15:8]							
	CFG_L2H_TIME[7:0]	TIME_L2H_3[7:0]							
0x37	CFG_CTRL0[15:8]	CTRL_MODE_3[1:0]		HHF_EN_3	OL_EN_3	H2L_EN_3	RDWE_3	RMDE_3	RUPE_3
	CFG_CTRL0[7:0]	RAMP_3[7:0]							
0x38	CFG_CTRL1[15:8]	–	–	–	–	–	HSnLS_3	F_PWM_3[1:0]	
	CFG_CTRL1[7:0]	T_BLANKING_3[1:0]		SLEW_RATE_3[1:0]		GAIN[1:0]		SNSF[1:0]	
0x39	CFG_DPM0[15:8]	–	–	–	–	DPM_THLD_3[11:8]			
	CFG_DPM0[7:0]	DPM_THLD_3[7:0]							
0x3A	CFG_DPM1[15:8]	–	DPM_EN_3	END_HIT_TO_HIZ_AUTO_3	END_HIT_AUTO_3	DPM_MIN_NBR_3[3:0]			
	CFG_DPM1[7:0]	DPM_START[7:0]							
0x3B	CFG_IDC_THLD[15:8]	IDC_THLD_3[15:8]							
	CFG_IDC_THLD[7:0]	IDC_THLD_3[7:0]							
0x3C	CFG_R_THLD[15:8]	RES_THLD_3[15:8]							
	CFG_R_THLD[7:0]	RES_THLD_3[7:0]							
0x3D	CFG_IND_0[15:8]	–	–	–	–	DITH_EN_3	L_MEAS_EN_3	L_MEAS_L2H_3	L_MEAS_H_3
	CFG_IND_0[7:0]	L_MEAS_WCYCLES_3[3:0]				L_NBR_CALC_3[3:0]			
0x3E	CFG_IND_1[15:8]	–	–	–	–	IAC_THLD_3[11:8]			
	CFG_IND_1[7:0]	IAC_THLD_3[7:0]							
0x3F	CFG_P[15:8]	CFG_P_3[15:8]							
	CFG_P[7:0]	CFG_P_3[7:0]							
0x40	CFG_I[15:8]	CFG_I_3[15:8]							
	CFG_I[7:0]	CFG_I_3[7:0]							
DIAGNOSTICS_CH 0									
0x41	I_DPM_PEAK[15:8]	I_DPM_PEAK_0[15:8]							
	I_DPM_PEAK[7:0]	I_DPM_PEAK_0[7:0]							
0x42	I_DPM_VALLEY[15:8]	I_DPM_VALLEY_0[15:8]							
	I_DPM_VALLEY[7:0]	I_DPM_VALLEY_0[7:0]							
0x43	TRAVEL_TIME[15:8]	TRAVEL_TIME[15:8]							
	TRAVEL_TIME[7:0]	TRAVEL_TIME[7:0]							

ADDRESS	NAME	MSB							LSB
0x44	REACTION_TIME[15:8]	REACTION_TIME_0[15:8]							
	REACTION_TIME[7:0]	REACTION_TIME_0[7:0]							
0x45	I_MONITOR[15:8]	I_MONITOR_0[15:8]							
	I_MONITOR[7:0]	I_MONITOR_0[7:0]							
0x47	I_AC[15:8]	I_AC_0[15:8]							
	I_AC[7:0]	I_AC_0[7:0]							
0x48	RES[15:8]	RES[15:8]							
	RES[7:0]	RES[7:0]							
0x49	PWM_DUTY[15:8]	PWM_DUTYCYCLE_0[15:8]							
	PWM_DUTY[7:0]	PWM_DUTYCYCLE_0[7:0]							
DIAGNOSTICS_CH 1									
0x4A	I_DPM_PEAK[15:8]	I_DPM_PEAK_1[15:8]							
	I_DPM_PEAK[7:0]	I_DPM_PEAK_1[7:0]							
0x4B	I_DPM_VALLEY[15:8]	I_DPM_VALLEY_1[15:8]							
	I_DPM_VALLEY[7:0]	I_DPM_VALLEY_1[7:0]							
0x4C	TRAVEL_TIME[15:8]	TRAVEL_TIME[15:8]							
	TRAVEL_TIME[7:0]	TRAVEL_TIME[7:0]							
0x4D	REACTION_TIME[15:8]	REACTION_TIME_1[15:8]							
	REACTION_TIME[7:0]	REACTION_TIME_1[7:0]							
0x4E	I_MONITOR[15:8]	I_MONITOR_1[15:8]							
	I_MONITOR[7:0]	I_MONITOR_1[7:0]							
0x50	I_AC[15:8]	I_AC_1[15:8]							
	I_AC[7:0]	I_AC_1[7:0]							
0x51	RES[15:8]	RES[15:8]							
	RES[7:0]	RES[7:0]							
0x52	PWM_DUTY[15:8]	PWM_DUTYCYCLE_1[15:8]							
	PWM_DUTY[7:0]	PWM_DUTYCYCLE_1[7:0]							
DIAGNOSTICS_CH 2									
0x53	I_DPM_PEAK[15:8]	I_DPM_PEAK_2[15:8]							
	I_DPM_PEAK[7:0]	I_DPM_PEAK_2[7:0]							
0x54	I_DPM_VALLEY[15:8]	I_DPM_VALLEY_2[15:8]							
	I_DPM_VALLEY[7:0]	I_DPM_VALLEY_2[7:0]							
0x55	TRAVEL_TIME[15:8]	TRAVEL_TIME[15:8]							
	TRAVEL_TIME[7:0]	TRAVEL_TIME[7:0]							
0x56	REACTION_TIME[15:8]	REACTION_TIME_2[15:8]							
	REACTION_TIME[7:0]	REACTION_TIME_2[7:0]							
0x57	I_MONITOR[15:8]	I_MONITOR_2[15:8]							
	I_MONITOR[7:0]	I_MONITOR_2[7:0]							
0x59	I_AC[15:8]	I_AC_2[15:8]							
	I_AC[7:0]	I_AC_2[7:0]							
0x5A	RES[15:8]	RES[15:8]							
	RES[7:0]	RES[7:0]							

ADDRESS	NAME	MSB							LSB
0x5B	PWM_DUTY[15:8]	PWM_DUTYCYCLE_2[15:8]							
	PWM_DUTY[7:0]	PWM_DUTYCYCLE_2[7:0]							
DIAGNOSTICS_CH 3									
0x5C	I_DPM_PEAK[15:8]	I_DPM_PEAK_3[15:8]							
	I_DPM_PEAK[7:0]	I_DPM_PEAK_3[7:0]							
0x5D	I_DPM_VALLEY[15:8]	I_DPM_VALLEY_3[15:8]							
	I_DPM_VALLEY[7:0]	I_DPM_VALLEY_3[7:0]							
0x5E	TRAVEL_TIME[15:8]	TRAVEL_TIME[15:8]							
	TRAVEL_TIME[7:0]	TRAVEL_TIME[7:0]							
0x5F	REACTION_TIME[15:8]	REACTION_TIME_3[15:8]							
	REACTION_TIME[7:0]	REACTION_TIME_3[7:0]							
0x60	I_MONITOR[15:8]	I_MONITOR_3[15:8]							
	I_MONITOR[7:0]	I_MONITOR_3[7:0]							
0x62	I_AC[15:8]	I_AC_3[15:8]							
	I_AC[7:0]	I_AC_3[7:0]							
0x63	RES[15:8]	RES[15:8]							
	RES[7:0]	RES[7:0]							
0x64	PWM_DUTY[15:8]	PWM_DUTYCYCLE_3[15:8]							
	PWM_DUTY[7:0]	PWM_DUTYCYCLE_3[7:0]							
FAULT LOG									
0x65	FAULT0[15:8]	DPM3	DPM2	DPM1	DPM0	OLF3	OLF2	OLF1	OLF0
	FAULT0[7:0]	HHF3	HHF2	HHF1	HHF0	OCP3	OCP2	OCP1	OCP0
0x66	FAULT1[15:8]	–	–	–	–	–	RES3	RES2	RES1
	FAULT1[7:0]	RES0	OVT	COMER	UVM	IND3	IND2	IND1	IND0

Register Details

GLOBAL_CTRL (0x00)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	F_PWM_M[3:0]				CNTL3	CNTL2	CNTL1	CNTL0
Reset								
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
F_PWM_M	7:4	Master chopping frequency	0x0: 100kHz 0x1: 80kHz 0x2: 60kHz 0x3: 50kHz 0x4: 40kHz 0x5: 30kHz 0x6: 25kHz 0x7: 20kHz 0x8: 15kHz 0x9: 10kHz 0xA: 7.5kHz 0xB: 5kHz 0xC: 2.5kHz
CNTL3	3	Used to control the corresponding channel depending on the CHS register field of the GLOBAL_CFG register. See Table 2 and Table 3 for more information.	0x0: Disable the channel 0x1: Enable the channel
CNTL2	2	Used to control the corresponding channel depending on the CHS register field of the GLOBAL_CFG register. See Table 2 and Table 3 for more information.	0x0: Disable the channel 0x1: Enable the channel
CNTL1	1	Used to control the corresponding channel depending on the CHS register field of the GLOBAL_CFG register. See Table 2 and Table 3 for more information.	0x0: Disable the channel 0x1: Enable the channel
CNTL0	0	Used to control the corresponding channel depending on the CHS register field of the GLOBAL_CFG register. See Table 2 and Table 3 for more information.	0x0: Disable the channel 0x1: Enable the channel

GLOBAL_CFG (0x01)

BIT	15	14	13	12	11	10	9	8
Field	ACTIVE	M_OVT	M_OCP	M_OLF	M_HHF	M_DPM	M_COMF	M_UVM
Reset								
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	CNTL_POL	STAT_POL	–	VDRnVDRDUTY	CHS[3:0]			
Reset			–					
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ACTIVE	15	Enable bit to activate the part	0x0: Disable part, low-power mode is active 0x1: Enable part
M_OVT	14	Masks overtemperature detection for FAULT pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin

BITFIELD	BITS	DESCRIPTION	DECODE
M_OCP	13	Masks overcurrent protection for $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
M_OLF	12	Masks open-load detection for $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
M_HHF	11	Masks hit current not reached error for the $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
M_DPM	10	Masks the DPM error for the $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
M_COMF	9	Masks the COMF error for the $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
M_UVM	8	Masks the UVM detection for the $\overline{\text{FAULT}}$ pin	0x0: Unmask detection for $\overline{\text{FAULT}}$ pin 0x1: Mask detection for $\overline{\text{FAULT}}$ pin
CNTL_POL	7	Polarity of control pins	0x0: Control pins are active-high 0x1: Control pins are active-low
STAT_POL	6	Configures polarity of status pins	0x0: Pin is active-high 0x1: Pin is active-low
VDRnVDRDUTY	4	When set Logic High, L2H, DC_H, and DC_L registers for each channel indicate a voltage level in voltage mode. When set Logic Low, L2H, DC_H, and DC_L registers for each channel indicate a duty cycle in voltage mode. This bit does not have any effect in current mode (CDR).	0x0: Compensation of V_M is turned off 0x1: Compensation of V_M is turned on
CHS	3:0	Hardware Configuration Settings. See Table 1, Table 2, and Table 3 for more information.	0x0: Four individual half-bridges. Either connected to V_M or to GND 0x1: Three half-bridges in parallel. One half-bridge independent 0x2: Two half-bridges in parallel. Two half-bridges independent 0x3: Two half-bridges in parallel. Two half-bridges independent 0x4: Four half-bridges in parallel 0x5: Two independent full bridges 0x6: One independent full bridge. Two independent half bridges 0x7: One independent full bridge. Two half-bridges in parallel 0x8: One parallel full-bridge

STATUS (0x02)

BIT	15	14	13	12	11	10	9	8
Field	–	STT3	STT2	STT1	STT0	MIN_T_ON	RES	IND
Reset	–							
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
BIT	7	6	5	4	3	2	1	0
Field	OVT	OCP	OLF	HHF	DPM	COMER	UVM	RFU
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
STT3	14	Status bit See Table 9	
STT2	13	Status bit See Table 9	
STT1	12	Status bit See Table 9	
STT0	11	Status bit See Table 9	
MIN_T_ON	10	Read-Only Status bit. All channels combined.	0x0: MIN_T_ON is compliant 0x1: MIN_T_ON is not compliant
RES	9	Read-Only bit of resistance measurement. All channels combined.	0x0: Measured resistance is compliant 0x1: Measured resistance is not compliant
IND	8	Read-Only bit of inductance measurement. All channels combined.	0x0: Measured inductance is compliant 0x1: Measured inductance is not compliant
OVT	7	Read-Only bit of overtemperature measurement.	0x0: No over temperature detected 0x1: Over temperature detected
OCP	6	Read-Only bit of overcurrent protection. All channels combined.	0x0: No overcurrent detected 0x1: Overcurrent detected
OLF	5	Read-Only bit of open-load detection. All channels combined.	0x0: No open-loop detected 0x1: Open-loop detected
HHF	4	Read-Only bit of hit current not reached function. All channels combined.	0x0: Hit current is reached 0x1: Hit current is not reached
DPM	3	Read-Only bit of detection of plunger movement status. All channels combined.	0x0: Plunger moved 0x1: Plunger did not move
COMER	2	Read-Only bit of detection of SPI communication error.	0x0: No communication error detected 0x1: Communication error detected
UVM	1	Read-Only bit of detection of under voltage status.	0x0: No undervoltage detected 0x1: Undervoltage detected
RFU	0	Reserved for future use	

STATUS_CFG (0x03)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	M_UVM_CMP	V5_nV3
Reset	–	–	–	–	–	–		
Access Type	–	–	–	–	–	–	Write, Read	Read Only

BIT	7	6	5	4	3	2	1	0
Field	EN_LDO	STRETCH_EN[1:0]		STAT_SEL1	STAT_SEL0	STAT_FUN[2:0]		
Reset								
Access Type	Read Only	Write, Read		Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
M_UVM_CMP	9	Mask stretched UVM information on the FAULT pin	0x0: Unmask UVM to FAULT pin 0x1: Mask UVM to FAULT pin

BITFIELD	BITS	DESCRIPTION	DECODE
V5_nV3	8	Internal LDO voltage	0x0: 3.3V 0x1: 5V
EN_LDO	7	Enable of the internal LDO on V_{IO} pin	0x0: Disable internal LDO on V_{IO} 0x1: Enable internal LDO on V_{IO}
STRETCH_EN	6:5	Stretch the fault indicator pin duration for UVM and OVT faults. See Table 9.	0x0: No stretch 0x1: 1s 0x2: 2s 0x3: 3s
STAT_SEL1	4	Used to select the channel that drives the status pins. See Table 8.	0x0: Use STAT2 bit of STATUS register to drive STAT1 pin 0x1: Use STAT3 bit of STATUS register to drive STAT1 pin
STAT_SEL0	3	Used to select the channel that drives the status pins. See Table 8.	0x0: Use STAT0 bit of STATUS register to drive STAT0 pin 0x1: Use STAT1 bit of STATUS register to drive STAT0 pin
STAT_FUN	2:0	Configuration of the value that drives the status pins. See Table 9.	0x0: Status detection based on inductance measurement 0x1: PWM monitor 0x2: Status detection based on resistance measurement 0x3: Status detection based on DPM 0x4: Status detection based on VM detection 0x5: Status detection based on I_MONITOR measurement

DC_H2L (0x04)

BIT	15	14	13	12	11	10	9	8
Field	DC_H2L[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DC_H2L[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DC_H2L	15:0	Demagnetization Voltage Setting (Global) Used to configure the demagnetization voltage of high to low time in bridge-tied-load configurations if the H2L_EN bit is set. Depending on the VDR_nDUTY bit, it either configures a voltage or a duty cycle. DC_H2L indicates a Voltage if VDRnVDRDUTY = "1". The voltage value is VOUT (V) = K_{VDR} x 36 x DC_H2L [15:0]$_{DEC}$. DC_H2L indicates a Duty Cycle if VDRnVDRDUTY = "0". The voltage value is VOUT (V) = K_{VDR} x VM x DC_H2L [15:0]$_{DEC}$.

VM_MONITOR (0x05)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	VM_MONITOR[12:8]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BIT	7	6	5	4	3	2	1	0
Field	VM_MONITOR[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VM_MONITOR	12:0	VM Measurement: VM = K_{VM} x VM_MONITOR[15:0]

VM_THRESHOLD (0x06)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	VM_THLD_UP[3:0]				VM_THLD_DOWN[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VM_THLD_UP	7:4	Rising Edge VM Threshold (from 1 to 15) 4.5V-34.5V steps 2V	0x0: disable 0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8 0x9 0xA 0xB 0xC 0xD 0xE 0xF

BITFIELD	BITS	DESCRIPTION	DECODE
VM_THLD_DOWN	3:0	Falling Edge VM Threshold 4-36V in 2V steps	0x0: disable 0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8 0x9 0xA 0xB 0xC 0xD 0xE 0xF

F_AC (0x07)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	F_AC_SCAN[11:8]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	F_AC_SCAN[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
F_AC_SCAN	11:0	Defines the carrier frequency that is used for the AC scan signal of the inductance measurement: F_AC = F_PWM_M * (F_AC_SCAN[11:0]$_{DEC}$/65535)

U_AC_SCAN (0x08)

BIT	15	14	13	12	11	10	9	8
Field	–	U_AC_SCAN[14:8]						
Reset	–							
Access Type	–	Write, Read						

BIT	7	6	5	4	3	2	1	0
Field	U_AC_SCAN[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
U_AC_SCAN	14:0	Defines the amplitude of the AC signal used for the inductance measurement or for dithering. VDR: VAC(V) = K_{VDR} x 36 x U_AC_SCAN[14:0]$_{DEC}$ VDRDUTY: VAC (V) = K_{VDR} x VM x U_AC_SCAN[14:0]$_{DEC}$ CDR Mode: IAC (mA) = K_{CDR} x GAIN x SNSF x U_AC[14:0]$_{DEC}$

CFG_DC_L2H (0x09, 0x17, 0x25, 0x33)

BIT	15	14	13	12	11	10	9	8
Field	DC_L2H[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DC_L2H[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DC_L2H	15:0	Sets the DC_L2H level: VDR: VOUT (V) = K_{VDR} x 36 x DC_L2H[15:0]$_{DEC}$ VDRDUTY: VOUT (V) = K_{VDR} x VM x DC_L2H[15:0]$_{DEC}$ CDR: IOUT (mA) = K_{CDR} x GAIN x SNSF x DC_L2H[15:0]$_{DEC}$

CFG_DC_H (0x18, 0x26, 0x34, 0xA)

BIT	15	14	13	12	11	10	9	8
Field	DC_H[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DC_H[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DC_H	15:0	Sets the DC_H level: VDR: VOUT (V) = K_{VDR} x 36 x DC_H[15:0]$_{DEC}$ VDRDUTY: VOUT (V) = K_{VDR} x VM x DC_H[15:0]$_{DEC}$ CDR: IOUT (mA) = K_{CDR} x GAIN x SNSF x DC_H[15:0]$_{DEC}$

CFG_DC_L (0x19, 0x27, 0x35, 0xB)

BIT	15	14	13	12	11	10	9	8
Field	DC_L[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DC_L[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DC_L	15:0	Sets the DC_L level: VDR: VOUT (V) = K_{VDR} x 36 x DC_L2H[15:0]$_{DEC}$ VDRDUTY: VOUT (V) = K_{VDR} x VM x DC_L2H[15:0]$_{DEC}$ CDR: IOUT (mA) = K_{CDR} x GAIN x SNSF x DC_L2H[15:0]$_{DEC}$

CFG_L2H_TIME (0x1A, 0x28, 0x36, 0xC)

BIT	15	14	13	12	11	10	9	8
Field	TIME_L2H[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TIME_L2H[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIME_L2H	15:0	Sets the TIME_L2H TIME_L2H = TIME_L2H[15:0]$_{DEC}$/F_PWM

CFG_CTRL0 (0x1B, 0x29, 0x37, 0xD)

BIT	15	14	13	12	11	10	9	8
Field	CTRL_MODE[1:0]		HHF_EN	OL_EN	H2L_EN	RDWE	RMDE	RUPE
Reset								
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	RAMP[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CTRL_MODE	15:14	CTRL_MODE defines the control scheme for DC_L2H and DC_H. Table 8 shows that VDR stands for VDR or VDRDUTY Mode, depending on the VDR_nDUTY bit.	0x0: VOLT 0x1: CDR 0x2: Limiter/VOLT 0x3: VOLT (during L2H) and CDR(during H)
HHF_EN	13	Current not reached Fault detection	0x0: Disable current not reached fault detection 0x1: Enable current not reached fault detection
OL_EN	12	Open Load Circuit Enable (enable pullup/dw)	0x0: Open-load detection disabled 0x1: Open-load detection disabled
H2L_EN	11	H2L Fast Demagnetization Enable bit. "1" enforces DC_H2L after CNTL H2L transition (For Bridge Operation only).	0x0: Disable fast demagnetization 0x1: Enable fast demagnetization
RDWE	10	Ramp Down Enable bit	0x0: Disable ramp down 0x1: Enable ramp down
RMDE	9	Ramp Mid Enable Bit	0x0: Disable mid ramp 0x1: Enable mid ramp
RUPE	8	Ramp UP enable	0x0: Disable ramp up 0x1: Enable ramp up
RAMP	7:0	RAMP[7:0] Sets the Ramp Slew Rate. **VDRDUTY:** Ramp Slew Rate (V/ms) = K_{VDR} x VM x (RAMP[7:0]$_{DEC}$ + 1) x F_PWM (kHz)) **VDR:** Ramp Slew Rate (V/ms) = K_{VDR} x 36 x (RAMP[7:0]$_{DEC}$ + 1) x F_PWM (kHz) **CDR:** Ramp Slew Rate (mA/ms) = K_{CDR} x GAIN x SNSF x (RAMP[7:0]$_{DEC}$ + 1) x F_PWM (kHz)	

CFG_CTRL1 (0x1C, 0x2A, 0x38, 0xE)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	HSnLS	F_PWM[1:0]	
Reset	–	–	–	–	–			
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	T_BLANKING[1:0]		SLEW_RATE[1:0]		GAIN[1:0]		SNSF[1:0]	
Reset								
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HSnLS	10	HS/LS: Bit Single-Ended Mode Only	0x0: Low-side driver 0x1: High-side driver
F_PWM	9:8	Defines the PWM frequency that is used for the channel. See Table 5	0x0: F_PWM_M 0x1: F_PWM_M/2 0x2: F_PWM_M/4 0x3: F_PWM_M/8

BITFIELD	BITS	DESCRIPTION	DECODE
T_BLANKING	7:6	Defines an additional blanking time for the current measurement.	0x0: 0µs 0x1: 0.96µs 0x2: 1.92µs 0x3: 2.88µs
SLEW_RATE	5:4	SRC[1:0]: Slew-rate control bits. ("10", "11" inhibited for F_PWM > 50kHz)	0x0: Fast 0x1: 200V/µs 0x2: 100V/µs 0x3: 50V/µs
GAIN	3:2	Sets a digital GAIN for the Current Driver Regulation (CDR)	0x0: Scale 1 0x1: Scale 2 0x2: Scale 3 0x3: Scale 4
SNSF	1:0	Sets the Sense Scaling Factor	0x0: Full scale 0x1: 2/3 0x2: 1/3

CFG_DPM0 (0x1D, 0x2B, 0x39, 0xF)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	DPM_THLD[11:8]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DPM_THLD[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DPM_THLD	11:0	DPM Fault Threshold: Fault is detected if the BEMF dip of the current is less than DPM_THLD(mA) = K_{CDR} x GAIN x SNSF x DPM_THLD[11:0].

CFG_DPM1 (0x10, 0x1E, 0x2C, 0x3A)

BIT	15	14	13	12	11	10	9	8
Field	–	DPM_EN	END_HIT_TO_HIZ_AUTO	END_HIT_AUTO	DPM_MIN_NBR[3:0]			
Reset	–							
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DPM_START[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DPM_EN	14	DPM enable bit	0x0: DPM disabled 0x1: DPM enabled
END_HIT_TO_HIZ_AUTO	13	Enable automatic DC_L2H to HiZ switchover	0x0: Automatic end of hit time is disabled 0x1: Automatic end of hit time is enabled
END_HIT_AUTO	12	Enable Automatic DC_L2H to DH_H switchover	0x0: Automatic end of hit time is disabled 0x1: Automatic end of hit time is enabled
DPM_MIN_NBR	11:8	In order to detect a valid BEMF dip, the condition has to be fulfilled for at least DPM_MIN_NBR*2 consecutive PWM cycles.	
DPM_START	7:0	The detection starts once the actual current has succeeded DPM_START*8.	

CFG_IDC_THLD (0x11, 0x1F, 0x2D, 0x3B)

BIT	15	14	13	12	11	10	9	8
Field	IDC_THLD[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	IDC_THLD[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
IDC_THLD	15:0	IDC_THLD thresholds IDC for mapping to status output STAT.

CFG_R_THLD (0x12, 0x20, 0x2E, 0x3C)

BIT	15	14	13	12	11	10	9	8
Field	RES_THLD[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	RES_THLD[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RES_THLD	15:0	Threshold of measured resistance that triggers the corresponding RES bits of the FAULT register or for mapping to status output STAT.

CFG_IND_0 (0x13, 0x21, 0x2F, 0x3D)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	DITH_EN	L_MEAS_EN	L_MEAS_L2H	L_MEAS_H
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	L_MEAS_WCYCLES[3:0]				L_NBR_CALC[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DITH_EN	11	Used to enable dithering function.	0x0: Dithering disabled 0x1: Dithering enabled
L_MEAS_EN	10	U_AC_SCAN is superimposed onto DC_L2H, DC_H, and DC_L if measurement is enabled.	0x0: Inductance measurement disabled 0x1: Inductance measurement enabled
L_MEAS_L2H	9	Used to enable inductance measurement during L2H excitation time.	0x0: Disabled during excitation time 0x1: Enabled during excitation time
L_MEAS_H	8	Used to enable inductance measurement during hold time.	0x0: Disabled during hold time 0x1: Enabled during hold time
L_MEAS_WCYCLES	7:4	Number of AC scan periods (Tscan/1/F_AC) starting from a L2H or H2L transition during which the inductance measurement is skipped because of unreliable measurements.	
L_NBR_CALC	3:0	Number of AC scan periods used to calculate the inductance. If L_NBR_CALC is different from zero and dithering is not enabled, AC_scan is disabled for L_NBR_CALC cycles.	

CFG_IND_1 (0x14, 0x22, 0x30, 0x3E)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	IAC_THLD[11:8]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	IAC_THLD[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
IAC_THLD	11:0	IAC_TLHD thresholds I_AC for mapping to the status output STAT. If the measured I_AC value exceeds this value, the status of the inductance measurement gets set to 1.

CFG_P (0x15, 0x23, 0x31, 0x3F)

BIT	15	14	13	12	11	10	9	8
Field	CFG_P[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	CFG_P[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CFG_P	15:0	Set the P parameter of the PI controller. The CFG_P_0 value is interpreted in Q4.12 representation. Meaning that CFG_P_0/2^12 gives the fixed point number used for the PI controller calculations.

CFG_I (0x16, 0x24, 0x32, 0x40)

BIT	15	14	13	12	11	10	9	8
Field	CFG_I[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	CFG_I[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CFG_I	15:0	Set the I parameter of the PI controller. The CFG_I_0 value is interpreted in Q4.12 representation. Meaning that CFG_I_0/2^12 gives the fixed point number used for the PI controller calculations.

I_DPM_PEAK (0x41, 0x4A, 0x53, 0x5C)

BIT	15	14	13	12	11	10	9	8
Field	I_DPM_PEAK[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I_DPM_PEAK[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I_DPM_PEAK	15:0	BEMF Current Local Peak during ramp-up. I_DPM_PEAK(mA) = K_{CDR} x GAIN x SNSF x I_DPM_PEAK[14:0]$_{DEC}$

I_DPM_VALLEY (0x42, 0x4B, 0x54, 0x5D)

BIT	15	14	13	12	11	10	9	8
Field	I_DPM_VALLEY[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I_DPM_VALLEY[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I_DPM_VALLEY	15:0	BEMF Current Local Valley during ramp-up. VDR or Duty Mode only. I_DPM_VALLEY(mA) = K_{CDR} x GAN x SNSF x I_DPM_VALLEY[14:0]$_{DEC}$

TRAVEL_TIME (0x43, 0x4C, 0x55, 0x5E)

BIT	15	14	13	12	11	10	9	8
Field	TRAVEL_TIME[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	TRAVEL_TIME[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TRAVEL_TIME	15:0	Travel time from local maximum to local minimum detection: Expressed in the number of PWM cycles.

REACTION_TIME (0x44, 0x4D, 0x56, 0x5F)

BIT	15	14	13	12	11	10	9	8
Field	REACTION_TIME[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	REACTION_TIME[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REACTION_TIME	15:0	Reaction time from CNTL L2H to local minimum detection: Expressed in number of PWM cycles

I_MONITOR (0x45, 0x4E, 0x57, 0x60)

BIT	15	14	13	12	11	10	9	8
Field	I_MONITOR[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I_MONITOR[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I_MONITOR	15:0	I_MONITOR Instantaneous sampled current. Return latest measured current sample. I_MONITOR (mA) = K_{CDR} x GAIN x SNSF x $I\_MONITOR[15:0]_{DEC}$

I_AC (0x47, 0x50, 0x59, 0x62)

BIT	15	14	13	12	11	10	9	8
Field	I_AC[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	I_AC[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
I_AC	15:0	AC current measured

RES (0x48, 0x51, 0x5A, 0x63)

BIT	15	14	13	12	11	10	9	8
Field	RES[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	RES[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RES	15:0	Measured resistance

PWM_DUTY (0x49, 0x52, 0x5B, 0x64)

BIT	15	14	13	12	11	10	9	8
Field	PWM_DUTYCYCLE[15:8]							
Reset								
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	PWM_DUTYCYCLE[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PWM_DUTYCYCLE	15:0	Duty cycle

FAULT0 (0x65)

BIT	15	14	13	12	11	10	9	8
Field	DPM3	DPM2	DPM1	DPM0	OLF3	OLF2	OLF1	OLF0
Reset								
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BIT	7	6	5	4	3	2	1	0
Field	HHF3	HHF2	HHF1	HHF0	OCP3	OCP2	OCP1	OCP0
Reset								
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DPM3	15	DPM status bit	0x0: Plunger moved 0x1: Plunger did not move

BITFIELD	BITS	DESCRIPTION	DECODE
DPM2	14	DPM status bit	0x0: Plunger moved 0x1: Plunger did not move
DPM1	13	DPM status bit	0x0: Plunger moved 0x1: Plunger did not move
DPM0	12	DPM status bit	0x0: Plunger moved 0x1: Plunger did not move
OLF3	11	Open-loop detection bit	0x0: No open-loop detected 0x1: Open-loop detected
OLF2	10	Open-loop detection bit	0x0: No open-loop detected 0x1: Open-loop detected
OLF1	9	Open-loop detection bit	0x0: No open-loop detected 0x1: Open-loop detected
OLF0	8	Open-loop detection bit	0x0: No open-loop detected 0x1: Open-loop detected
HHF3	7	Hit current not reached detection bit	0x0: Hit current is reached 0x1: Hit current is not reached
HHF2	6	Hit current not reached detection bit	0x0: Hit current is reached 0x1: Hit current is not reached
HHF1	5	Hit current not reached detection bit	0x0: Hit current is reached 0x1: Hit current is not reached
HHF0	4	Hit current not reached detection bit	0x0: Hit current is reached 0x1: Hit current is not reached
OCP3	3	Overcurrent protection detection bit	0x0: No overcurrent detected 0x1: Overcurrent detected
OCP2	2	Overcurrent protection detection bit	0x0: No overcurrent detected 0x1: Overcurrent detected
OCP1	1	Overcurrent protection detection bit	0x0: No overcurrent detected 0x1: Overcurrent detected
OCP0	0	Overcurrent protection detection bit	0x0: No overcurrent detected 0x1: Overcurrent detected

FAULT1 (0x66)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	RES3	RES2	RES1
Reset	–	–	–	–	–			
Access Type	–	–	–	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BIT	7	6	5	4	3	2	1	0
Field	RES0	OVT	COMER	UVM	IND3	IND2	IND1	IND0
Reset								
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES3	10	Bit is set if the measured resistance exceeds the R_THLD value of the according channel.	0x0: Measured resistance is compliant 0x1: Measured resistance is not compliant
RES2	9	Bit is set if the measured resistance exceeds the R_THLD value of the according channel.	0x0: Measured resistance is compliant 0x1: Measured resistance is not compliant

BITFIELD	BITS	DESCRIPTION	DECODE
RES1	8	Bit is set if the measured resistance exceeds the R_THLD value of the according channel.	0x0: Measured resistance is compliant 0x1: Measured resistance is not compliant
RES0	7	Bit is set if the measured resistance exceeds the R_THLD value of the according channel.	0x0: Measured resistance is compliant 0x1: Measured resistance is not compliant
OVT	6	Bit is set if overtemperature is detected.	0x0: No overtemperature detected 0x1: Overtemperature detected
COMER	5	Bit is set if a communication error is detected.	0x0: No communication error detected 0x1: Communication error detected
UVM	4	Bit is set if undervoltage is detected. Is active after IC startup	0x0: No undervoltage detected 0x1: Undervoltage detected
IND3	3	Bit is set if the measured inductance is not compliant according to Excitation Hold or Low Phase.	0x0: Measured inductance is compliant 0x1: Measured inductance is not compliant
IND2	2	Bit is set if the measured inductance is not compliant according to Excitation Hold or Low Phase.	0x0: Measured inductance is compliant 0x1: Measured inductance is not compliant
IND1	1	Bit is set if the measured inductance is not compliant according to Excitation Hold or Low Phase.	0x0: Measured inductance is compliant 0x1: Measured inductance is not compliant
IND0	0	Bit is set if the measured inductance is not compliant according to Excitation Hold or Low Phase.	0x0: Measured inductance is compliant 0x1: Measured inductance is not compliant

OTP_CONTROLLER

The OTP_CONTROLLER register can be accessed in OTP Programming mode only. To enter OTP Programming mode, the SPI command 0xFD12A7 needs to be issued (see the OTP Programming procedure).

ADDRESS	NAME	MSB							LSB
MTP_CTRL									
0x68	OTP_CONTROL[7:0]	–	–	–	–	–	–	STOP_PROG	SRT_PROG
0x69	OTP_STATUS[7:0]	DONE	ECC_ER R_2BIT	ECC_ER R_1BIT	OV_DUR ING_BU RN_PUL SE	VPP_INI T_FAIL	OTP_FU LL	VERI_FA IL	–
OTP_RECORD									
0x7A	OTP_DATA0[7:0]	OTP_RECORD[7:0]							
0x7B	OTP_DATA1[7:0]	OTP_RECORD[15:8]							
0x7C	OTP_ADDR[7:0]	OTP_RECORD[23:16]							

Register Details

OTP_CONTROL (0x68)

OTP Control Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STOP_PROG	SRT_PROG
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read, Pulse	Write, Read, Pulse

BITFIELD	BITS	DESCRIPTION
STOP_PROG	1	At any time, writing this bit to 1 will STOP/abandon a field program burn.
SRT_PROG	0	Start executing the OTP write procedure.

OTP_STATUS (0x69)

OTP Status Register

BIT	7	6	5	4	3	2	1	0
Field	DONE	ECC_ERR_2BIT	ECC_ERR_1BIT	OV_DURING_BURN_PULSE	VPP_INIT_FAIL	OTP_FULL	VERI_FAIL	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION
DONE	7	Programming complete
ECC_ERR_2BIT	6	One of the previously burned records contains an uncorrectible 2-bit error. The record was not loaded, and the registers it was intended to load were not written. If an erronus record is overwritten by a correct record, this status will not be cleared.
ECC_ERR_1BIT	5	One of the actively loaded records contains a single-bit error that was corrected. If an erroneous record is overwritten by a correct record, this status will be cleared for each mtp register.
OV_DURING_BURN_PULSE	4	When the memory is actively executing a burn pulse, the high-voltage VPP voltage has gone above the abs-max specified in the data sheet. This is considered a critical failure, and device operation is not guaranteed thereafter.
VPP_INIT_FAIL	3	The programming voltage did not reach the desired value before burning. Therefore, the burn was abandoned and not attempted.
OTP_FULL	2	The OTP is full, and no more records can be burned.
VERI_FAIL	1	OTP record was attempted to be burned OTP_REPG_TIMES times, and verification of each attempt produced an incorrect result. Where OTP_REPG_TIMES is a parameter to the IP.

OTP_DATA0 (0x7A)

Least Significant Byte for OTP write

BIT	7	6	5	4	3	2	1	0
Field	OTP_RECORD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTP_RECORD	7:0	

OTP_DATA1 (0x7B)

Most Significant Byte for OTP write

BIT	7	6	5	4	3	2	1	0
Field	OTP_RECORD[15:8]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTP_RECORD	7:0	

OTP_ADDR (0x7C)

RegMap Register Address for OTP Write

BIT	7	6	5	4	3	2	1	0
Field	OTP_RECORD[23:16]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTP_RECORD	7:0	

Applications Information

Examples of Use

The high configurability of the MAX22216/MAX22217 provide flexibility. Figure 14 shows some of the typical applications addressed by the device.

- [A] shows a SPI-based application. The MCU and the driver communicate via SPI. Configuration settings are written into the device after power up. Status information is exchanged via SPI too. Different loads are supported (single/ended/differential solenoids, brushed DC motors, mixed solenoid + brushed).
- [B] and [C] show two typical applications in which the MAX22216/MAX22217 are OTP programmed and controlled by a remote host controller. The number of control signal wires is minimized.
  - [B] refers to a single differential valve driver with minimum wiring (supply and GND only) (see the *VM Switching Stand-Alone* section).
  - [C] refers to a multi valves and/or DC-motor driver in which the remote host controller outputs the CNTL trigger signals for the actuators.

In these examples, the STAT output pins drive LED diodes.

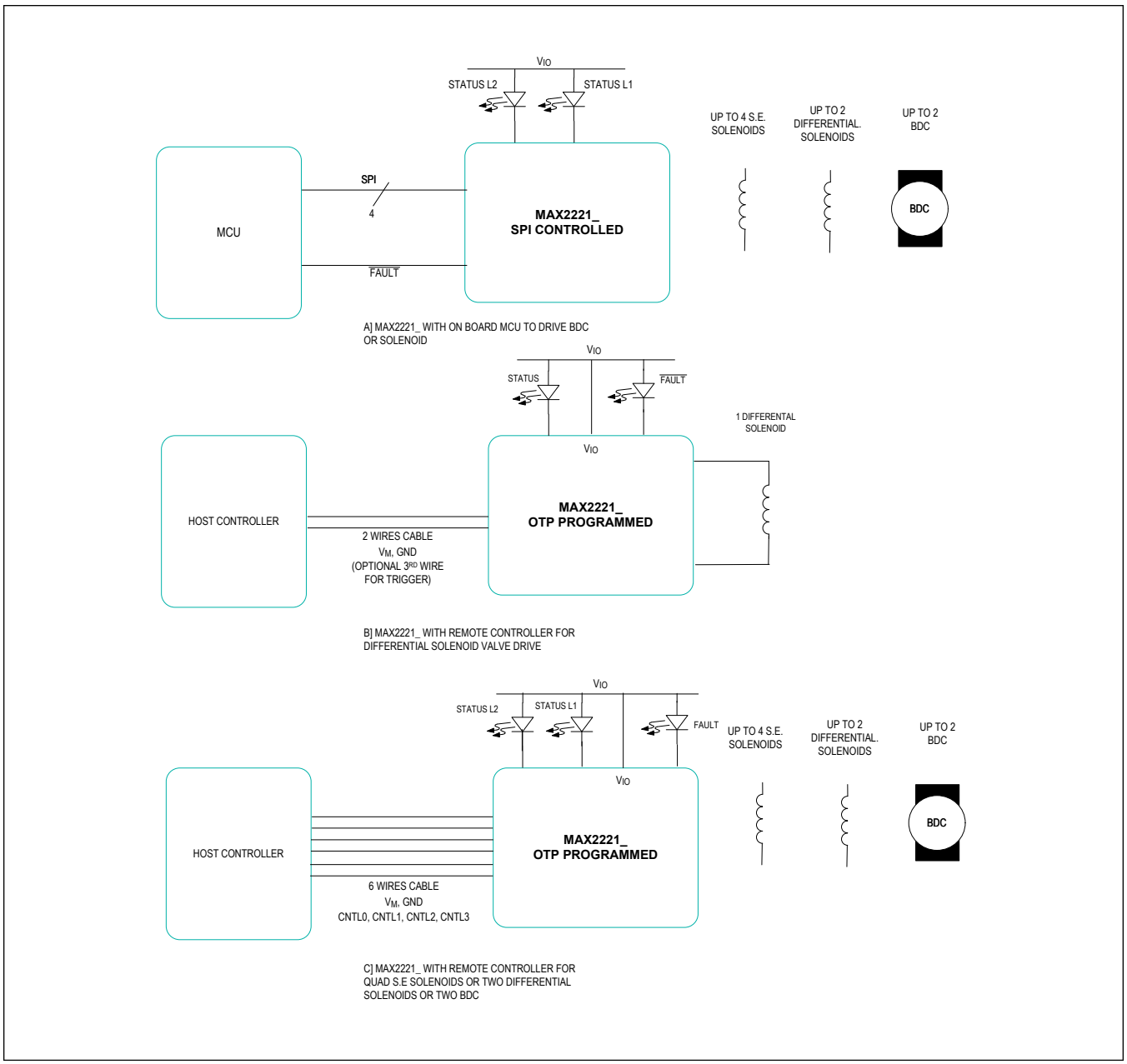


Figure 14. Examples of Use

V_M Switching Stand-Alone

Figure 15 shows an example of an electronic valve application. The driver is locally mounted into the valve housing and controlled remotely by simply switching the supply voltage (V_M). The MAX22216/MAX22217 are OTP programmed to drive a solenoid valve differentially with pairs of half bridges connected in parallel. This configuration requires two control wires from a remote controller (VM and GND). The V_{IO} is internally generated (see the *V_{IO} Pin Description (V_{IO})* section). The solenoid energization is triggered by the rising edge of the V_M supply and starts after a wake-up time (T_{WAKE}), which includes the rising time of the supply and the wake-up time of the device (see the *Electrical Characteristics* table).

The activation and deactivation V_M thresholds (VM_THLD_UP, VM_THLD_DW) can be set by writing the corresponding

4 bits OTP bitfields in the VM_THRESHOLD register. If only the VM_THLD_DOWN is used, the set voltage in this register will become the deactivation limit if the V_M falls under it, and it will resume normal functionality when the V_M goes again over it. When both V_M thresholds are used, they create a hysteresis effect in which VM_THLD_DOWN remains the low voltage deactivation limit, but for reactivation, the V_M must be bigger than the set voltage for VM_THLD_UP. These limits can be set to control the ICs functionality even without the OTP.

$\overline{\text{FAULT}}$ and STAT logic outputs can be used to activate LED diodes, as shown in the diagram. In this example, the STAT output provides the ON/OFF status of the valve.

For fast valves, where the MAX22216/MAX22217 wake-up time would limit the speed performance of the valve, a third wire would be necessary to drive the CNTL signal of the device.

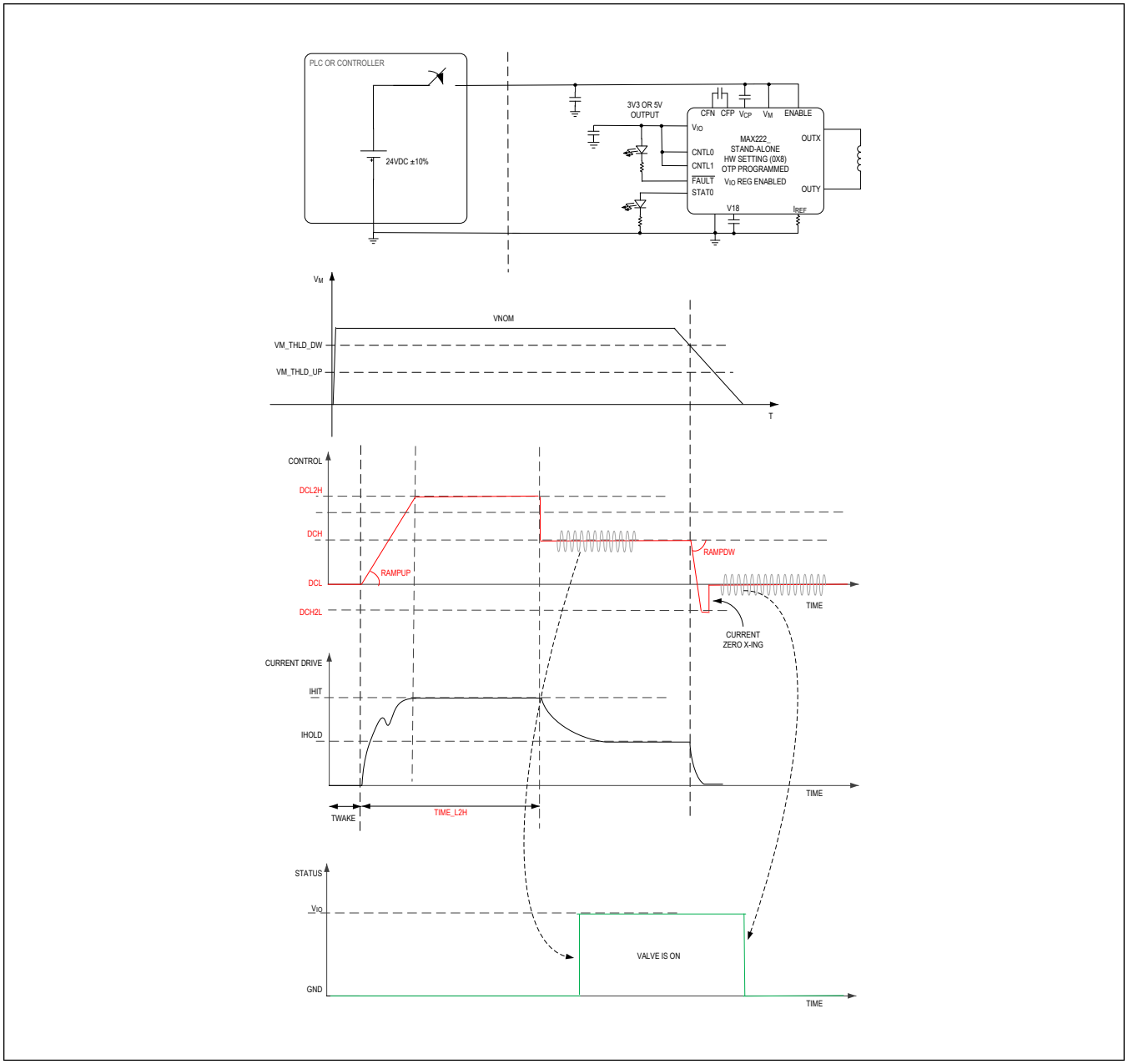
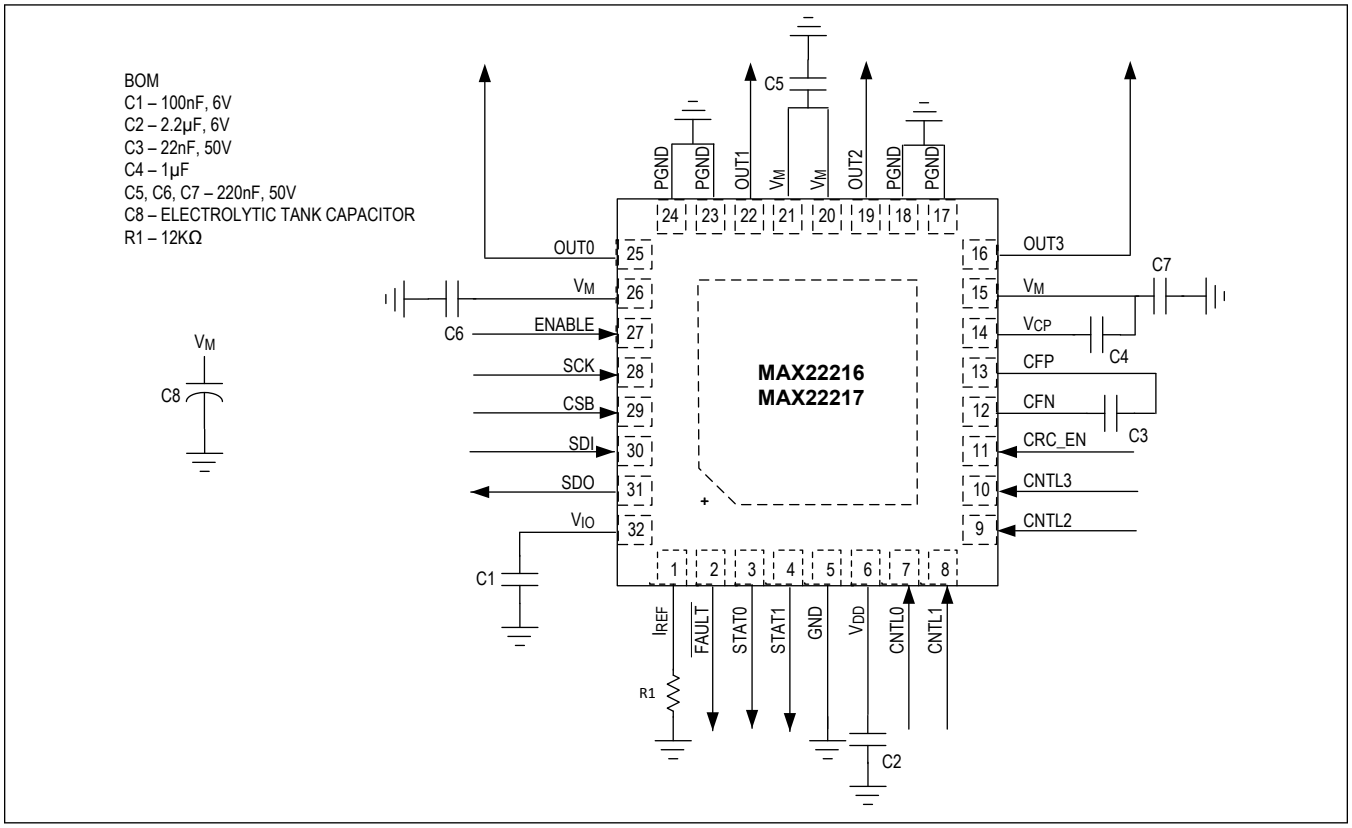


Figure 15. Stand-Alone - VM Switching

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	FULL-SCALE CURRENT (IFS)
MAX22216ATJY+	-40°C to +125°C	32 TQFN - 5mm x 5mm	3.2A
MAX22217ATJY+*	-40°C to +125°C	32 TQFN - 5mm x 5mm	1A

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	09/23	Release for Market Intro	—