



## 3 Phase DC Brushless Motor Pre-Driver IC

### FEATURES

- Supply Voltage  $V_{CC}=6.3$  to  $36V$
- Low Quiescent Current  $I_{DD}=3.2mA$  typ. (at  $V_{CC}=24V$ )
- PWM Control (2 type) DC Voltage Input  
Direct PWM Input
- Lock Protection (2 type) Auto Recovery  
Latching
- FG Output (2type)
- Forward / Reverse Function
- Current Limit  $V_{DETLIM}=0.28V\pm 0.03V$
- Thermal Shutdown
- Under Voltage Lockout
- Operating Temperature  $T_{opr}=-40$  to  $125^{\circ}C$
- Package Outline EQFN24-LE

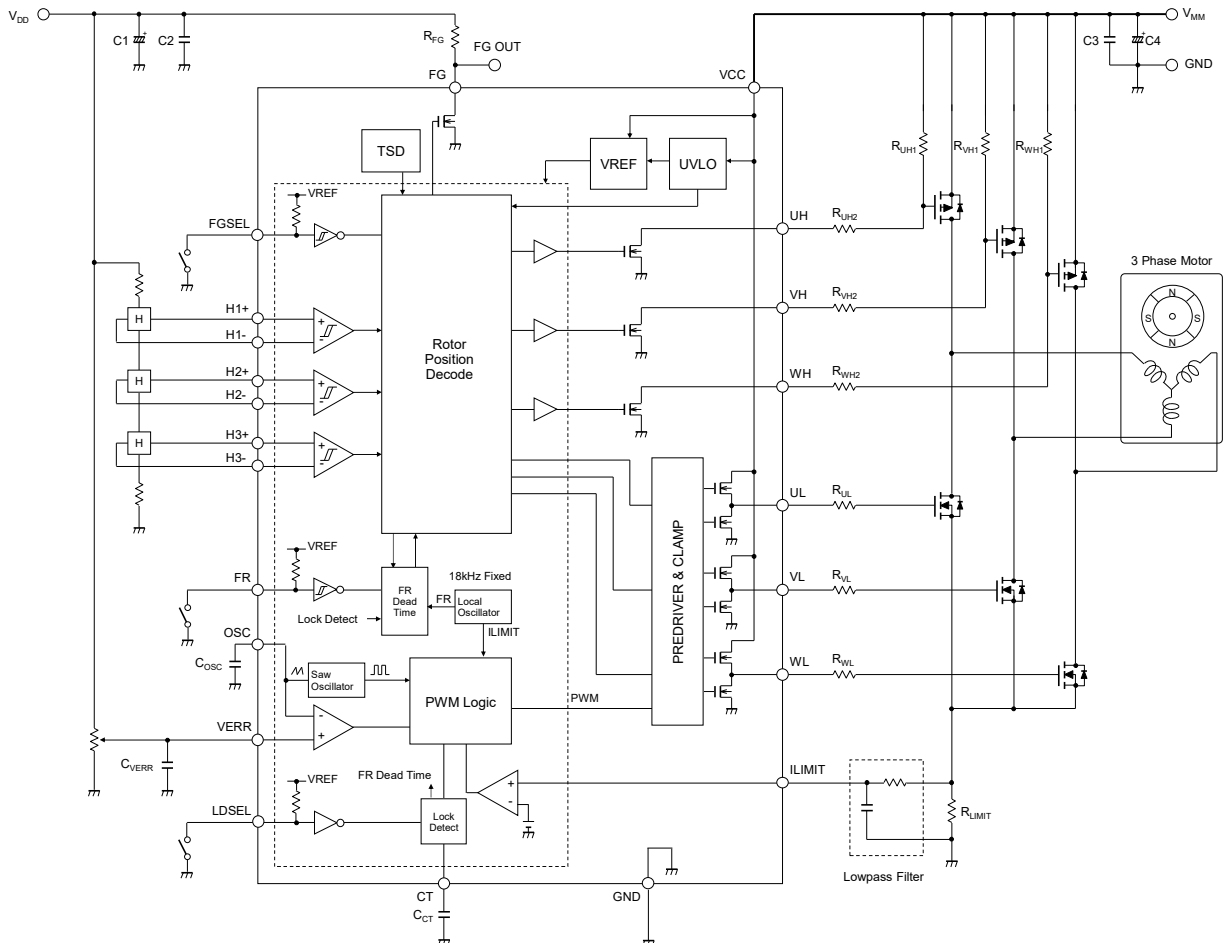
### GENERAL DESCRIPTION

The NJW4315 is a 3-Phase Brushless DC Motor pre-driver IC with  $120^{\circ}$  turn-on. The NJW4315 generates 3 phase sequence based on external hall signal input and drives power elements. It features wide operating voltage range from  $6.3V$  to  $36V$ , small package and wide temperature range as T1 spec. Therefore, It is suitable for automotive fan motor and built-in motor.

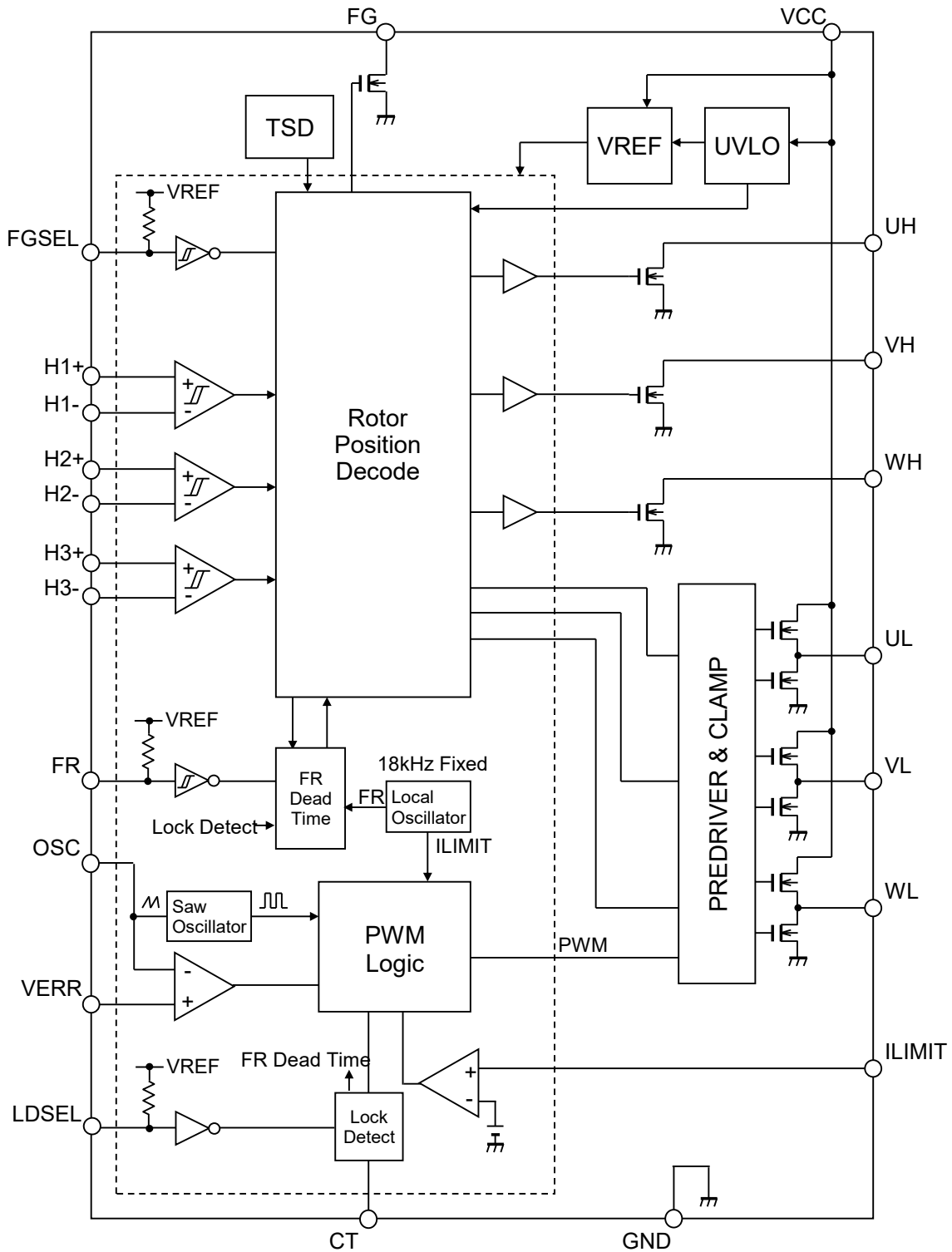
### APPLICATION

- FAN Motor
- Small Built-in Motor

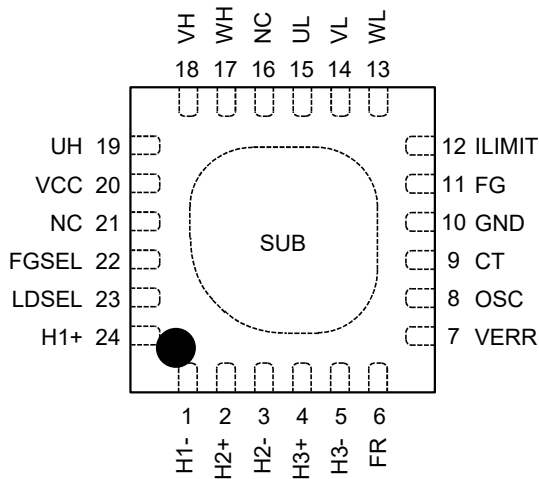
### TYPICAL APPLICATION



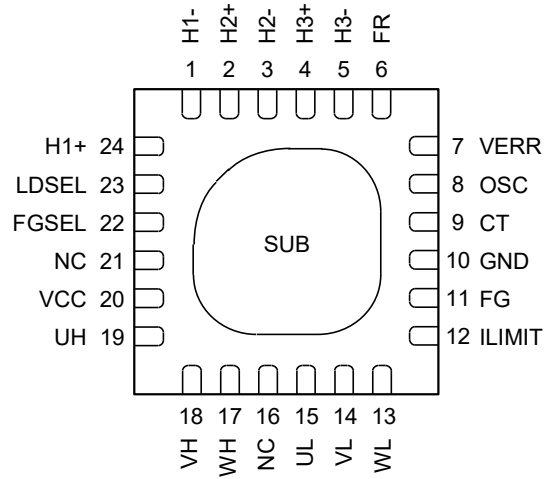
## ■BLOCK DIAGRAM



## ■PIN CONFIGURATION



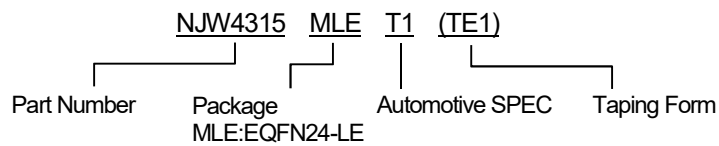
< Top View >



< Bottom View >

PIN NO.	SYMBOL	I/O	DESCRIPTION	NOTE
1	H1 -	I	Hall Input Pin H1-	U Phase Hall Signal Input -
2	H2+	I	Hall Input Pin H2+	V Phase Hall Signal Input +
3	H2 -	I	Hall Input Pin H2-	V Phase Hall Signal Input -
4	H3+	I	Hall Input Pin H3+	W Phase Hall Signal Input +
5	H3 -	I	Hall Input Pin H3-	W Phase Hall Signal Input -
6	FR	I	FR Input Pin	Select for direction of motor rotation
7	VERR	I	VERR Input Pin	Setting for PWM duty
8	OSC	-	OSC Frequency setting Pin	Setting for PWM frequency
9	CT	-	Ct Frequency setting Pin	Setting for lock protection timer
10	GND	-	Ground Pin	Connect to GND
11	FG	O	FG Output Pin	Frequency output of motor rotation
12	ILIMIT	I	ILIMIT Detection Pin	Over Current Detection of motor drive circuit
13	WL	O	WL Output Pin	W Phase Output for Low Side
14	VL	O	VL Output Pin	V Phase Output for Low Side
15	UL	O	UL Output Pin	U Phase Output for Low Side
16, 21	NC	-	Non Connection	Not Internally Connected
17	WH	O	WH Output Pin	W Phase Output for High Side
18	VH	O	VH Output Pin	V Phase Output for High Side
19	UH	O	UH Output Pin	U Phase Output for High Side
20	VCC	-	Power Supply Pin	Connect to DC power supply.
22	FGSEL	I	FG Select Pin	Select for FG output type
23	LDSEL	I	LD Select Pin	Select for release type of lock protection
24	H1+	I	Hall Input Pin H1+	U Phase Hall Signal Input +
-	Exposed PAD	-	Back Side Thermal PAD	It must be set to open or connected to GND.

## ■PRODUCT NAME INFORMATION



## ■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJW4315MLET1(TE1)	EQFN24-LE	yes	yes	Sn2Bi	4315T1	31	1000

## ■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	$V_{CC}$	40	V	VCC Pin
H Side Output Pin Voltage	$V_{OH}$	40	V	UH, VH, WH Pin
FG Pin Voltage	$V_{FG}$	7	V	FG Pin
Hall Input Pin Voltage	$V_{IH}$	7	V	H1+, H1-, H2+, H2-, H3+, H3- Pin
Logic Input Pin Voltage	$V_{IN}$	7	V	FR Pin
ILIMIT Pin Voltage	$V_{LIM}$	3.5	V	ILIMIT Pin
VERR Pin Voltage	$V_{VERR}$	7	V	VERR Pin
H Side Output Current	$I_{OH}$	150	mA	UH, VH, WH Pin
L Side Output Current	$I_{OL}$	±150	mA	UL, VL, WL Pin
FG Output Current	$I_{FG}$	15	mA	FG Pin
Power Dissipation(Ta=25°C)	$P_D$	910 <sup>(1)</sup>	mW	
EQFN24-LE		2100 <sup>(2)</sup>		
Junction Temperature Range	$T_j$	-40 to +150	°C	
Operating Temperature Range	$T_{opr}$	-40 to +125	°C	
Storage Temperature Range	$T_{stg}$	-50 to +150	°C	

(1): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(2): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

(For 4Layers: Applying 99.5×99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

## ■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	6.3 to 36	V

## ■ PIN OPERATING CONDITION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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### Hall Input Pin (H1+, H1-, H2+, H2-, H3+, H3-)

Hall Input Sensitivity	$\Delta V_{MIH}$	Peak to peak	0.08	-	-	V
Hall Input Voltage Range	$V_{ICMIH}$	$V_{IHB} \leq 2.0V$	0	-	3.0	V

### Logic Input Pin (FR, FGSEL, LDSEL)

H Level Input Voltage 1	$V_{HIN1}$	FR, FGSEL Pin	2	-	5.5	V
H Level Input Voltage 2	$V_{HIN2}$	LDSEL Pin	2.4	-	5.5	V
L Level Input Voltage	$V_{LIN}$		0	-	0.8	V

### VERR Pin

Input Voltage Range	$V_{ICMVERR}$		0-	-	5.5	V
PWM Input Frequency	$f_{PWMVERR}$		-	-	150	kHz

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V_{CC}=24V$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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### GENERAL

Quiescent Current 1	$I_{CC1}$	$V_{CC}=12V$	2.4	2.9	3.8	mA
		$V_{CC}=12V$ , $T_a=-40^\circ C$ to $125^\circ C$	2.2	-	4.1	
Quiescent Current 2	$I_{CC2}$		2.7	3.2	4.1	mA
		$T_a=-40^\circ C$ to $125^\circ C$	2.5	-	4.4	

### THERMAL SHUTDOWN BLOCK

TSD Operating Temperature	$T_{TSD1}$		-	180	-	$^\circ C$
TSD Recovery Temperature	$T_{TSD2}$		-	130	-	$^\circ C$
TSD Hysteresis Temperature	$\Delta T_{TSD}$		-	50	-	$^\circ C$

### UNDER VOLTAGE LOCK OUT BLOCK

UVLO Detect Voltage	$V_{DUVLO}$	$V_{CC}$ Decreasing	4.8	5.4	6.0	V
		$V_{CC}$ Decreasing, $T_a=-40^\circ C$ to $125^\circ C$	4.7	-	6.1	
UVLO Recovery Voltage	$V_{RUVLO}$	$V_{CC}$ Increasing	4.9	5.5	6.1	V
		$V_{CC}$ Increasing, $T_a=-40^\circ C$ to $125^\circ C$	4.8	-	6.2	
UVLO Hysteresis Voltage Width	$\Delta V_{UVLO}$		-	0.1	-	V

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V_{CC}=24V$ ,  $T_a=25^{\circ}C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>LOCK DETECT BLOCK</b>						
Lock Protection ON Time	$t_{ON}$	$C_{CT}=0.47\mu F$	-	0.25	-	s
H Level Voltage	$V_{HCT}$		2.8	3.0	3.2	V
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	2.8	-	3.2	
L Level Voltage	$V_{LCT}$		0.8	1.0	1.2	V
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	0.8	-	1.2	
Lock Charge Current	$I_{CHGCT}$	$V_{CT}=0V \rightarrow 2.0V$	5.0	6.5	8.5	$\mu A$
		$V_{CT}=0V \rightarrow 2.0V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	4.0	-	10	
Lock Discharge Current	$I_{DCHGCT}$	$V_{CT}=3.5V \rightarrow 2.0V$	0.3	0.65	0.9	$\mu A$
		$V_{CT}=3.5V \rightarrow 2.0V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	0.3	-	1.1	
Lock Charge Discharge Current Ratio	$I_{CHGCT} / I_{DCHGCT}$		-	10	-	-

## HALL AMP BLOCK

Hysteresis Voltage Range	$\Delta V_{HYSH}$		10	30	50	mV
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	5	-	60	
Input Bias Current	$I_{BIH}$	Per 1 Input	-	-	2	$\mu A$
		Per 1 Input, $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	2	

## HIGH SIDE OUTPUT BLOCK

High Side Output Voltage	$V_{OLH}$	$I_{SINK}=50mA$	-	0.5	1.2	V
		$I_{SINK}=50mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	1.6	
High Side Leak Current	$I_{OLEAKH}$	$V_{OH}=36V$	-	-	1	$\mu A$
		$V_{OH}=36V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	1	

## LOW SIDE OUTPUT BLOCK

Low Side Output H Voltage 1	$V_{OHL1}$	$V_{CC}=12V$ , $I_{SOURCE}=50mA$	8.0	10.0	-	V
		$V_{CC}=12V$ , $I_{SOURCE}=50mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	8.0	-	-	
Low Side Output H Voltage 2	$V_{OHL2}$	$I_{SOURCE}=50mA$	8.0	10.0	-	V
		$I_{SOURCE}=50mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	8.0	-	-	
Low Side Output L Voltage	$V_{OLL}$	$I_{SINK}=50mA$	-	0.5	1.2	V
		$I_{SINK}=50mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	1.6	
Low Side Clamp Voltage	$V_{OCLL}$	$V_{CC}=36V$ , $I_{SOURCE}=0.1mA$	-	-	16	V
		$V_{CC}=36V$ , $I_{SOURCE}=0.1mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	16	

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V_{CC}=24V$ ,  $T_a=25^{\circ}C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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### FG OUTPUT BLOCK

Output Voltage	$V_{FG}$	$I_{FG}=10mA$	-	0.2	0.6	V
		$I_{FG}=10mA$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	0.6	
Leak Current	$I_{FGLEAK}$	$V_{FG}=5V$	-	-	1	$\mu A$
		$V_{FG}=5V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	1	

### OVER CURRENT DETECTION BLOCK

Detect Voltage	$V_{DETLIM}$		0.25	0.28	0.31	V
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	0.25	-	0.32	
Input Bias Current	$I_{BLIM}$		-	1.0	2.0	$\mu A$
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	5.0	

### ERROR AMP BLOCK

PWM0% Detect Voltage	$V_{PWM1VERR}$	Output ON Duty=0%	-	-	0.6	V
		Output ON Duty=0%, $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	0.6	
PWM100% Detect Voltage	$V_{PWM2VERR}$	Output ON Duty=100%	3.5	-	-	V
		Output ON Duty=100%, $T_a=-40^{\circ}C$ to $125^{\circ}C$	3.5	-	-	
Input Bias Current	$I_{BVERR}$	$V_{ERR}=0V$	-	1.0	2.0	$\mu A$
		$V_{ERR}=0V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	5.0	

### OSCILLATOR BLOCK

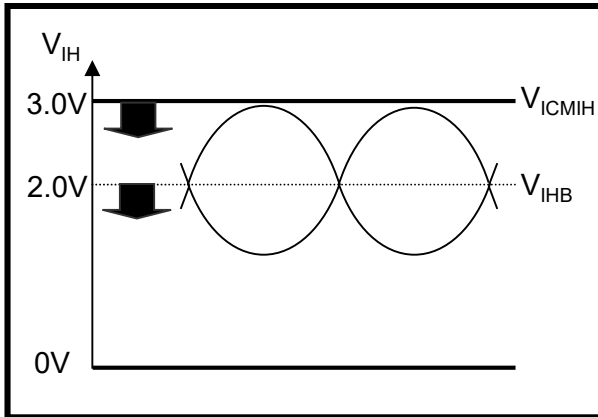
Saw Wave Peak Voltage	$V_{POSC}$		2.7	3.0	3.3	V
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	2.7	-	3.3	
Saw Wave Bottom Voltage	$V_{BOSC}$		0.8	1.0	1.2	V
		$T_a=-40^{\circ}C$ to $125^{\circ}C$	0.8	-	1.2	
OSC Charge Current	$I_{CHGOSC}$	$V_{OSC}=0V \rightarrow 2.0V$	50	80	120	$\mu A$
		$V_{OSC}=0V \rightarrow 2.0V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	40	-	130	
OSC Discharge Current	$I_{DCHGOSC}$	$V_{OSC}=3.5V \rightarrow 2.0V$	0.6	1.3	2.0	mA
		$V_{OSC}=3.5V \rightarrow 2.0V$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	0.5	-	2.1	
Oscillation Frequency	$f_{OSC}$	$C_{OSC}=1000pF$	-	35	50	kHz
		$C_{OSC}=1000pF$ , $T_a=-40^{\circ}C$ to $125^{\circ}C$	-	-	55	

### LOGIC INPUT BLOCK

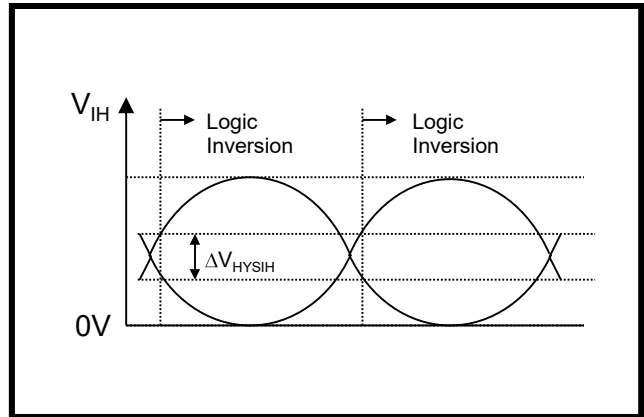
H Level Input Current	$I_{HIN}$	Per 1 Input	-10	-	10	$\mu A$
		Per 1 Input, $T_a=-40^{\circ}C$ to $125^{\circ}C$	-10	-	10	
L Level Input Current	$I_{LIN}$	$V_{IN}=0V$ , Per 1 Input	30	50	100	$\mu A$
		$V_{IN}=0V$ , Per 1 Input, $T_a=-40^{\circ}C$ to $125^{\circ}C$	30	-	100	
Pull Up Resistance	$R_{IN}$		-	100	-	k $\Omega$

## APPLICATION NOTE / GLOSSARY

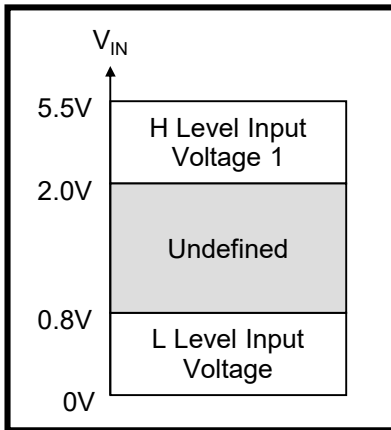
### <Hall Input Pin Common Mode Input Voltage Range>



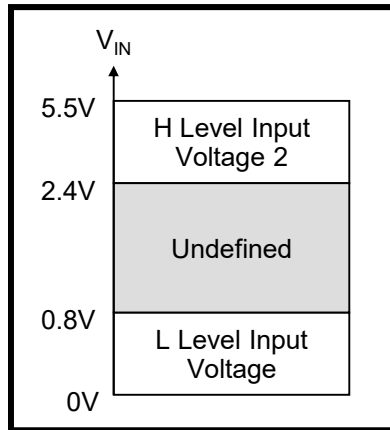
### <Hall Input Hysteresis Voltage width>



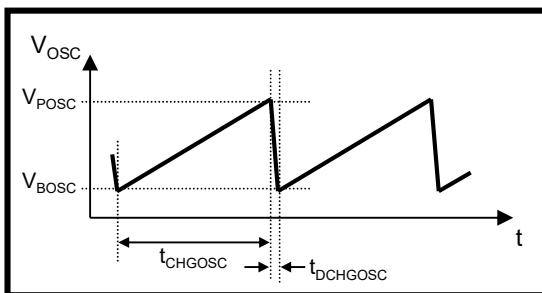
### <FR, FGSEL Pin>



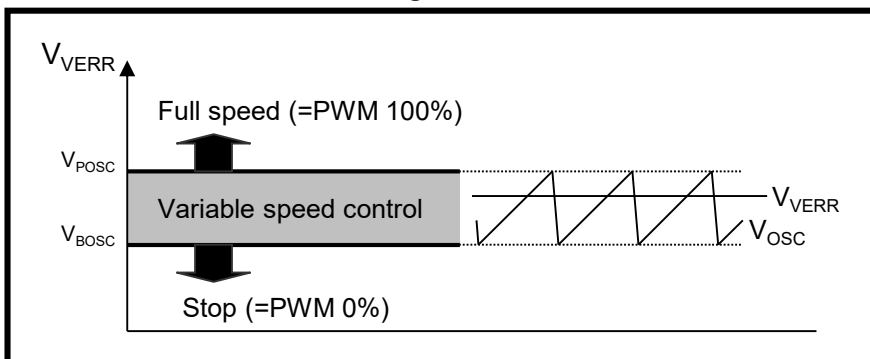
### <LDSEL Pin>



### <OSC Frequency>

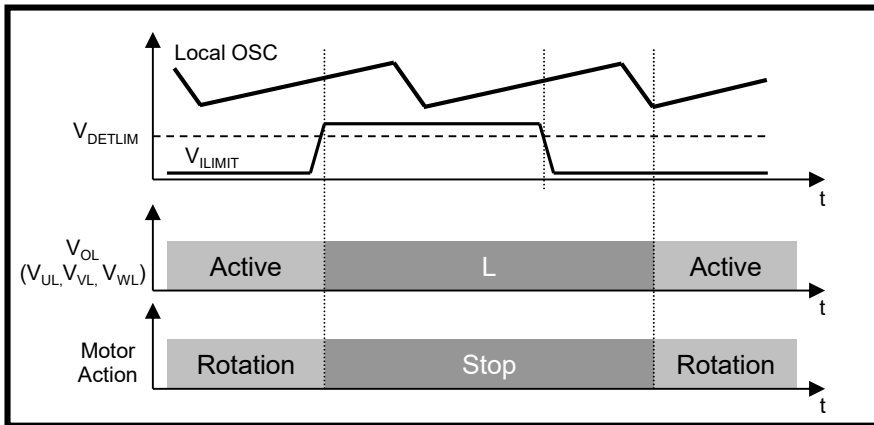


### <PWM0% / PWM100% Detect Voltage>

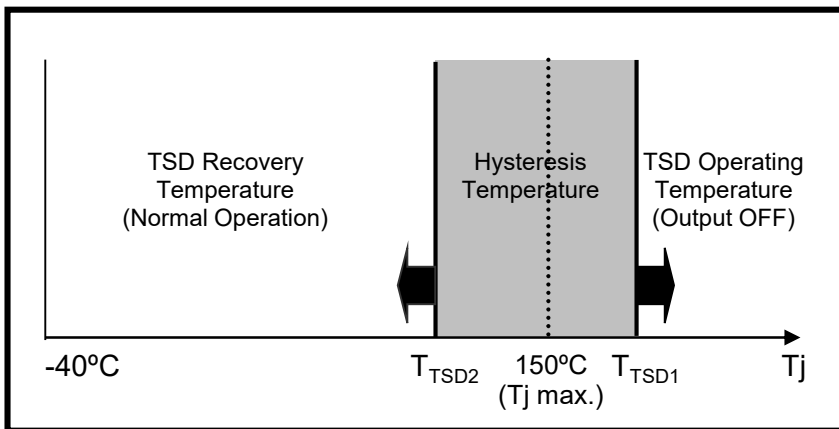




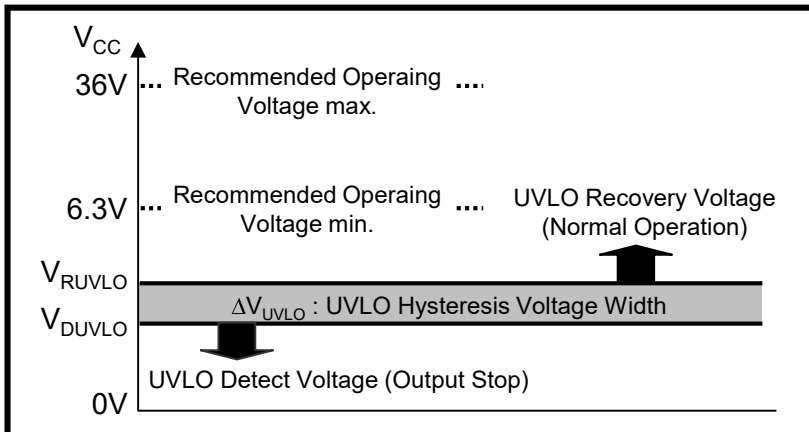
### <Over Current Protection>



### <Thermal Shutdown Protection>



### <Under Voltage Lockout Protection>



●Truth Table

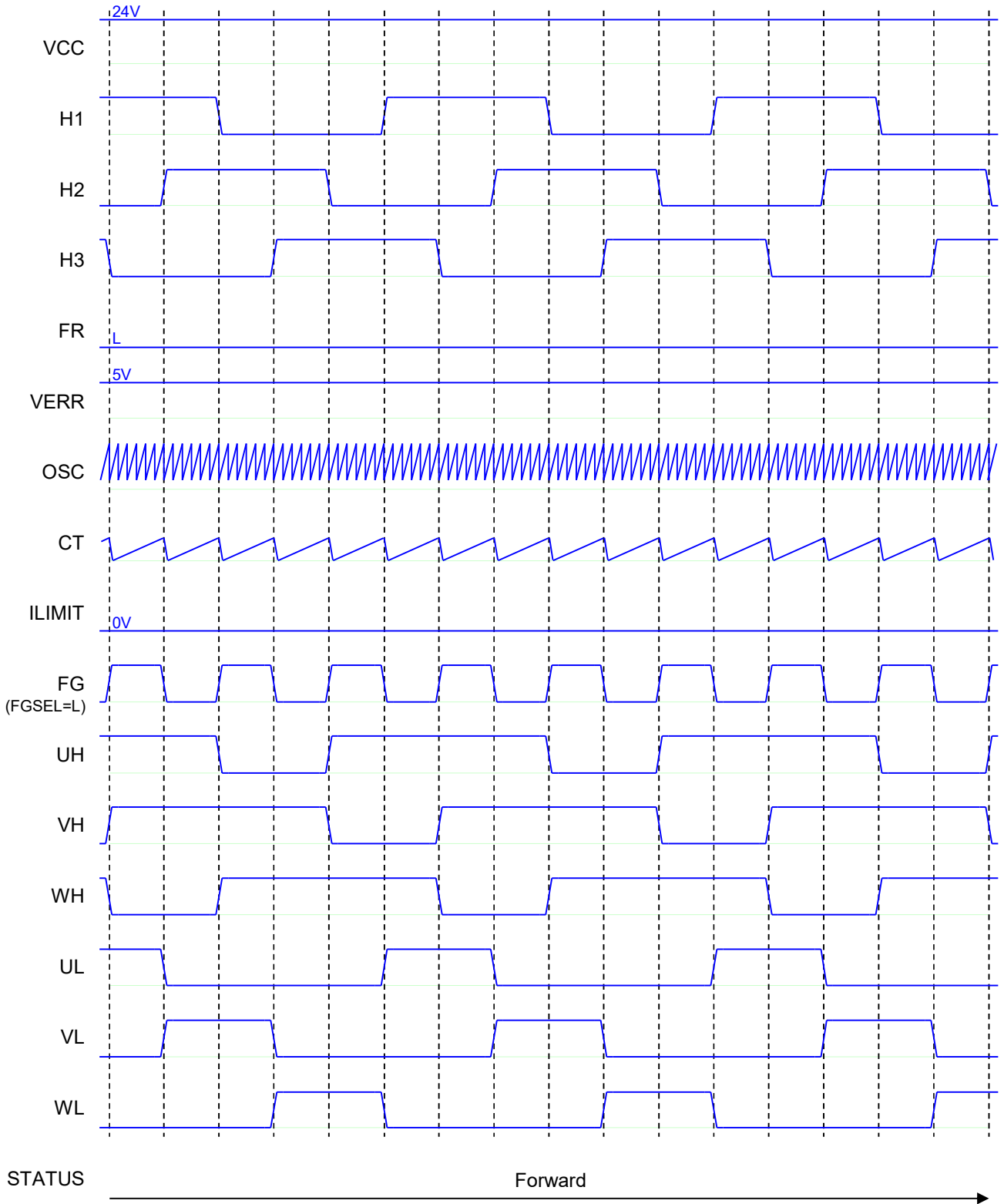
(H1+>H1-, H2+>H2-, H3+>H3- = "H" , Don't care = "X")

H1	H2	H3	FR	TSD	UVLO	ILIMIT	VERR	OSC	CT	UH	VH	WH	UL	VL	WL	FG		STATUS	
																FGSEL=L	FGSEL=H		
H	L	L	L	OFF	OFF	OFF	H/L	L/H	L	Hi-Z	Hi-Z	L	H/L	L	L	Hi-Z	H	Forward (PWM)	
H	H	L								Hi-Z	Hi-Z	L	L	H/L	L	L	H		
L	H	L								L	Hi-Z	Hi-Z	L	H/L	L	L	Hi-Z		L
L	H	H								L	Hi-Z	Hi-Z	L	L	H/L	L	L		L
L	L	H								Hi-Z	L	Hi-Z	L	L	H/L	Hi-Z	L		
H	L	H								Hi-Z	L	Hi-Z	H/L	L	L	L	L		H
H	L	L	L	OFF	OFF	X	X	X	H	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	H	Forward Lock Detect (Output Off Period)	
H	H	L								Hi-Z	Hi-Z	L				Hi-Z	L		
L	H	L								L	Hi-Z	Hi-Z				L	Hi-Z		L
L	H	H								L	Hi-Z	Hi-Z				L	Hi-Z		L
L	L	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
H	L	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
H	L	L	L	OFF	OFF	ON	H	X	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	H	Forward Over Current Protection (Output Off Period)	
H	H	L								Hi-Z	Hi-Z	L				Hi-Z	L		
L	H	L								L	Hi-Z	Hi-Z				L	Hi-Z		L
L	H	H								L	Hi-Z	Hi-Z				L	Hi-Z		L
L	L	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
H	L	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
H	L	L	L	X	ON	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	H	Forward Under Voltage Lockout Protection	
H	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	H								L	Hi-Z	L				Hi-Z	L		
L	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	L	L	ON	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	H	Forward Thermal Shutdown Protection	
H	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	H								L	Hi-Z	L				Hi-Z	L		
L	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	H								L	Hi-Z	L				Hi-Z	L		

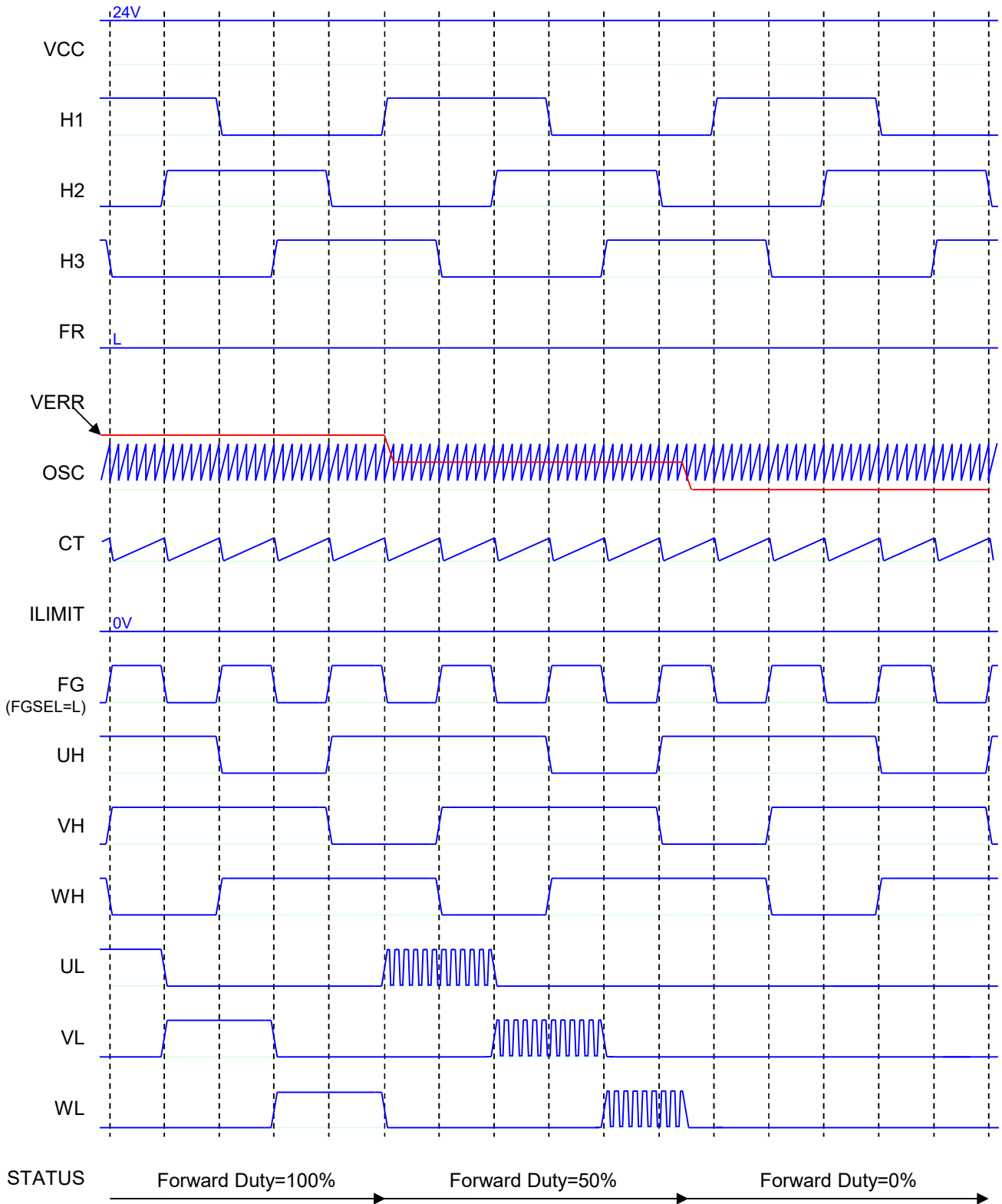
H1	H2	H3	FR	TSD	UVLO	ILIMIT	VERR	OSC	CT	UH	VH	WH	UL	VL	WL	FG		STATUS	
																FGSEL=L	FGSEL=H		
H	L	H	H	OFF	OFF	OFF	H/L	L/H	L	L	Hi-Z	Hi-Z	L	H/L	L	L	H	Reverse (PWM)	
L	L	H								Hi-Z	Hi-Z	L	L	H/L	L	L	Hi-Z		L
L	H	H								Hi-Z	Hi-Z	L	H/L	L	L	L	L		L
L	H	L								Hi-Z	L	Hi-Z	H/L	L	L	L	Hi-Z		L
H	H	L								Hi-Z	L	Hi-Z	L	L	H/L	L	H		
H	L	L								L	Hi-Z	Hi-Z	L	L	H/L	Hi-Z	H		
H	L	L	H	OFF	OFF	X	X	X	H	L	Hi-Z	Hi-Z	L	L	L	L	H	Reverse Lock Detect (Output Off Period)	
H	H	L								Hi-Z	Hi-Z	L				Hi-Z	L		
L	H	L								Hi-Z	Hi-Z	L				Hi-Z	L		
L	H	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
L	L	H								Hi-Z	L	Hi-Z				L	Hi-Z		L
H	L	H								L	Hi-Z	Hi-Z				L	Hi-Z		L
H	L	L	H	X	ON	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	L	H	Reverse Under Voltage Lockout Protection	
H	H	L								Hi-Z	L	Hi-Z				L	Hi-Z		L
L	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	H								L	Hi-Z	L				Hi-Z	L		
L	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	L	H	ON	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	L	Reverse Thermal Shutdown Protection	
H	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	L								L	Hi-Z	L				Hi-Z	L		
L	H	H								L	Hi-Z	L				Hi-Z	L		
L	L	H								L	Hi-Z	L				Hi-Z	L		
H	L	H								L	Hi-Z	L				Hi-Z	L		

H1	H2	H3	FR	TSD	UVLO	ILIMIT	VERR	OSC	CT	UH	VH	WH	UL	VL	WL	FG		STATUS
																FGSEL=L	FGSEL=H	
H	H	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	Hi-Z	Hall Signal Input Error Pattern
L	L	L								Hi-Z	Hi-Z	Hi-Z				Hi-Z	Hi-Z	

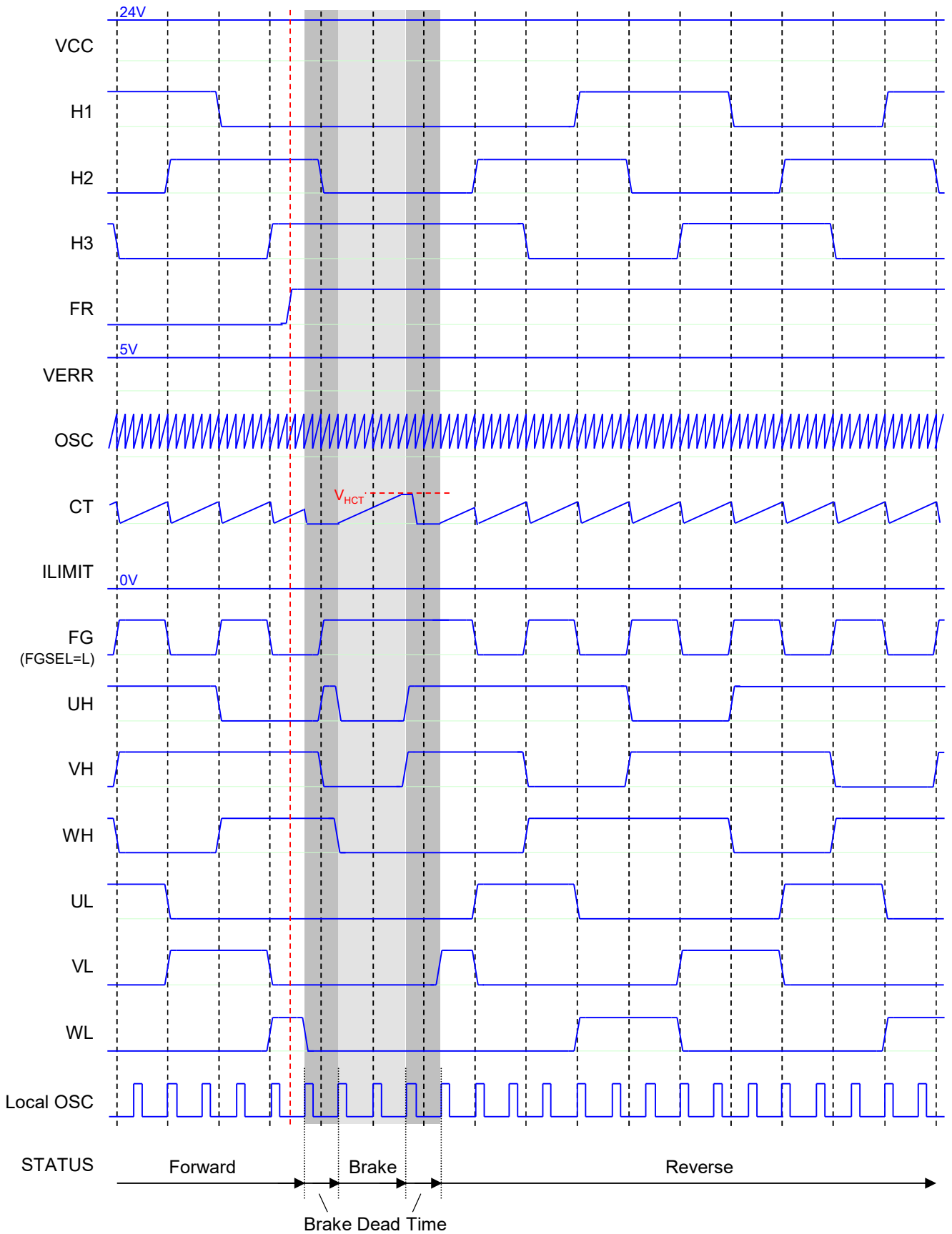
•Timing Chart  
1. Forward



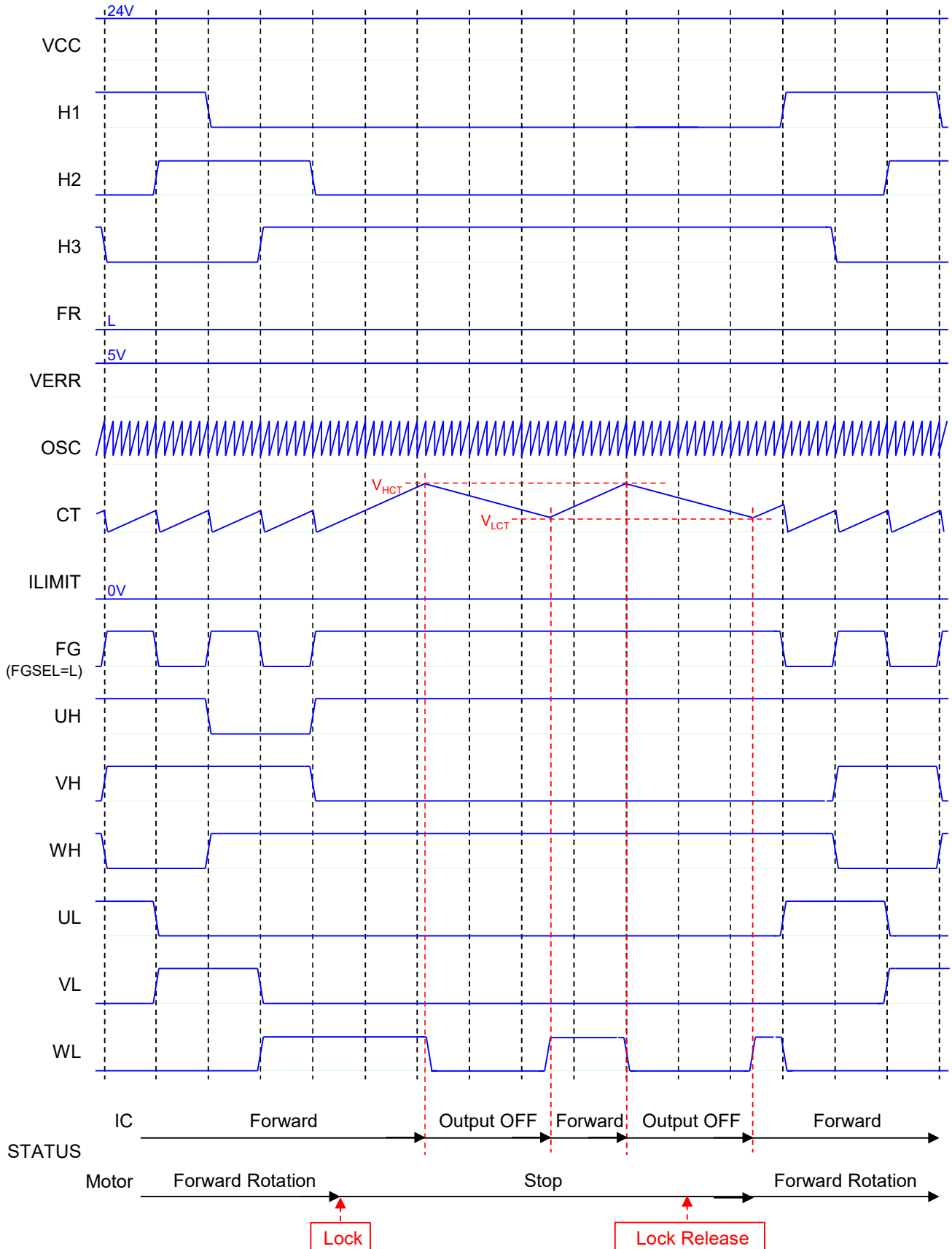
## 2. Forward with PWM



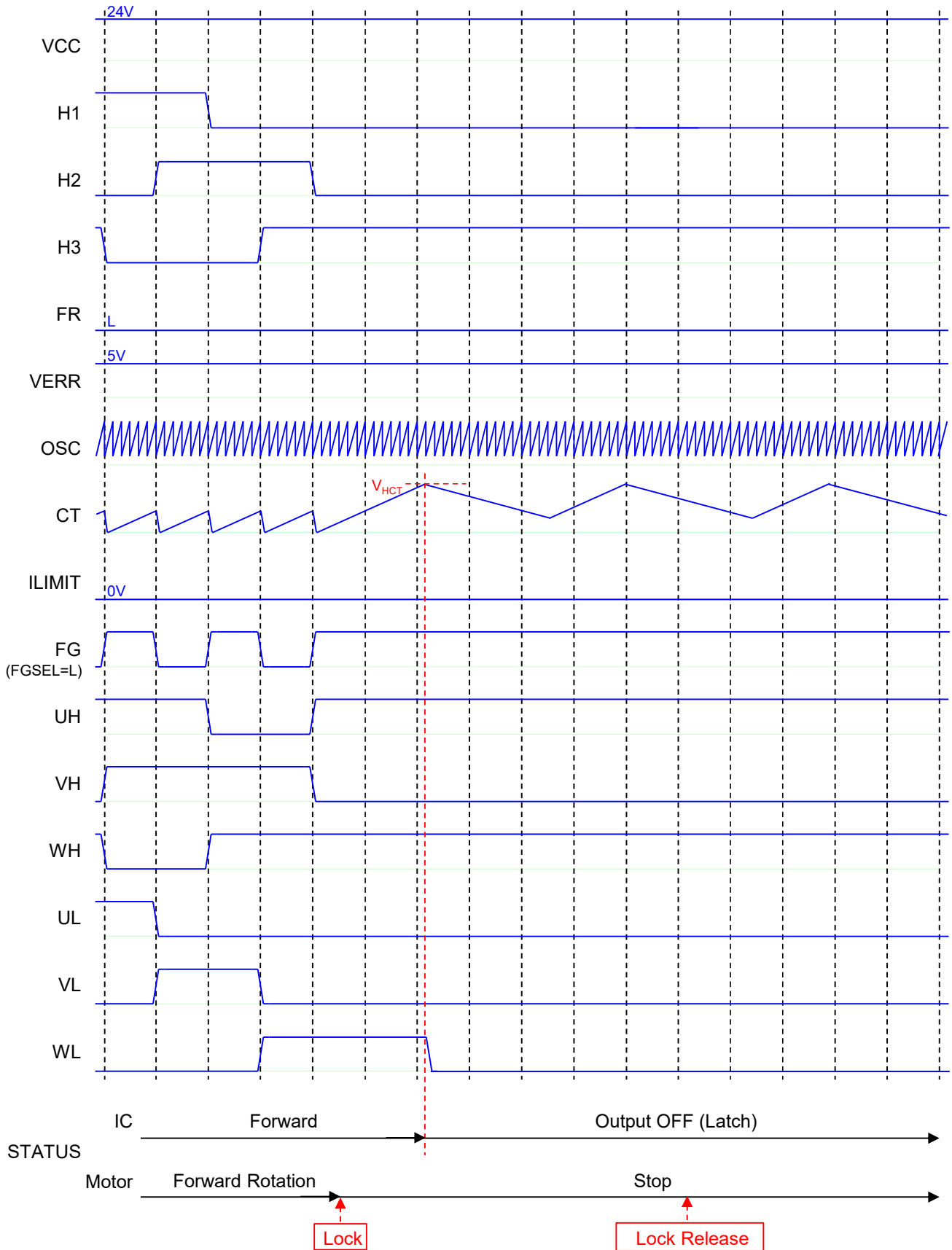
### 3. Switch from forward rotation to reverse rotation



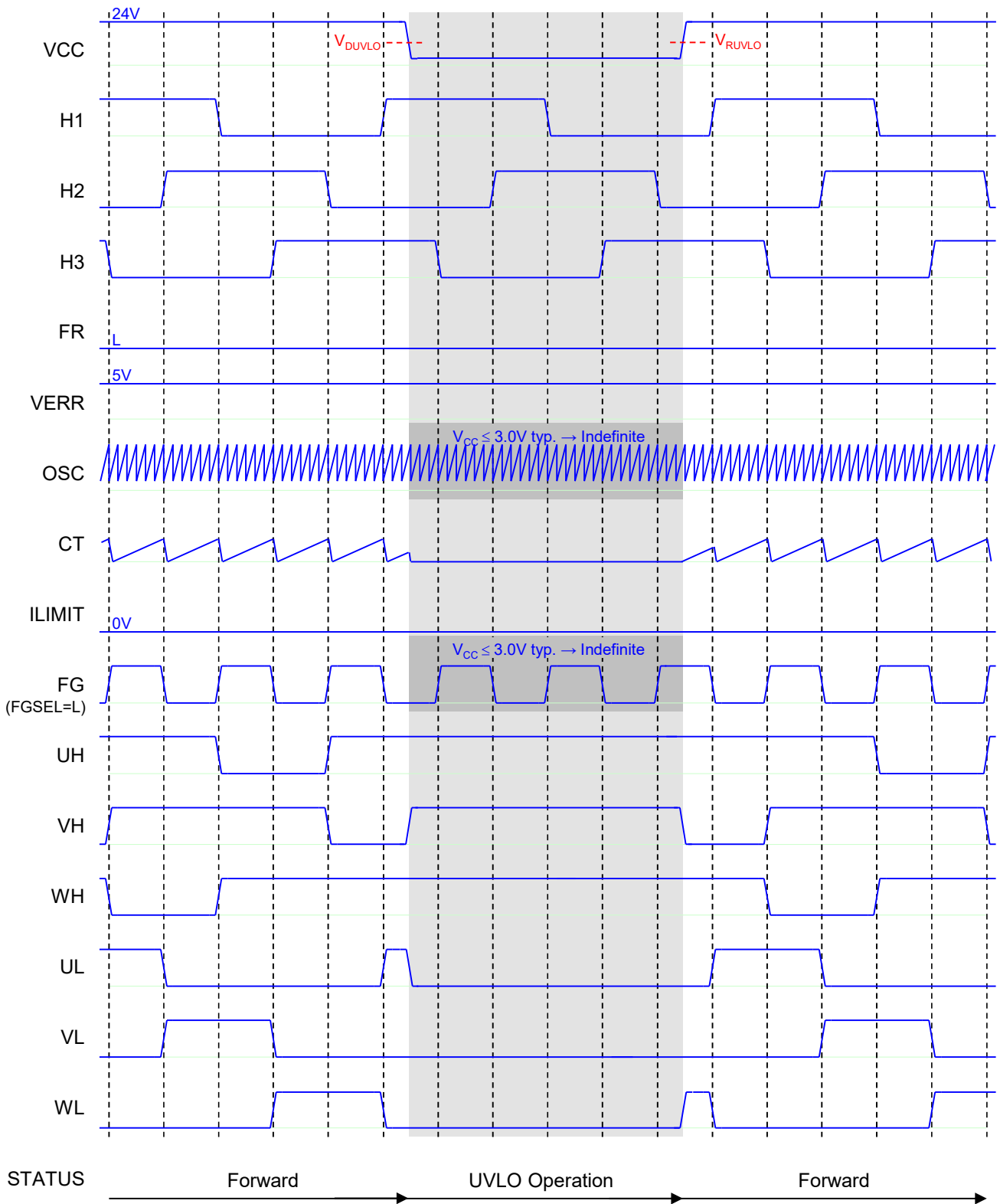
## 4. Lock Operation (at LDSEL=L)



## 5. Lock Operation (at LDSEL=H)

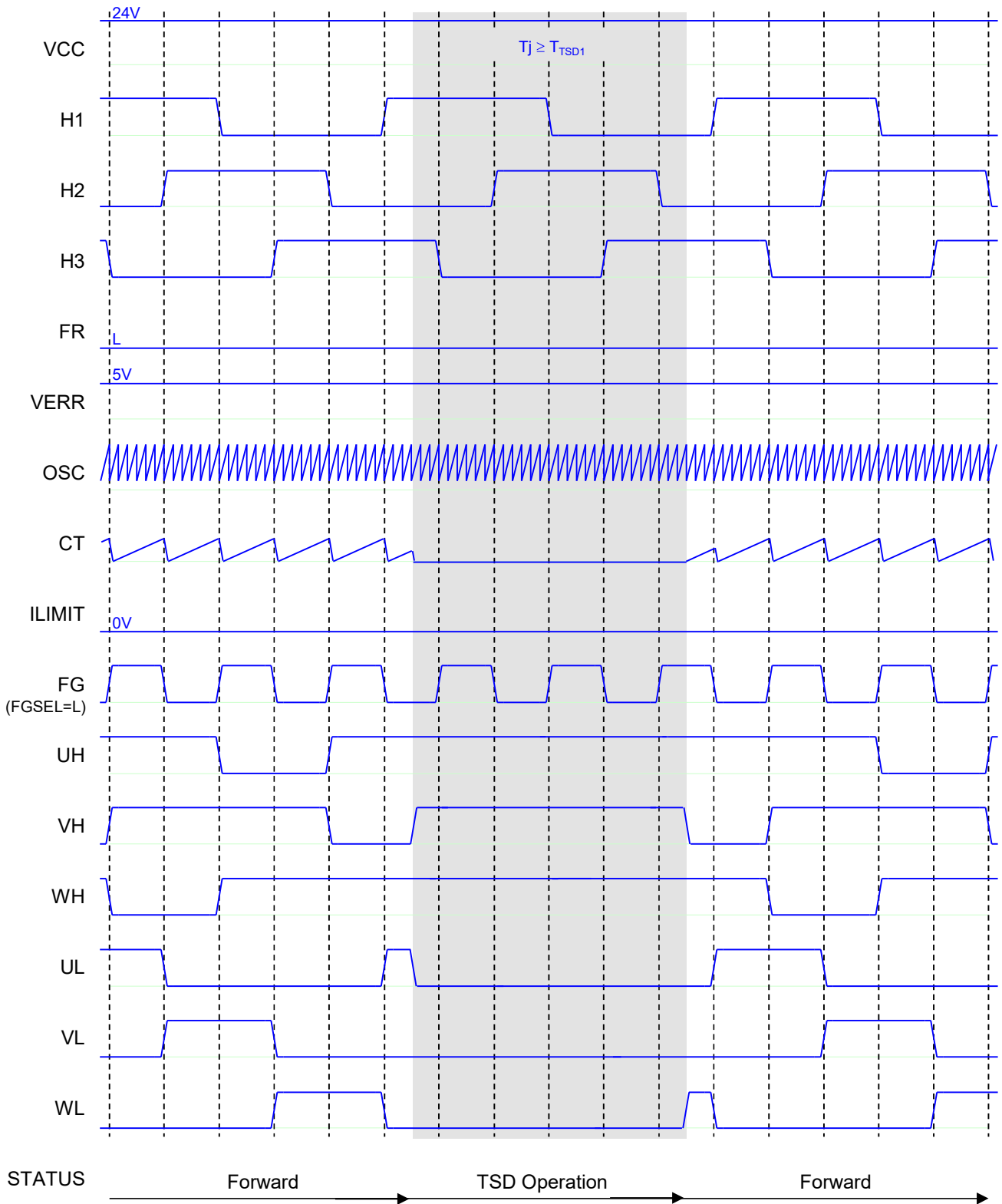


## 6. UVLO Operation



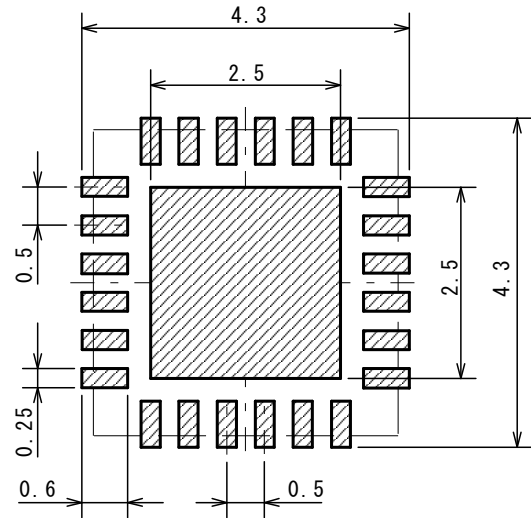
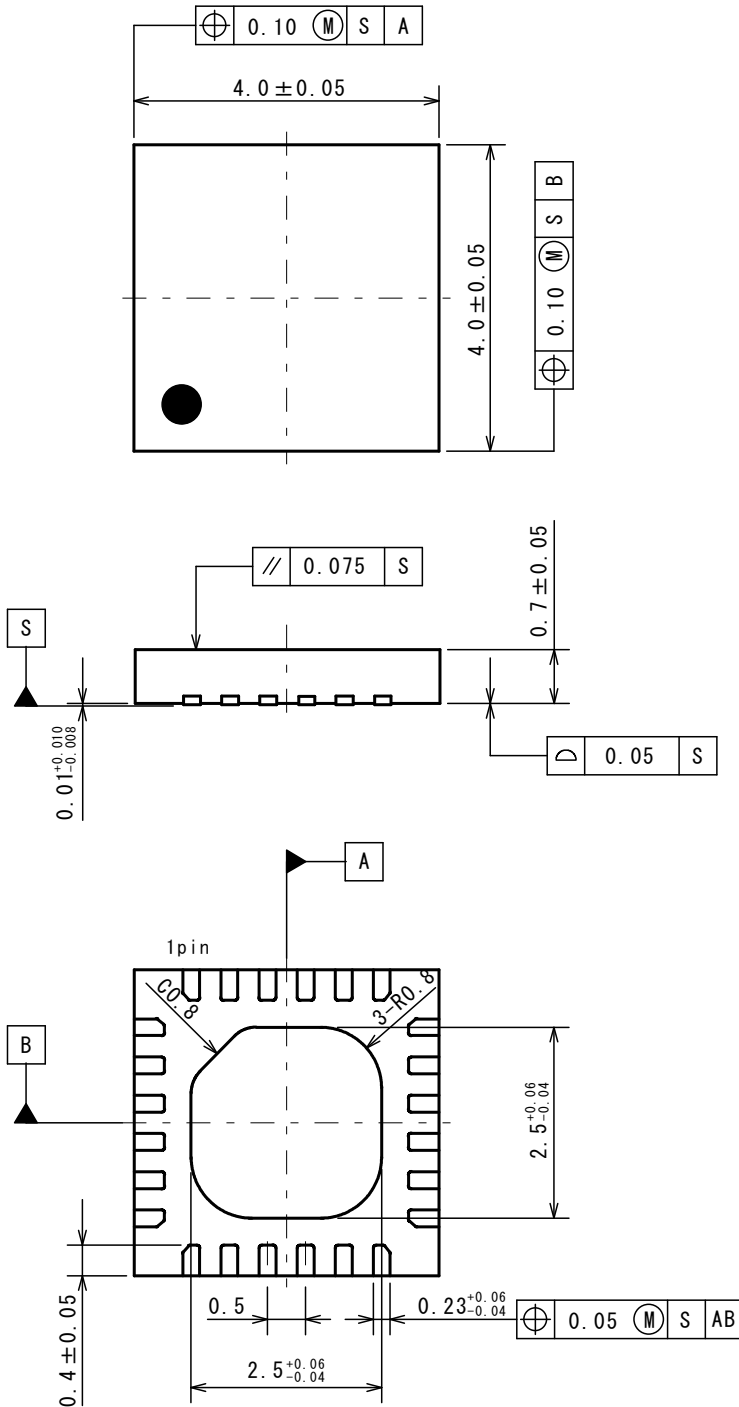


## 7. TSD Operation



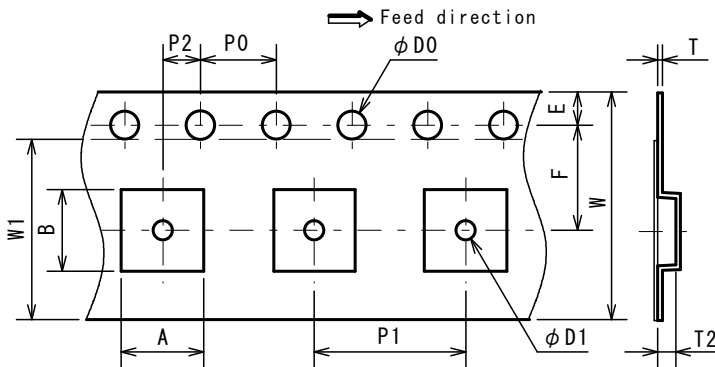
### PACKAGE DIMENSIONS

### EXAMPLE OF SOLDER PADS DIMENSIONS



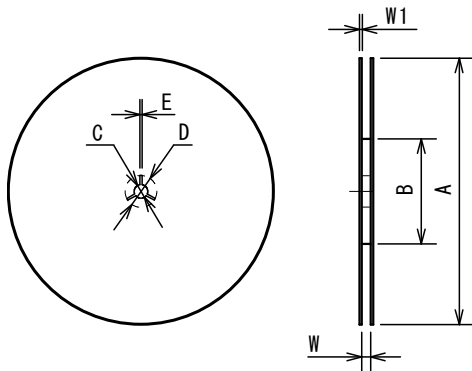
### PACKING SPEC

#### TAPING DIMENSIONS



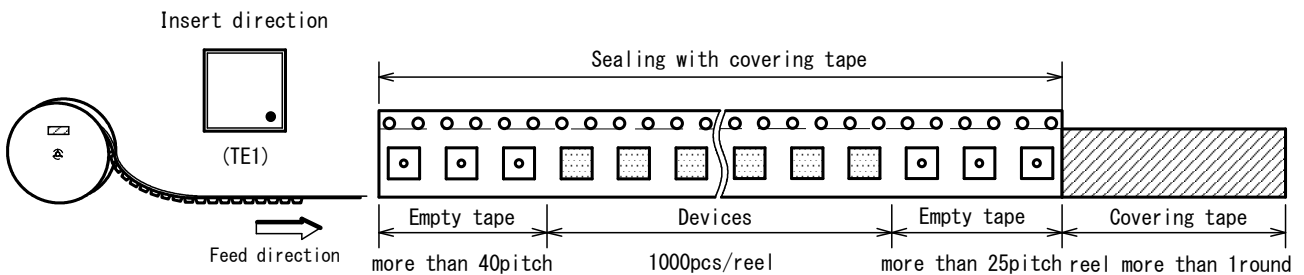
SYMBOL	DIMENSION	REMARKS
A	4.35±0.05	BOTTOM DIMENSION
B	4.35±0.05	BOTTOM DIMENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	1.0±0.1	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	1.3±0.05	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

#### REEL DIMENSIONS

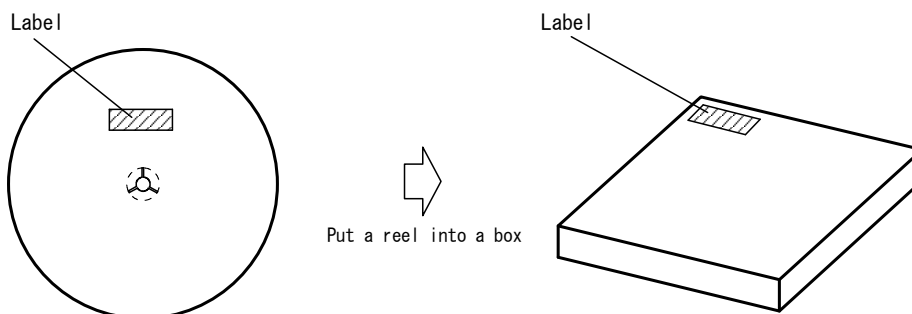


SYMBOL	DIMENSION
A	φ 180 <sup>0</sup> <sub>-1.5</sub>
B	φ 60 <sup>+1</sup> <sub>0</sub>
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13 <sup>+1.0</sup> <sub>0</sub>
W1	1.2

#### TAPING STATE



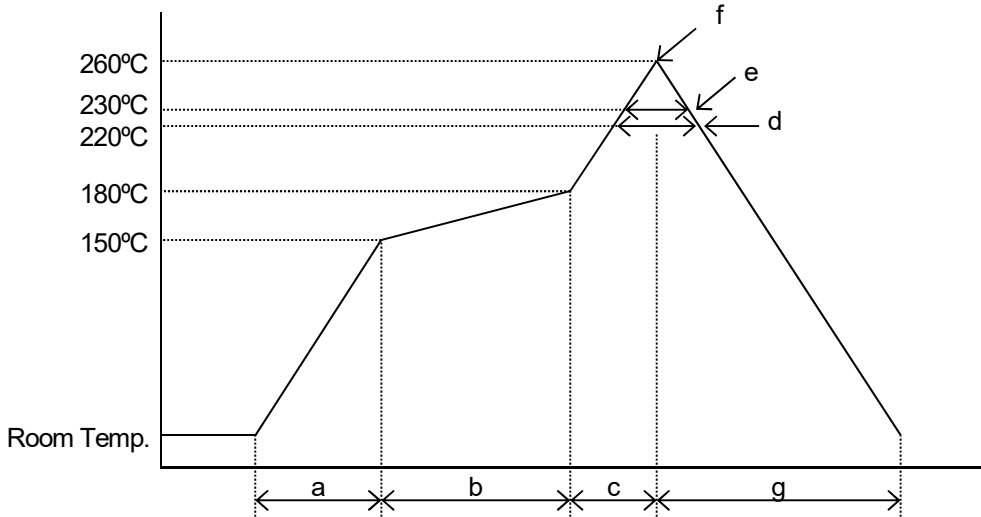
#### PACKING STATE



## ■RECOMMENDED MOUNTING METHOD

### INFRARED REFLOW SOLDERING METHOD

\*Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4°C/s
- b: Pre-heating temperature : 150 to 180°C  
Pre-heating time : 60 to 120s
- c: Temperature ramp rate : 1 to 4°C /s
- d: 220°C or higher time : Shorter than 60s
- e: 230°C or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260°C
- g: Temperature ramping rate : 1 to 6°C /s

The temperature indicates at the surface of mold package.

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