8bit 8ch D/A Converter

■ GENERAL DESCRIPTION

The NJW5211 is 8bit 8ch D/A converter for electronic adjustment. 8ch DC out put can be independently controlled by three-wire serial interface.

The NJW5211 features low operating voltage(2.7V) and can be full-swing outputted regardless of supply voltage.

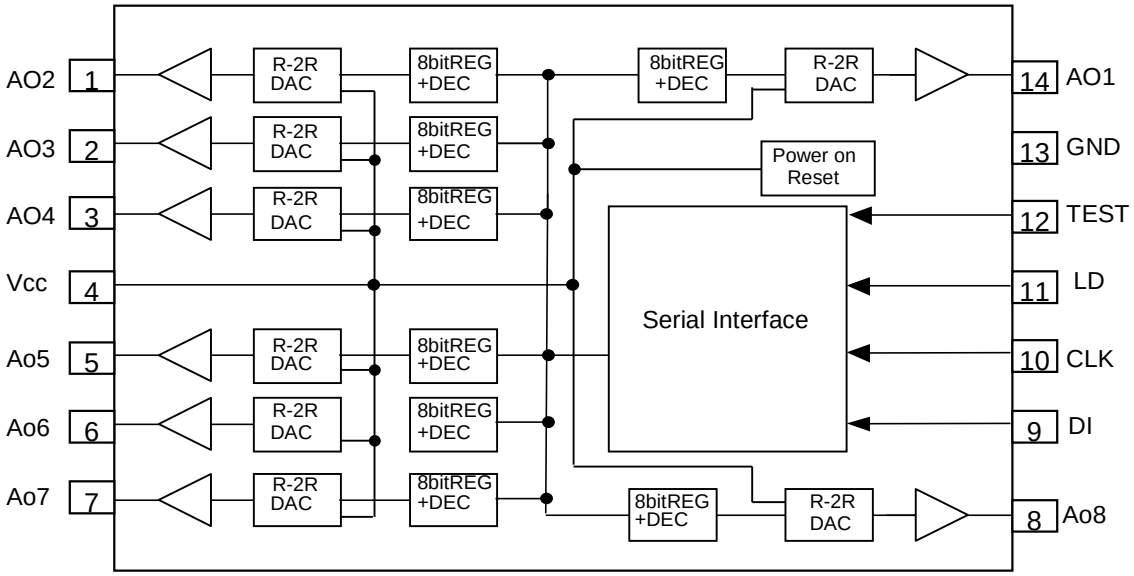
■ PACKAGE OUTLINE

NJW5211V

■ FEATURES

- Low Operating Voltage 2.7 to 5.5V
- 8bit 8ch D/A Converters Adopting R-2R System
- 3-wire 11-bit Serial Interface
- Internal POWER ON RESET Circuit
- Bi-CMOS Technology
- Package Outline SSOP14

■ BLOCK DIAGLAM and PIN DIAGRAM



Pin No.	Pin Name	IN/OUT	Description
1	AO2	OUT	Analog Output
2	AO3	OUT	Analog Output
3	AO4	OUT	Analog Output
4	Vcc	-	Vcc
5	AO5	OUT	Analog Output
6	AO6	OUT	Analog Output
7	AO7	OUT	Analog Output
8	AO8	OUT	Analog Output
9	D1	IN	Serial Data Input
10	CLK	IN	Serial CLK Input
11	LD	IN	Serial Load Input
12	TEST	-	TEST Terminal
13	GND	-	GND
14	AO1	OUT	Analog Output

■ **ABOSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	-0.3 to 7.0	V
Terminal Voltage	Vin	-0.3 to Vcc	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +150	°C

■ **RECOMMENDED OPERATING CONDITION** (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr		2.7	-	5.5	V
Analog Output Source Current	IOL		-	-	1.0	mA
Analog Output Sink Current	IOH		-	-	1.0	mA
Serial Clock Frequency	FSCLK		-	2.0	-	MHz
Limit Road Capacitance	CL		-	-	0.1	μF

■ **ELECTRICAL CHARACTERISTICS** (Vcc =3.0V, Ta=25°C)

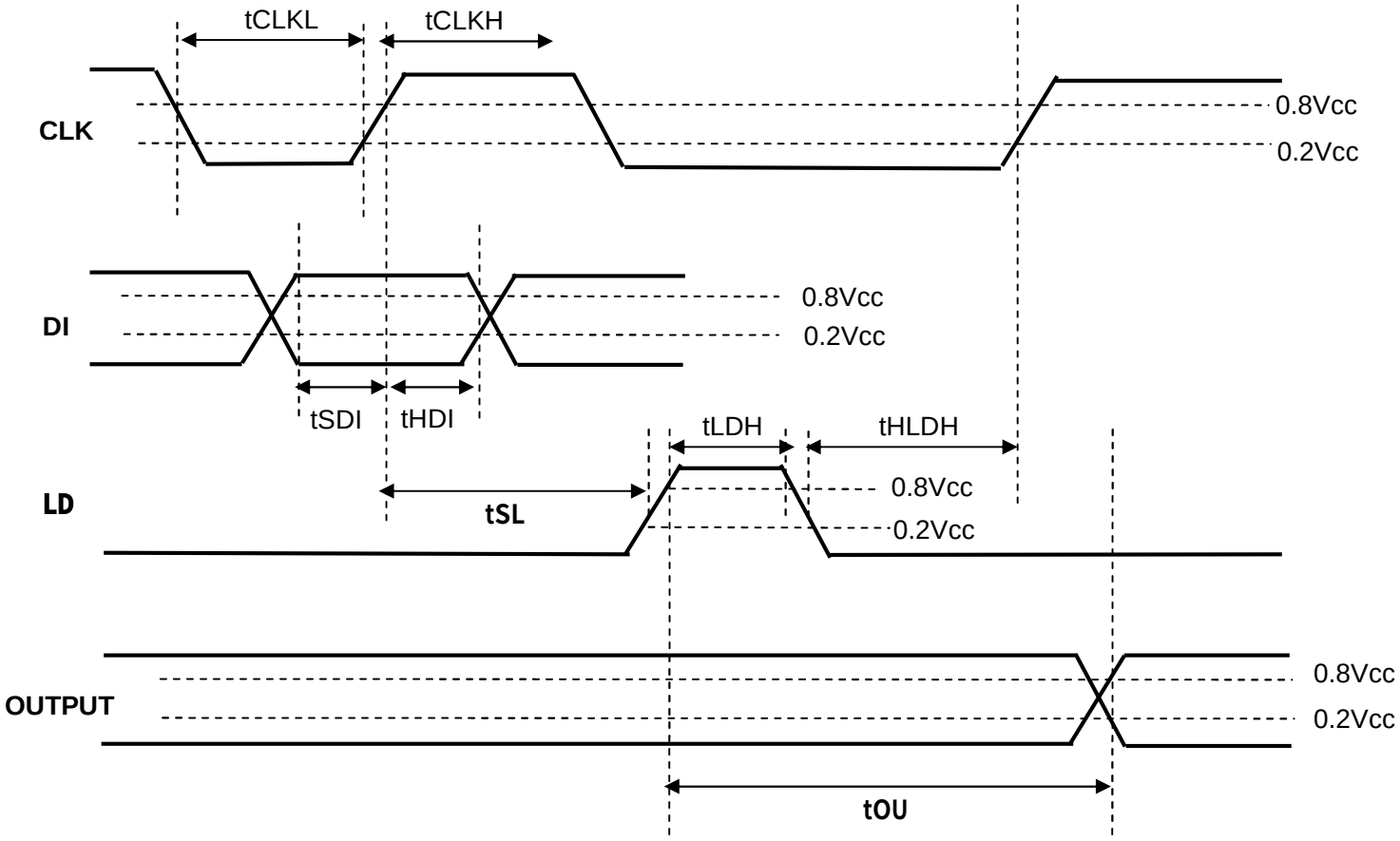
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	CLK=1MHz 80H set	-	0.75	1.5	mA
<Logic Interface>						
Input low voltage	VIL		0	-	0.3	V
Input high voltage	VIH		1.8	-	Vcc	V
Input low current	IIL		-	-	10	μA
Input high current	IIH		-	-	10	μA
<Buffer Amplifier>						
Minimum output voltage	ZS1	00H set IOH=0.0mA	0	-	0.1	V
	ZS2	00H set IOH=0.5mA	0	-	0.2	
	ZS3	00H set IOH=1.0mA	0	-	0.3	
Maximum output voltage	FS1	FFH set IOL=0.0mA	Vcc-0.1	-	Vcc	V
	FS2	FFH set IOL=0.5mA	Vcc-0.2	-	Vcc	
	FS3	FFH set IOL=1.0mA	Vcc-0.3	-	Vcc	
<DAC accuracy>						
Resolution	RES		-	8	-	bit
Difference non-linearity error	DNL	Input code 02H to FDH	-1.0	-	1.0	LSB
Integral non-linearity error	INL	Input code 02H to FDH	-1.5	-	1.5	LSB

■ **POWER ON RESET**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc supply voltage rise time	trVcc	Vcc=0 to 2.7V	100	-	-	μs
Power on reset voltage	VPOR		-	1.9	-	V

■ **Condition of operating timing**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CLK L level pulse width	tCLKL		200	-	-	ns
CLK H level pulse width	tCLKH		200	-	-	ns
DI setup time	tSDI		30	-	-	ns
DI hold time	tHDI		60	-	-	ns
LD setup time	tSLD		200	-	-	ns
LD hold time	tHLD		100	-	-	ns
LD "H" level pulse width	tLDH		100	-	-	ns
Analog output delay time voltage	tOUT	CL=50pF, RL=10kΩ	-	-	300	μs



*A signal level is judged at 80% or 20% of Vcc

■Command sending

Control command is 3wire 10bit serial interface.(MSB first)
Data is taken in with rise edge on the CLK and output data is fixed in the LD high section.
Data is maintained in the LD low section.

LSB(LAST) MSB(FIRST)

Data set								Channel select		
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10

Data Set

D0	D1	D2	D3	D4	D5	D6	D7	Analog output voltage level
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(Vcc-GND)/256x1
0	1	0	0	0	0	0	0	(Vcc-GND)/256x2
1	1	0	0	0	0	0	0	(Vcc-GND)/256x3
0	0	1	0	0	0	0	0	(Vcc-GND)/256x4
:	:	:	:	:	:	:		:
0	1	1	1	1	1	1	1	(Vcc-GND)/256x254
1	1	1	1	1	1	1	1	(Vcc-GND)/256x255

Channel select

D8	D9	D10	Address select
0	0	0	AO1
1	0	0	AO2
0	1	0	AO3
1	1	0	A04
0	0	1	A05
1	0	1	AO6
0	1	1	AO7
1	1	1	AO8