SOLO MOTOR CONTROLLERS

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SOLO SOM — HARDWARE USER MANUAL

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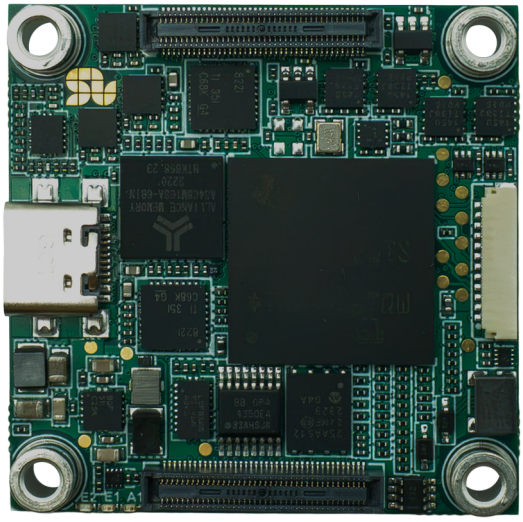

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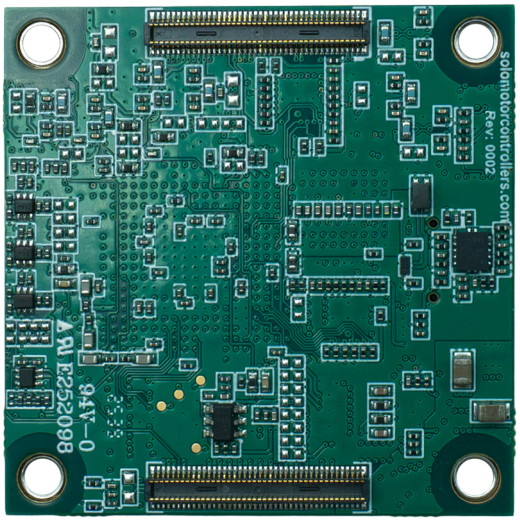

BOTTOM

EtherCAT CANopen

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1. ABOUT THIS DOCUMENT

1.1 PURPOSE AND SCOPE

The SOLO SOM is a 40 × 40 mm System-on-Module that implements the complete digital control section of a motor controller. It is built around the Texas Instruments TMS320F28388D dual-core DSP and contains the control processor, the analog front end for current and voltage sensing, the position-sensor interfaces, and the EtherCAT, CANopen, USB, and UART communication transceivers. In a motor drive, the digital control section is the part that demands the most engineering effort and validation time. The SOLO SOM provides it as a single qualified component, so the user supplies only the power stage and the system connectors, and the module performs the control function.

The module is organized as two processing cores with distinct roles:

- **Motion Core (CPU1).** Programmed and maintained by SOLO, this core runs the production motor-control firmware: Field Oriented Control of the motor, the position-sensing interfaces, and the EtherCAT and CANopen communication stacks. It requires no firmware development. The user configures it through the SOLO Motion Terminal and commands it over the communication interfaces.
- **User Core (CPU2).** Fully open and user-programmable, this core runs the user's own C application on a second 200 MHz processor with its own analog and digital I/O. It removes the need for a separate microcontroller for auxiliary functions such as a DC-DC converter, a power-factor-correction stage, or supervisory logic.

For a power electronics engineer, the SOLO SOM is a tool for reducing both the development cost and the unit cost of a drive. The power stage is where most of a drive's cost and design risk reside, and where the engineer's expertise is best applied; by delegating the entire digital control section to a pre-engineered module, the design effort concentrates on the power stage, the time to a working drive is shortened, and the recurring component and assembly cost of the digital section is reduced to that of a single module. Because the module does not fix the power rating, the same control platform serves designs ranging from a low-voltage drive to a high-power industrial inverter with no limitation for voltage, current or Power on the Motor.

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This manual specifies the electrical and mechanical characteristics, the full connector pinout, the communication interfaces, the supported position sensors, and the procedure for developing firmware on the User Core. It provides the information required to design an interface board around the module and to commission a drive.

The reader is assumed to be familiar with power electronics and digital interfacing. No prior experience with this specific module is assumed. Where a design constraint is not self-evident, the text states the underlying reason so that it can be applied correctly to a given system.

1.2 SAFETY SYMBOLS

Four callout types appear throughout this manual. They follow the ANSI Z535 convention, in which the severity of the potential consequence determines the label:

Symbol	Meaning
i NOTE	Additional information or guidance. No risk of damage.
⚠ CAUTION	Possible minor equipment damage or data loss if disregarded.
⚠ WARNING	Possible personal injury or significant equipment damage.
⛔ DANGER	Immediate risk of serious injury or death.

> ⛔ **DANGER:** Do not connect or disconnect the SOLO SOM while the interface board is powered. Mating a high-density connector under power can momentarily short adjacent contacts, which is sufficient to destroy the module or cause injury if the power stage is energized.
>
> ⚠ **CAUTION:** The module contains ESD-sensitive components. Handle it at a grounded workstation, use a wrist strap, and retain it in antistatic packaging until installation.

1.3 ABBREVIATIONS

Abbreviation	Definition
ADC	Analog-to-Digital Converter
BiSS-C	Bidirectional Serial Synchronous, protocol C (an open absolute-encoder standard)
CAN	Controller Area Network
CLA	Control Law Accelerator (a co-processor within the TI DSP)

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Abbreviation	Definition
DAC	Digital-to-Analog Converter
DFU	Device Firmware Upgrade (entered via the active-high forced-boot pin, DFU1)
DSP	Digital Signal Processor
EnDAT	Encoder Data protocol (Heidenhain)
ESC	EtherCAT Slave Controller
FOC	Field Oriented Control
GND	Ground
INC	Incremental (encoder type)
IPC	Inter-Processor Communication
JTAG	Joint Test Action Group (standard debug interface)
LSS	Layer Setting Services (CANopen — sets node ID and bit rate)
PFC	Power-Factor Correction
PHY	Physical Layer transceiver (here, the Ethernet line driver)
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse-Width Modulation
RS-422 / RS-485	Differential (balanced-line) serial signalling standards
RTD	Resistance Temperature Detector (e.g. PT1000)
SOM	System-on-Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
VCP	Virtual COM Port

1.4 REVISION HISTORY

Rev	Date	Firmware	Author	Summary of Changes
V1.0.0	31/05/2023	0x0000B00F	SOLO Motor Controllers	First release
01	2026-06-24	—	SOLO Motor Controllers	Expanded hardware manual

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1.5 FURTHER INFORMATION

This manual covers the **hardware** of the SOLO SOM. Everything beyond it is documented separately on the SOLO website, **solomotorcontrollers.com**: configuring and tuning the drive with the **SOLO Motion Terminal**, the **CANopen (DS402)** and **EtherCAT** communication profiles and their object dictionaries, **User Core (CPU2)** programming, and application notes.

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2. PRODUCT SAFETY

2.1 GENERAL SAFETY PRECAUTIONS

The SOLO SOM is the control element of a motor drive, which can deliver sufficient energy to cause injury or fire if misapplied. Review this section before applying power.

The module logic operates primarily at 3.3 V. The DSP pins at this level are **not** 5 V tolerant: applying more than 3.3 V to such a pin can permanently damage that pin or the device. Certain pin groups are rated higher. The single-ended encoder inputs tolerate up to 5.2 V and the Hall inputs up to 5.5 V, for example, but the rating of each group must be confirmed against the absolute-maximum table in Section 7.5 rather than assumed.

> ⚠ **WARNING:** The 3.3 V pins are not 5 V tolerant. Applying more than 3.3 V to a 3.3 V pin, even briefly, can permanently damage the device.
>
> ⚠ **CAUTION:** Treat every I/O pin as 3.3 V nominal unless Section 7.5 states otherwise. Confirm the rating of a pin group before connecting it to 5 V or 12 V logic.
>
> ⚠ **CAUTION:** The module contains SDRAM and two fine-pitch connectors. Support the board during mating to avoid flexing the PCB or deforming the connector contacts.
>
> ⚠ **CAUTION:** The two switched 5 V outputs (+5V_OUT_P and +5V_OUT_S) are intended solely to supply encoders and Hall sensors. Each provides up to 500 mA of continuous current and is protected by an on-board e-fuse (TPS2001EDBVR) that trips when the draw exceeds approximately 2 A. Do not connect other loads to them. Overloading will trip the e-fuse or cause a brownout of the position feedback during operation.
>
> ℹ **NOTE:** Limit encoder and Hall sensor cables to 3 m, and connect the cable shield to ground at one end only. Grounding a shield at both ends forms a ground loop that injects noise into the feedback signals.

The module is a component intended for integration, not a finished product. The complete system must comply with the standards applicable to its market and application. For industrial drives, this is typically the IEC 61800 series. Protection functions such as over-current trip, over-voltage clamp, and thermal shutdown are implemented partly in firmware and partly in interface-board hardware. The interface-board hardware is the responsibility of the integrator.

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2.2 INTENDED USE

The SOLO SOM is the digital control section of a motor controller or servo drive. It is mounted on a user-designed interface board that provides the power stage, the gate drivers, the current-sense shunts and amplifiers, and the protection circuits. The module cannot drive a motor on its own, as it contains no power semiconductors.

2.3 PROHIBITED USE

Do not use the SOLO SOM in any of the following ways:

- As a standalone product without an interface board.
- In a safety-critical application without an independent safety system.
- Outside the specified temperature range.
- In an environment subject to condensation or to conductive dust and contamination.
- As a general-purpose 5 V supply. The +5V_OUT_P/S rails are for position sensors only.

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3. PRODUCT OVERVIEW

3.1 DESIGN CONCEPT

In a typical motor controller, most of the cost and design risk reside in the power stage: the switching transistors, the gate drivers, the bus capacitors, and the thermal design. The digital section (the processor, the encoder interfaces, the communication transceivers) is smaller in scale, but the firmware and the analog front end require substantial engineering effort to develop and validate.

The SOLO SOM, shown in Figure 1, packs that entire digital section into a single 40 × 40 mm module.

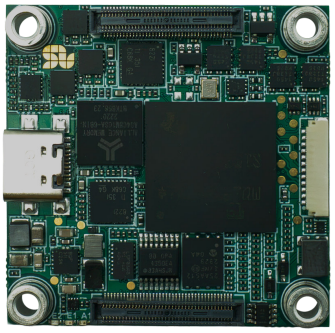

Figure 1. The SOLO SOM — a complete 40 × 40 mm digital motor-control module.

The SOLO SOM separates these two domains. It integrates the entire digital section into one 40 × 40 mm module that is pre-designed, tested, and running production firmware. The user designs the power stage to the required voltage and current ratings, routes the necessary signals to the module through an interface board, and the module executes the control loops. Because the power rating is not fixed by the module, a single control platform scales from a low-voltage drive to a high-power industrial inverter, and development time is reduced relative to designing the digital section from the start.

The module also provides a second, fully open DSP core. The user can run custom C code on it (a DC-DC converter, a power-factor-correction stage, or a supervisory routine, for example) without adding a separate microcontroller, reducing board area, bill-of-materials cost, and toolchain count.

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3.2 DUAL-CORE ARCHITECTURE — TWO INDEPENDENT CORES IN PARALLEL

The SOLO SOM is built on the dual-core TMS320F28388D, which provides two 32-bit C28x CPUs running in parallel at 200 MHz, each with its own double-precision floating-point unit and Control Law Accelerator. The two cores are assigned distinct, complementary roles: the **Motion Core** executes the production motor-control firmware, while the **User Core** is left fully open for the user's own application. They operate simultaneously and exchange data over an on-chip inter-processor link, so user code runs without interrupting the motor-control loops.

Motion Core (programmed and maintained by SOLO):

- Field Oriented Control with nested position, speed, and torque loops
- Drives BLDC, PMSM (surface-magnet and interior-magnet types), DC brushed, and EC coreless motors
- Two independent position-sensing channels (primary for control, secondary for monitoring), covering five encoder families
- EtherCAT with two on-board PHYs and DS402 device profiling
- CANopen (DS402) through an on-board CAN transceiver. The hardware is CAN FD capable
- USB Full-Speed (Type-C) for configuration and firmware updates through the SOLO Motion Terminal
- PT1000 temperature-sensor input for motor or heatsink monitoring

User Core (user-programmable):

- A dedicated 200 MHz C28x CPU with double-precision floating-point unit and Control Law Accelerator, independent of the Motion Core
- Up to 6 high-performance PWM outputs (EPWM5A/B, EPWM6A/B, EPWM7A/B) for an auxiliary converter, a chopper, or other timed switching functions
- Up to 5 parallel-sampled ADC channels, configurable 12- or 16-bit, in a 3 + 2 grouping (ADCINA4, ADCINB4, ADCINC4, ADCINA0, ADCINB0)
- 50 MHz SPI (SPID) for high-speed external devices (sufficient for protocols such as PROFINET)
- UART (SCIB TX and RX) for a serial link to an external host
- On-board JTAG connector for debugging with a standard TI probe

Hardware summary:

- 40 × 40 × 7 mm, 35 g
- 16 MB (128 Mbit) on-board SDRAM (used internally by the firmware)

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- Two 80-pin DF40 high-density connectors, accessible from both faces of the module
- Dedicated JTAG header and USB Type-C port

3.3 FUNCTIONAL BLOCK DIAGRAM

Figure 2 shows the functional block diagram of the SOLO SOM.

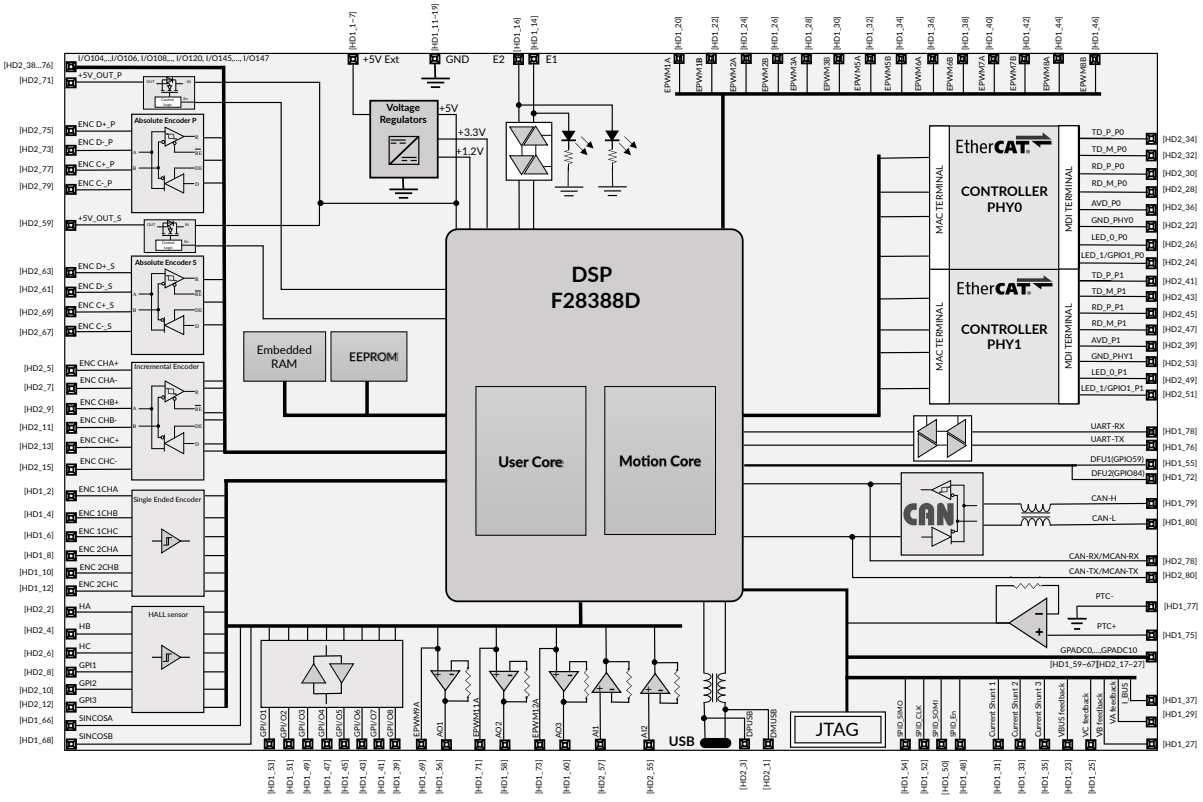

Figure 2. SOLO SOM functional block diagram.

3.4 CONTROL PRINCIPLE

This section describes the control function performed by the Motion Core. The function is built in and requires no user programming, but an understanding of it supports sensor selection, drive tuning, and interpretation of the feedback signals.

3.4.1 THREE-PHASE MOTORS AND FIELD ORIENTED CONTROL

A three-phase motor (BLDC or PMSM) produces torque through the interaction between the rotating stator field and the rotor magnets. Smooth, efficient torque requires that stator current be injected at the correct angle relative to the rotor. Field Oriented Control (FOC), also termed vector control, performs this function.

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FOC consists of three control loops nested one inside another. Each loop encloses the next and executes at a faster rate:

1. **Torque (current) loop.** The innermost and fastest loop, executing in step with the PWM switching (down to approximately 1 µs per update). Motor torque is proportional to winding current, so torque control is implemented as current control. The loop measures the phase currents, compares them with the demand, and adjusts the PWM duty cycles to regulate the current. The phase currents are measured at 12-bit resolution by default. A 16-bit option for the phase-current measurement is available on request.

2. **Speed loop.** Enclosing the torque loop and executing approximately ten times slower, this loop compares measured shaft speed with the demand and sets the torque reference. When the load increases and the motor decelerates, the speed loop commands additional torque. Speed is therefore regulated through torque rather than directly, because a motor is fundamentally a torque-producing device and speed is the result of applied torque acting against the load.

3. **Position loop.** The outermost and slowest loop. It compares commanded shaft position with measured position and sets a speed reference that reduces the error. This loop requires the torque and speed loops beneath it to be tuned first.

FOC requires four feedback quantities:

- **Phase current**, measured on the module from the interface-board shunt signals. Used by the torque loop.
- **Speed**, derived from the position sensor. Used by the speed loop.
- **Position**, from an encoder. This enables servo operation.
- **Rotor electrical angle**, computed on the module. Closed-loop control is not possible without it, because the controller would not know the correct direction in which to inject current.

Figure 3 shows the FOC architecture with its nested torque, speed, and position loops.

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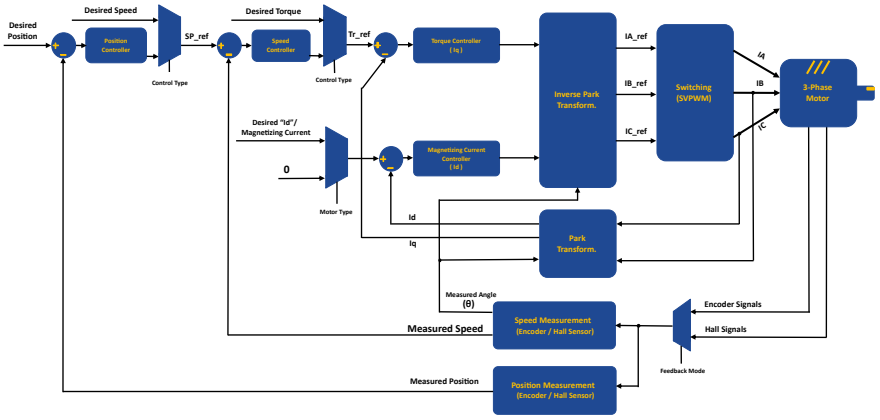

Figure 3. Field Oriented Control architecture for three-phase motors (nested torque, speed, and position loops).

3.4.2 DC BRUSHED MOTORS

A DC brushed motor is electrically simpler: commutation occurs mechanically through the brushes, so no rotor-angle computation or three-phase management is required. The SOLO SOM applies the same nested torque-speed-position structure with a single control channel rather than three, as shown in Figure 4. As with three-phase motors, adding an incremental encoder enables closed-loop position (servo) control.

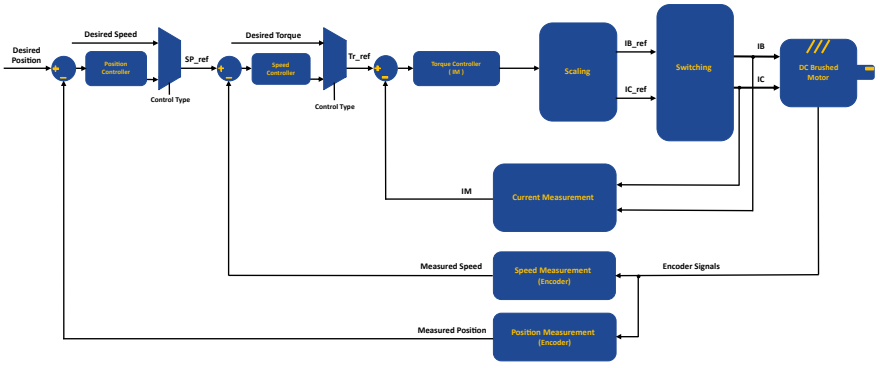

Figure 4. Cascade control architecture for DC brushed motors (single torque-speed-position channel).

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3.4.3 SENSORLESS CONTROL

The SOLO SOM can run a three-phase motor **without a position sensor**. Instead of reading the rotor angle from an encoder or Hall sensors, the Motion Core estimates it in real time from the motor's own electrical behaviour: the measured phase currents and the applied voltages. This removes the encoder, its cable, and its connector from the system, which lowers cost and eliminates a common point of failure. It suits fans, pumps, compressors, and other applications where a sensor is undesirable or impractical.

Sensorless estimation is inherently weak at very low speed, where the signals the estimator relies on become small. For the high-speed end, SOLO provides a dedicated **High-Speed Observer (HSO)** method, optimized to keep the angle estimate accurate and stable as the electrical frequency rises, the regime where high-pole-count or high-RPM motors operate. HSO lets the module drive high-speed motors reliably in sensorless mode, where a general-purpose estimator would lose tracking.

> ℹ **NOTE:** Sensorless and sensored operation use the same FOC structure described above; only the source of the rotor angle differs. A position sensor is still required where holding torque at zero speed or absolute position knowledge at power-up is needed.

3.5 ORDERING AND PART NUMBERS

Field	Value
Module part number	SLSG0XZ011
PCB assembly	SOLO SOM V02
HD1 top connector	DF40HC(4.0)-80DS-0.4V(58) — female, 80-pin, Hirose
HD1 bottom connector	DF40C-80DP-0.4V(58) — male, 80-pin, Hirose
HD2 top connector	DF40HC(4.0)-80DS-0.4V(58) — female, 80-pin, Hirose
HD2 bottom connector	DF40C-80DP-0.4V(58) — male, 80-pin, Hirose
JTAG connector	SM12B-SURS-TF — 12-pin, single-row, 1.0 mm pitch, SMD (JST)
USB port	USB Type-C

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3.6 MECHANICAL DRAWING

The fully dimensioned mechanical drawing of the SOLO SOM is shown in Figure 5. All dimensions are in millimetres. Use it to lay out the module footprint, mounting, and keep-out zones on the interface board and enclosure.

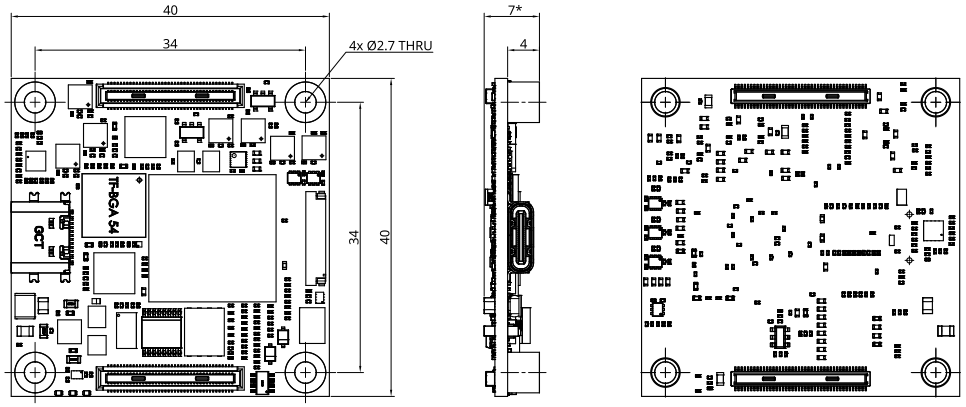

Figure 5. SOLO SOM V02 mechanical drawing — all dimensions in millimetres.

3.6.1 REAL PRODUCT VIEWS

Figure 6 and Figure 7 show the manufactured module from both faces, alongside the dimensioned drawing above.

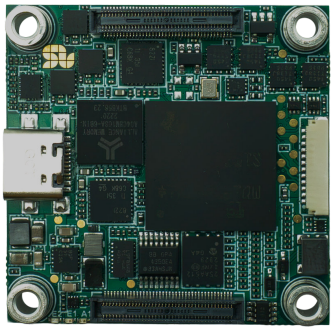

Figure 6. The SOLO SOM, top face (real product).

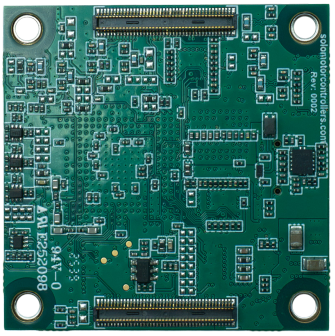

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Figure 7. The SOLO SOM, bottom face (real product), showing the second high-density connector.

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4. USER CORE — OPEN ACCESS

4.1 DUAL-CORE ALLOCATION

The TMS320F28388D contains two independent C28x CPUs, each with its own Control Law Accelerator (a co-processor that executes math-intensive control routines without loading the main CPU). The SOLO SOM allocates them between SOLO and the user:

Core	Function	Clock	Firmware
CPU1 — Motion Core	Motor control, EtherCAT, CANopen, encoder handling	200 MHz	Programmed and maintained by SOLO; not user-modifiable
CPU2 — User Core	User application	200 MHz	Fully open; programmed in CCS
CLA1	Associated with the Motion Core	200 MHz	SOLO
CLA2	Associated with the User Core	200 MHz	User

The User Core is a complete second processor at 200 MHz, with its own accelerator and a defined set of I/O, available without adding a separate device to the board. Typical applications are an auxiliary DC-DC converter, a power-factor-correction front end, and supervisory logic that would otherwise require a separate microcontroller. Figure 8 shows the User Core, its link to the Motion Core, and the I/O brought out to the connectors and JTAG.

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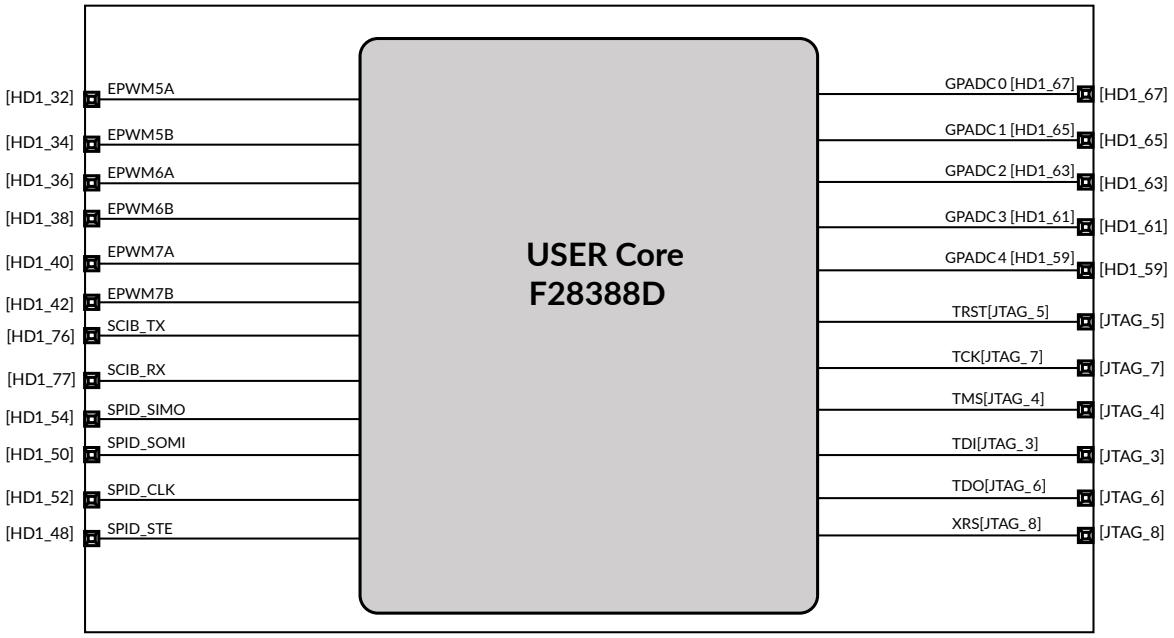

Figure 8. The User Core (CPU2 + CLA2), its relationship to the Motion Core over the IPC link, and the User Core I/O brought out to the connectors and JTAG.

4.2 INTER-CORE COMMUNICATION

The two cores share a block of RAM and a set of interrupt flags within the DSP, which together form the Inter-Processor Communication (IPC) channel. Through it, User Core code reads all Motion Core data (commanded and measured torque, speed, and position, and the current feedback) and returns commands, with under 1 µs of latency and no external wiring. The User Core can alternatively operate as a standalone processor, independent of the Motion Core.

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4.3 USER CORE RESOURCES

Resource	Detail	Pins
PWM outputs	Up to 6 high-performance channels: EPWM5A/B, EPWM6A/B, EPWM7A/B	HD1 even pins 32–42
ADC inputs	Up to 5 parallel-sampled channels, configurable 12- or 16-bit, in a 3 + 2 grouping: ADCINA4, ADCINB4, ADCINC4 plus ADCINA0, ADCINB0	See Section 9 pinout
SPI (SPID)	Full-duplex, rated to 50 MHz	HD1 even pins 48–54
UART (SCIB)	Full-duplex TX and RX, 3.3 V	HD1 pins 76, 78
JTAG	Debug access to the User Core through the on-board JTAG connector	JTAG connector

The five ADC channels are sampled in parallel (simultaneously), which is essential for measuring several signals at the same instant, such as the inputs and output of an auxiliary converter, and they can be configured for 12-bit or 16-bit resolution. The 3 + 2 grouping refers to three channels on separate ADC modules (ADCINA4, ADCINB4, ADCINC4) and two further channels (ADCINA0, ADCINB0).

4.4 DEVELOPMENT ENVIRONMENT

User Core code can be developed either by writing C directly with the Texas Instruments C2000 tools, or by generating it from a model in MATLAB/Simulink. Both paths target the User Core through the on-board JTAG connector.

Hand-written C, using the Texas Instruments C2000 tools:

- **Code Composer Studio (CCS):** TI's IDE, available at no cost from ti.com/tool/CCSTUDIO.
- **C2000Ware:** TI's driver library and example projects, from ti.com/tool/C2000WARE. Starting from an example project is the fastest method to bring up a peripheral.
- A **JTAG debug probe** connected to the on-board JTAG connector: TI XDS100V2, XDS110, or XDS200, or the general-purpose JTAG programmer offered by SOLO.

Model-based design, using MATLAB/Simulink:

Because the User Core (CPU2 and its CLA2) is reachable directly over the on-board JTAG connector, it can be programmed from MATLAB/Simulink without writing C by hand. The user builds a control model in Simulink, and the **Embedded Coder Support Package for Texas**

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Instruments C2000 Processors generates the corresponding C code, builds it, and loads it onto the User Core through a JTAG debug probe. This suits engineers who prefer to develop and verify a control algorithm as a block diagram and deploy it to the hardware directly.

- **MATLAB, Simulink, and Embedded Coder** with the **C2000 Processors** support package (from MathWorks).
- A **JTAG debug probe** connected to the on-board JTAG connector: TI XDS100V2, XDS110, or XDS200, or the general-purpose JTAG programmer offered by SOLO.

Deploying User Core code through the on-device bootloader:

A JTAG probe is needed only while developing and debugging the User Core application. Once the debug sessions are complete, the finished code can be loaded onto the User Core without a JTAG probe: SOLO provides an **on-device bootloader** that programs not only the Motion Core but also the User Core (CPU2). The user builds the application, connects the module over USB, and flashes it into the User Core through this bootloader, the same path used to update the module firmware (see Section 13.4). This lets production and field units receive User Core updates over USB alone, with no debug probe attached.

> **i NOTE:** The Motion Core firmware is supplied and supported by SOLO. It is not accessible to the user and cannot be modified: the core is locked, and the JTAG connector reaches only the User Core (CPU2 and its CLA2). No access to the Motion Core is required, since the user interacts with it through the SOLO Motion Terminal and the communication interfaces. The User Core, by contrast, is fully open, with no locked regions or licensing restrictions.

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5. DESIGNING A MOTOR DRIVE AROUND THE SOLO SOM

This section describes how to build a complete motor drive around the SOLO SOM at the architectural level. Section 6 specifies the individual interface-board connections. This section places those connections in context, showing how the module, the interface board, and the power (drive) stage fit together and which signals must flow between them for the module to run a motor.

A complete drive is made of three parts:

- **SOLO SOM:** the digital controller. It executes the motor-control loops and the communication stacks, but contains no power components.
- **Interface board:** the user-designed PCB that adapts the module to the power stage. It conditions analog signals into the module's 0–3.3 V range, level-shifts and routes the PWM, distributes power, carries the protection/fault signals, and holds the external connectors.
- **Drive (power) stage:** the gate drivers, the inverter (power transistors), the DC bus, the current-sense shunts, and the motor connections. This is the part the user designs to the required voltage and current rating.

5.1 OVERALL SYSTEM ARCHITECTURE

Figure 9 shows the three parts of the drive and the signal groups that pass between them: power and the conditioned feedback flowing from the drive stage through the interface board to the module, and the PWM and control signals flowing from the module back out to the drive stage.

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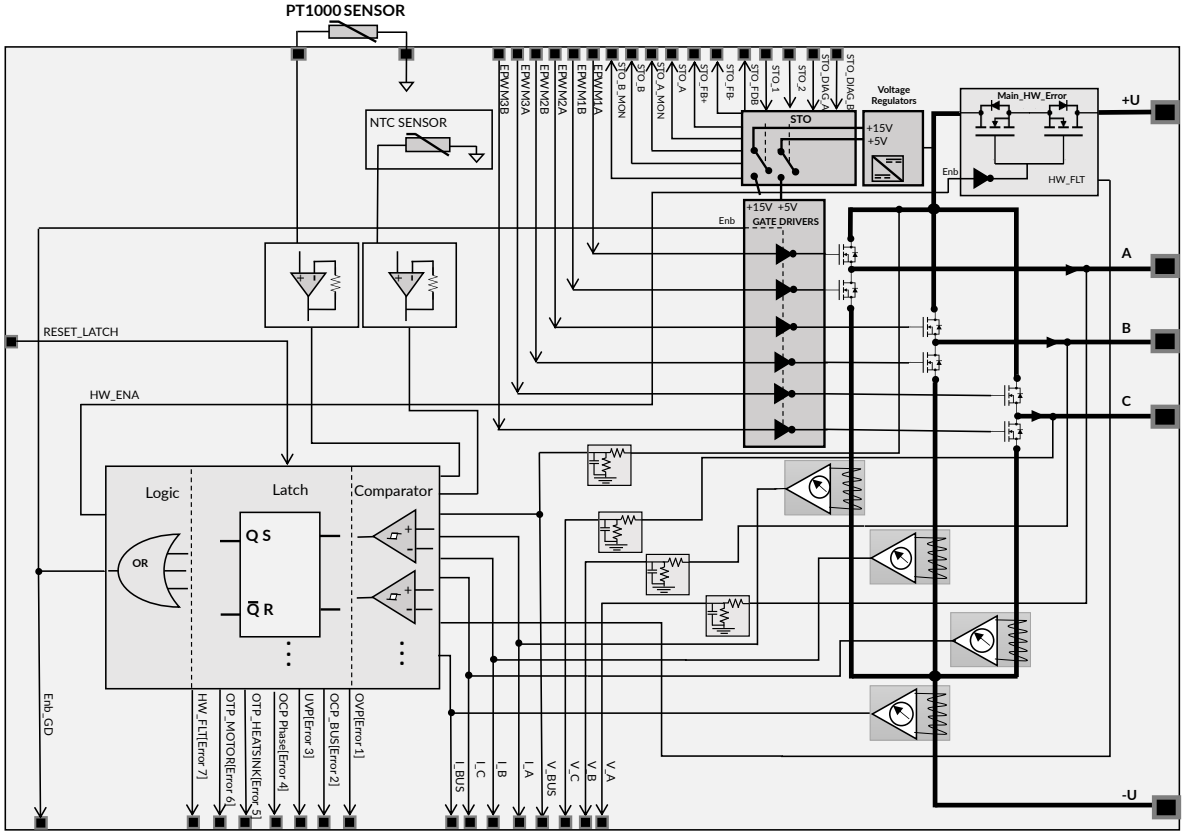

Figure 9. Overall drive architecture — the SOLO SOM, the interface board, and the power stage, with the signal groups exchanged between them.

In a typical build, the interface board sits between the module and the power stage. The module mates to the interface board through the HD1 and HD2 connectors. The interface board carries the gate-driver PWM, the conditioned current and voltage feedback, the encoder and Hall signals, the communication links, and the supply. The power stage connects to the interface board through the gate-driver inputs, the shunt-amplifier outputs, the bus-voltage divider, and the protection/fault outputs.

5.2 DRIVE-STAGE INTEGRATION AND I/O REQUIREMENTS

For the Motion Core to run a motor controller, a defined set of signals must pass between the module and the drive stage. Figure 10 shows these signals at the drive-stage boundary. The list that follows describes each group and points to the section with the detailed electrical requirements.

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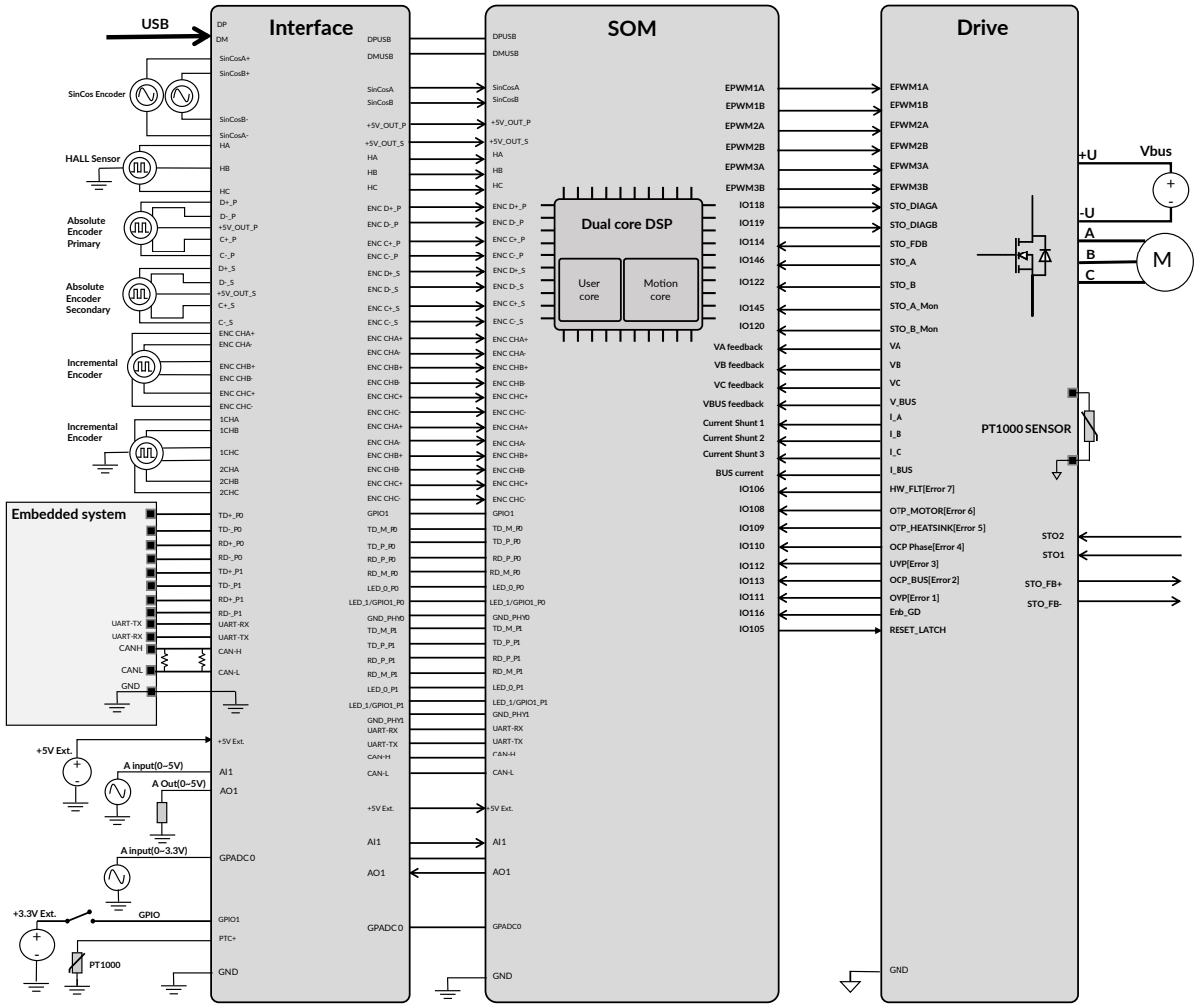

Figure 10. Full wiring of a drive built around the SOLO SOM, showing the signals exchanged with the drive stage.

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Signal group	Direction	Purpose	Detailed requirements
Gate-driver PWM	SOM → drive stage	Six PWM outputs (EPWM1A/B–EPWM3A/B) drive the three half-bridges of the inverter through the gate drivers. The module outputs 3.3 V logic; the gate driver provides level-shifting and isolation.	Section 6.3
Phase current measurement	drive stage → SOM	The three phase-shunt currents are amplified and fed to the module's ADC as bipolar signals centred on 1.65 V. Required by the torque (current) control loop.	Section 6.3
Bus current measurement	drive stage → SOM	The DC bus-shunt current, conditioned the same way as the phase currents (1.65 V-centred).	Section 6.3
Phase and bus voltage feedback	drive stage → SOM	The three motor terminal voltages and the DC bus voltage, attenuated to the 0–3.3 V range. Used for control and protection.	Section 6.3
Hardware fault / error signals	drive stage → SOM	Seven latched, active-high hardware fault inputs (bus OVP / OCP / UVP, phase OCP, heatsink and motor OTP, and a general fault). The hardware detects and latches each fault; the firmware then identifies it and reports it over the communication buses and the error LED.	Section 5.3
Position feedback	encoder → SOM	Encoder or Hall signals for commutation, speed, and position (see Section 11).	Section 11
Power	interface board → SOM	The 5 V module supply (the interface board derives it from the system supply).	Section 6.3

ℹ NOTE: The SOLO SOM has no on-module hardware protection for the motor (see Section 7.5). Over-current, over-voltage, and over-temperature trips run in firmware, acting on the conditioned feedback above. The drive stage must therefore provide its own independent hardware protection (fuses, a desaturation-detecting gate driver, or a hardware over-current comparator, for instance) and route the resulting fault signal into the module, as detailed in Section 5.3, so both layers act together.

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5.3 HARDWARE FAULT DETECTION AND LATCHING

A motor drive must react to certain faults faster than any software loop can: a phase short or a bus over-current has to be cleared within microseconds to avoid destroying the power stage. For this reason, **high-speed detection of hardware faults is the responsibility of the drive (hardware) designer, not the SOM firmware.** The hardware must detect each fault and **latch** it, then present the latched state to the module. Detecting these faults in the DSP alone cannot meet the timing required for protection and is not a substitute for hardware detection.

The SOLO SOM accepts **seven hardware fault inputs**, presented on its GPIO inputs (see Section 9.2). Each input is:

- **Active-high:** a high level signals a fault.
- **Latched in hardware:** once a fault occurs the input is held asserted until the system clears it, so even a brief transient is captured.

Once a fault input is asserted, the Motion Core firmware identifies which fault occurred and reports it to the user over the communication interfaces (USB, UART, CAN, EtherCAT) and on the error LED (Section 12). The firmware reports and responds to faults the hardware has already caught. It does not perform the high-speed protection itself.

Input	Fault indicated	What the drive designer must do
OVP	DC bus over-voltage	Tune the hardware to trip (latch) this input whenever a bus over-voltage is detected
OCP_BUS	DC bus over-current	Tune the hardware to trip this input whenever a bus over-current is detected
UVP	DC bus under-voltage	Tune the hardware to trip this input whenever a bus under-voltage is detected
OCP_Phase	Motor phase over-current	Tune the hardware to trip this input whenever a phase over-current is detected
OTP_Heatsink	Heatsink over-temperature	Tune the hardware to trip this input whenever the heatsink exceeds its temperature limit
OTP_Motor	Motor over-temperature	Tune the hardware to trip this input whenever the motor exceeds its temperature limit
HW_FLT	General hardware fault (catch-all)	Latch any other hardware fault into this input

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The general fault input (HW_FLT). HW_FLT is a catch-all for any hardware fault not covered by the six specific inputs. It also offers a simplified option: where a design cannot latch and route all seven faults separately, perhaps for want of latch circuitry or spare I/O, tie the six specific inputs to their inactive (low) level and OR every hardware fault into HW_FLT. The drive will still report a hardware fault, but without per-fault detail: the firmware flags a general hardware error rather than naming the specific cause.

> ⚠ **WARNING:** High-speed hardware fault detection and latching is the responsibility of the drive designer. The SOM firmware reports and reacts to latched faults, but it cannot detect them with the timing needed to protect the power stage. Implement hardware detection and latching for every fault that can damage the drive.
>
> ℹ **NOTE:** Drive every unused fault input to its inactive (low) level so it does not float. A floating active-high input can register a false fault.

5.4 SAFE TORQUE OFF (STO)

Safe Torque Off (STO) is a functional-safety function that brings a drive to a safe, torque-free state: it removes the torque-producing energy from the motor by disabling the path to the power stage, so the motor can no longer generate movement, while the rest of the system may remain powered. STO is the foundation for safe-stop functions in machinery (for example, Stop Category 0 under IEC 60204-1) and is a building block for higher-level safety functions.

In a drive built around the SOLO SOM, STO uses a **dual-channel, de-energize** architecture (1oo2). Two independent request signals from outside the drive, **STO1** and **STO2**, activate one opto-isolator per channel on the interface board. Each channel's logic then drives a load switch on its supply line, shown in Figure 11, that gates that channel's gate-driver supply rail: channel A gates **Vin1 → Vout1** and channel B gates **Vin2 → Vout2**. When STO is requested, both switches open and cut the power to the gate drivers, so the inverter physically cannot energize the motor. STO simply removes the gate-driver supply; whether those gate drivers are isolated or non-isolated is entirely the designer's choice. Because this trip path is implemented entirely in hardware on the interface board, it does not depend on the SOLO SOM firmware. The module's role is to **monitor and diagnose** the STO channels through the feedback and diagnostic signals below.

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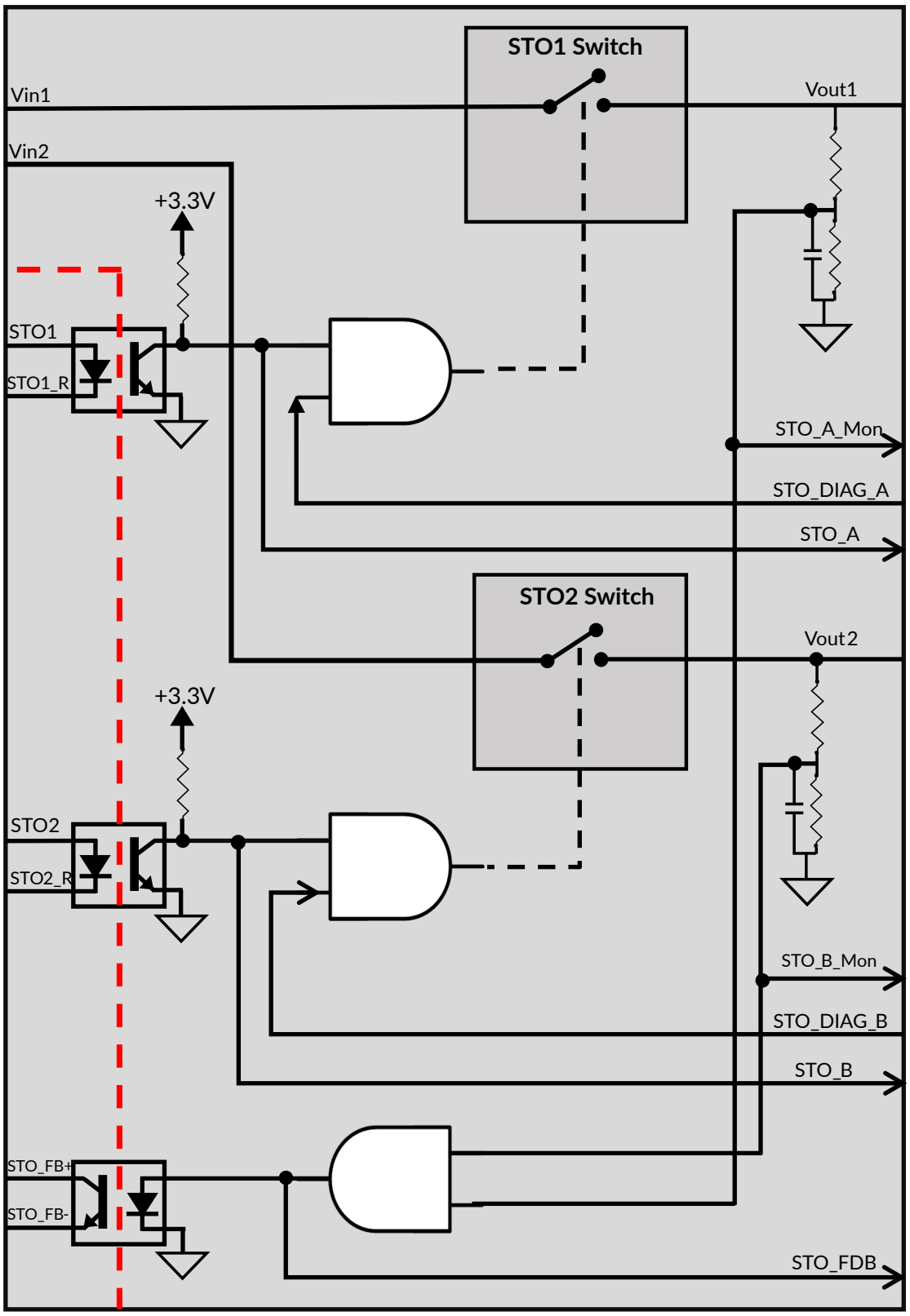

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Figure 11. STO wiring: two opto-isolated request channels (STO1 / STO2) drive load switches that gate the per-channel gate-driver supply rails (Vin1 → Vout1, Vin2 → Vout2). The SOLO SOM reads the channel feedback and injects the diagnostic signals.

The STO interface signals are:

Signal	Direction	Function
STO1, **STO2**	external → drive	The two STO request signals from outside the drive (for example, from a safety relay or safety controller). Each activates a per-channel opto-isolator that arms or trips the STO function.
STO1_R, **STO2_R**	external	The return (reference) path for the STO1 and STO2 request signals.
STO_A, **STO_B**	interface board → SOM	Feedback reporting the status of each channel's opto-isolator to the SOM.
STO_A_Mon, **STO_B_Mon**	interface board → SOM	Feedback taken **after** the voltage-line (load) switch, so the SOM can confirm that the gate-driver supply was actually removed.
STO_DIAG_A, **STO_DIAG_B**	SOM → interface board	Diagnostic signals the SOM drives, on demand, to test that each STO channel still trips correctly.

This follows the established industrial STO principle of two independent channels (1oo2, hardware fault tolerance 1), a de-energize trip that physically removes the gate-driver supply, and a diagnostic path through which the controller periodically verifies the function. Implemented and validated correctly, it can support drive safety functions up to SIL 3 (IEC 61508) and PL e, Cat. 3 (ISO 13849).

> ⚠ **WARNING:** The STO circuit shown here is built on the user's interface board and is the **integrator's responsibility**. SOLO provides only the SOM-side interface signals and this reference wiring; selecting and qualifying the STO components, and validating the complete safety function to the required level, is the responsibility of the machine builder. Do not rely on STO for personnel safety until the implementation has been verified and certified for the application.
>
> **i NOTE:** If the application does not require STO, the function can be bypassed and the SOLO SOM operates normally. To bypass on the SOM side: pull **STO_A**, **STO_B**, **STO_DIAG_A**, and **STO_DIAG_B** down to GND through a 1 kΩ resistor, and pull **STO_A_Mon** and **STO_B_Mon** up to 3.3 V through a 1 kΩ resistor.

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6. INTERFACE BOARD DESIGN GUIDE

6.1 FUNCTION OF THE INTERFACE BOARD

The interface board is the PCB designed to connect the SOLO SOM to the remainder of the drive. It carries the module's low-level signals to the power transistors and gate drivers, the current-sense shunts and amplifiers, and the connectors for the motor, the encoders, the network, and the supply. All functions required to control a motor but specific to the power stage are implemented on this board. Figure 12 shows the interface board sitting between the SOLO SOM and the power stage.

For designs based on a standard Texas Instruments evaluation inverter, SOLO supplies ready-made interface boards, which eliminate this design step for an initial prototype.

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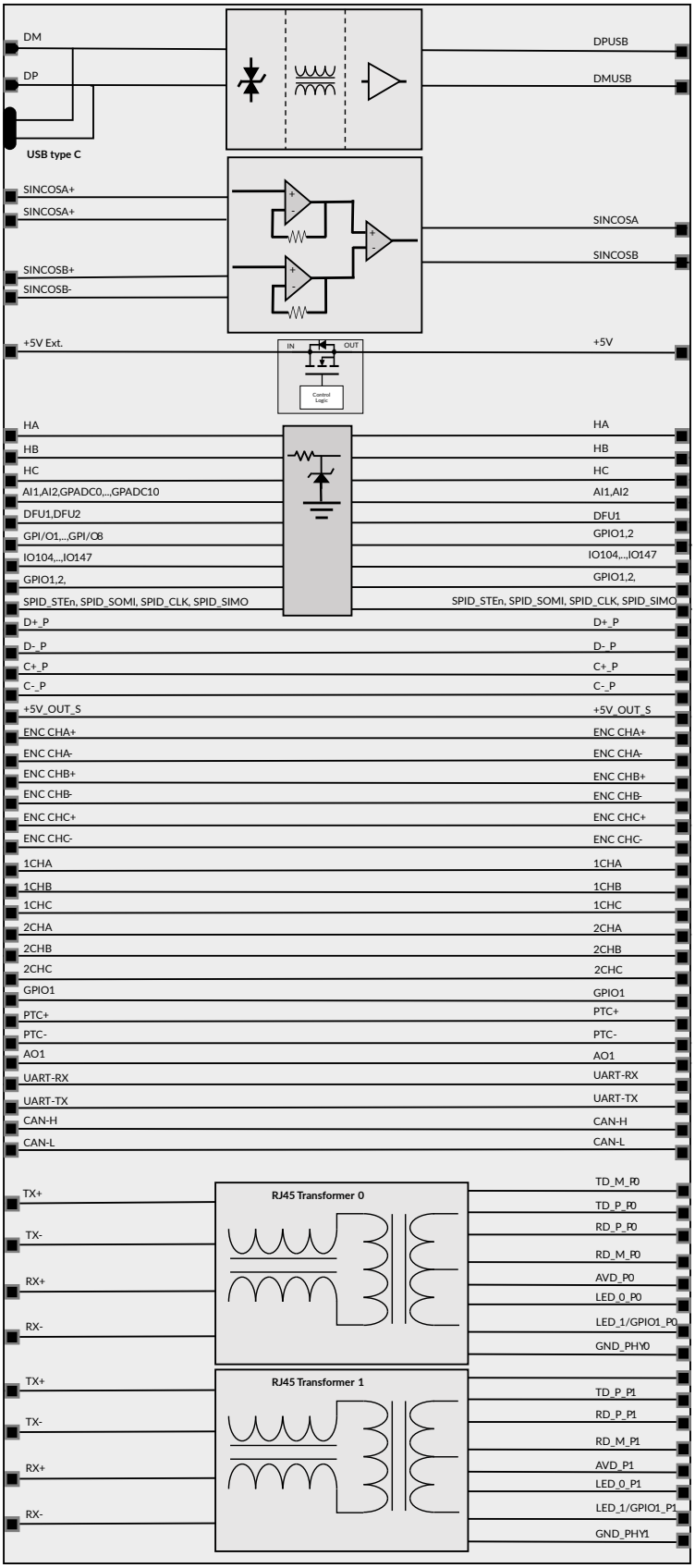

Figure 12. The interface board sits between the SOLO SOM and the power stage.

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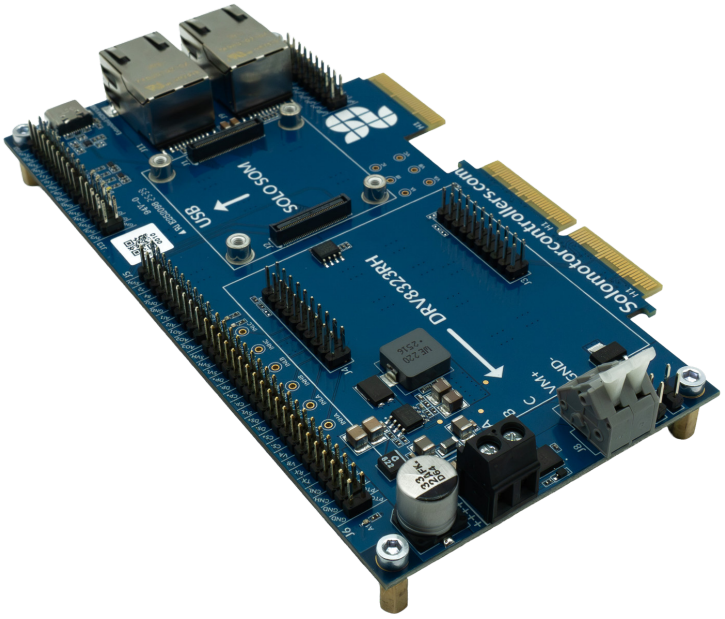
6.2 READY-MADE INTERFACE BOARDS FROM SOLO

Target inverter	TI board	Voltage range	Notes
BOOSTXL-DRV8323RH	TI BoosterPack	4.5–24 V	Low-voltage three-phase, 15 A peak
TMDXIDK379D	TI InstaSPIN IDDK	up to 400 V	High-voltage three-phase inverter

SOLO also provides fully open-source **evaluation boards** that mate the SOLO SOM to these inverters with no interface-board design required, so you can prototype a complete drive immediately. Section 14 lists the full family.



The open-source SOLO SOM evaluation board (Section 14).

6.3 REQUIRED CONNECTIONS

Four signal groups are mandatory. Without them the drive cannot run a motor:

- **Power.** Connect 5 V to the +5V_Ext pins (HD1 pins 1, 3, 5, 7, 9) and ground to HD1 pins 11, 13, 15, 17, 19. Connect all of them so the supply current is distributed across multiple contacts.
- **Gate-driver PWM.** Route the six motor PWM outputs, EPWM1A/B through EPWM3A/B (HD1 even pins 20–30), through the gate-driver devices to the inverter transistors. The module outputs 3.3 V logic. The gate driver performs the level-shifting and isolation.
- **Current sensing (phase and bus).** Route the three phase-shunt amplifier outputs and the DC bus-shunt output to HD1 odd pins 31, 33, 35, 37 (pin 37 carries the bus current). Each of these signals, including the bus current, must be a bipolar measurement centred on a

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precise **1.65 V** offset (mid-scale): zero current corresponds to 1.65 V, the maximum positive measurable current corresponds to **+3.3 V**, and the maximum negative measurable current corresponds to **0.0 V**. The amplifier on the interface board therefore sets this 1.65 V bias, and the measurement must be **symmetric** about it, with the same amplification gain on the positive and negative sides, so that the full-scale positive and negative currents are equal in magnitude. An accurate, stable 1.65 V reference is important here, because any error in the offset appears directly as a current-measurement error in the control loop. The DC bus current (pin 37) uses the same 1.65 V bias and symmetric scaling as the phase currents.

Each current channel must also include a low-pass filter immediately before the SOM input, to suppress switching noise and present an already-filtered signal to the ADC. The cut-off frequency depends on the channel: - **Phase currents:** between 20 kHz and 1 MHz, chosen for the application from the current rise time and the reaction time the control loop requires. Around **300 kHz** is a good general starting point. - **Bus current:** a much lower cut-off is appropriate; **2–5 kHz** is sufficient.

The Motion Core samples each phase current at the **centre of the PWM cycle**, the point where switching activity has settled and EMI and noise are at their minimum. Because the reading is taken at that instant, the current-sense chain (amplifier and filter) must be settled by the PWM centre. That is what sets the bandwidth requirement above. A measurement bandwidth of about **300 kHz is recommended**. A lower bandwidth may be used where the application allows, but keep it **at or above 20 kHz** so the amplifier settles in time. Below that the current reading degrades. Keep the source impedance driving the ADC input low so its sample-and-hold charges fully: use a light RC filter rather than a large series resistor ahead of the pin. - **Voltage feedback (phase and bus).** Route attenuated versions of the three motor terminal voltages and the DC bus voltage to HD1 odd pins 29, 27, 25, 23 (pin 23 carries the bus voltage). Unlike the current signals, these are unipolar: each voltage must be scaled so that **0 V at the motor or bus maps to 0 V at the pin and the maximum measurable voltage maps to 3.3 V**. For most designs a simple resistor divider provides this attenuation. Where isolation or a defined input impedance is needed, use a suitable amplifier instead, isolated or non-isolated according to the project's requirements. The DC bus voltage (pin 23) is conditioned in exactly the same way as the phase voltages.

Each voltage channel must include a low-pass filter immediately before the SOM input, with a cut-off frequency between **2 kHz and 4 kHz** and no higher. This cleans up the signal and presents an already-filtered voltage to the SOM.

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> ⚠ **CAUTION: leave headroom on every measurement.** Scale each current and voltage measurement so that the largest value expected in operation does **not** reach the ends of the 0–3.3 V range. Leave at least a **10 % window**: the worst-case signal should map to roughly 3.0 V instead of 3.3 V (and, for the bipolar current signals, to roughly 0.3 V instead of 0 V). If a measurement saturates, clipping at 0 V or 3.3 V, the firmware no longer sees the true current or voltage and can lose control of the drive, with possible damage to the hardware. Budget both a **control margin** (headroom for normal transients and regulation overshoot) and a **safety margin** (headroom for fault-level peaks) into the interface-board scaling.

The common requirement is the 0–3.3 V range. The DSP ADC reads only signals within this range, so every measured quantity, whether a 400 V bus voltage or a shunt voltage of tens of millivolts, must be conditioned by the interface board into 0–3.3 V before it reaches the module. This signal conditioning is a primary element of the interface-board design. Figure 13 shows the resulting current-measurement mapping, with bipolar current centred on the 1.65 V offset.

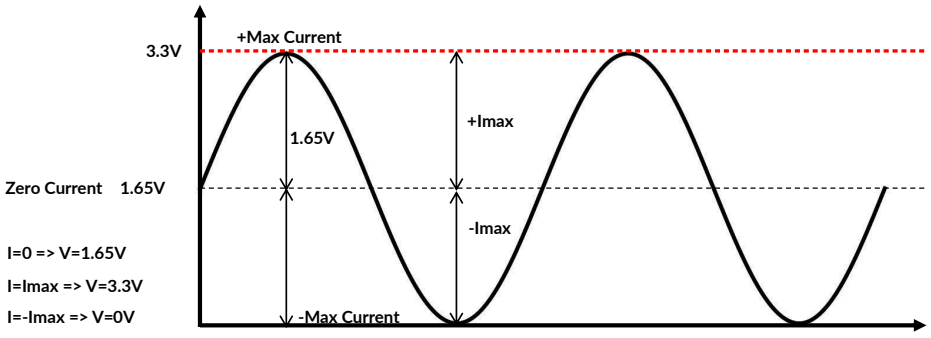

Figure 13. Current-measurement mapping: bipolar current centred on 1.65 V — zero current at 1.65 V, +Imax at 3.3 V, and –Imax at 0 V, with symmetric gain on both sides.

The interface board fixes the physical scaling, but that scaling does not have to be coded by hand. Through the SOLO Motion Terminal, the Motion Core firmware adapts to the user's declared parameters and learns the minimum and maximum value that each measurement represents at full scale: phase currents, bus current, phase voltages, and bus voltage. The user enters the scaling implemented on the interface board, and the firmware maps the 0–3.3 V ADC range to the correct engineering units for every signal.

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6.4 ANALOG AND DIGITAL I/O WIRING

Analog inputs AI1 and AI2 (0–5 V) connect on HD2 pins 57 and 55, and accept a 0–5 V command from a PLC or another controller. Ground the cable shield at one end only, and connect the module ground to the controller ground. An analog signal requires a shared reference. The wiring is shown in Figure 14.

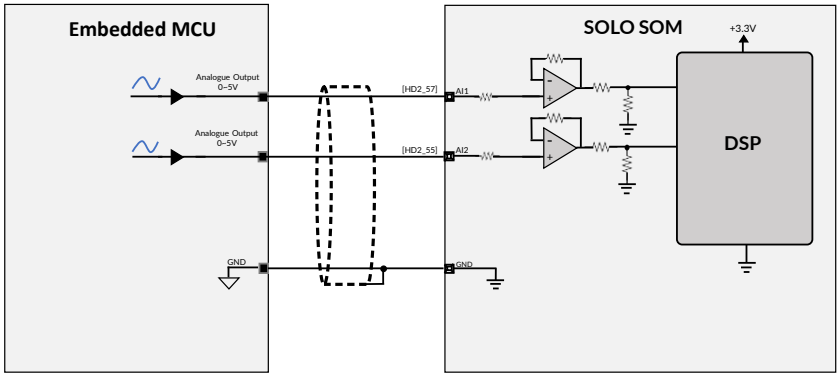

Figure 14. 0–5 V analog input (AI1 / AI2) wiring.

General-purpose ADC inputs (0–3.3 V) are the GPADC0–10 channels, for 0–3.3 V analog sources. The same shield and grounding requirements apply. The wiring is shown in Figure 15.

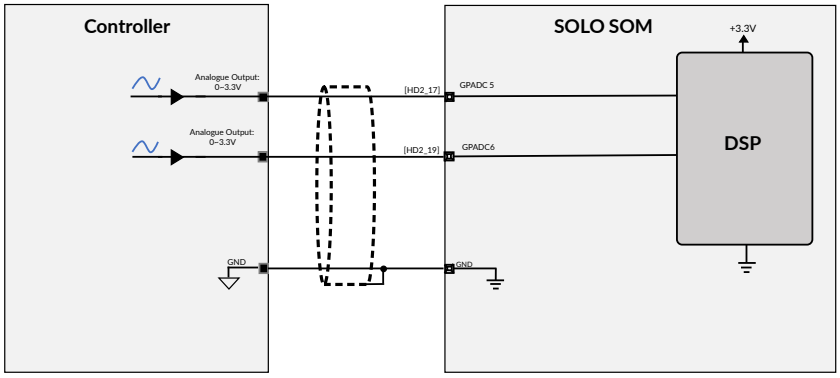

Figure 15. 0–3.3 V general-purpose ADC (GPADC) input wiring.

Analog outputs AO1, AO2, AO3 (0–5 V) connect on HD1 pins 56, 58, 60, and transmit an analog signal, a torque or speed value for example, to an external controller or instrument. The wiring is shown in Figure 16.

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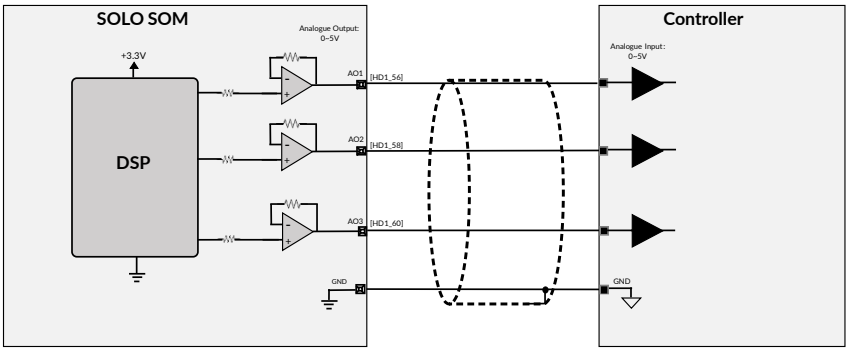

Figure 16. 0–5 V analog output (AO1 / AO2 / AO3) wiring.

Digital inputs (GPI1–GPI3 and the GPI/O pins) accept on/off logic signals. Observe the voltage rating of each pin group (Section 7.5) when wiring them. The wiring is shown in Figure 17.

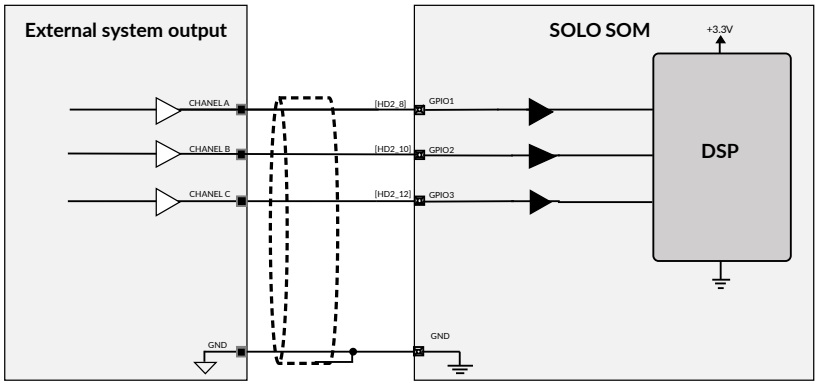

Figure 17. Digital input wiring.

Digital outputs (GPO1 and the GPI/O pins) drive an external logic load. GPO1 can source up to 5 mA. Use it to switch a transistor for heavier loads. The wiring is shown in Figure 18.

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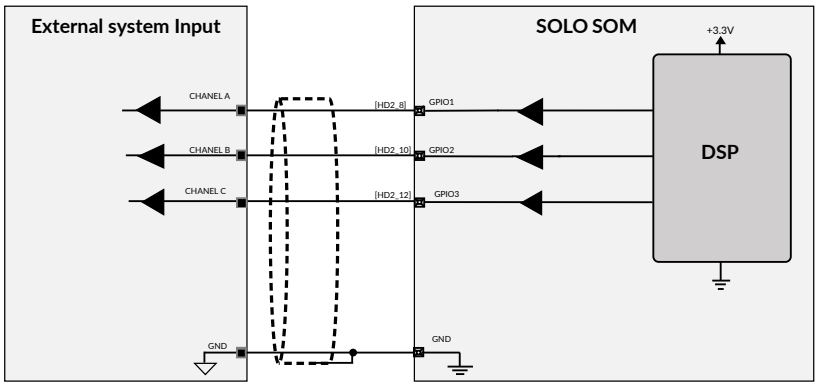

Figure 18. Digital output wiring.

6.5 OPTIONAL CONNECTIONS

Route these only where the application requires them:

Signal	HD pins	Recommended connector
EtherCAT port 0	HD2 pins 28–36	RJ45 via isolating LAN transformer (e.g. Würth 7499011448), or embedded magnetics module (e.g. Abracon ALANL100X1-DE12DT) — see Section 10.1
EtherCAT port 1	HD2 odd pins 39–53	RJ45 via isolating LAN transformer (e.g. Würth 7499011448), or embedded magnetics module (e.g. Abracon ALANL100X1-DE12DT) — see Section 10.1
CAN H/L	HD1 pins 79, 80	DB9 or M12; add an ISO1042 where isolation is required
USB D+/D−	HD2 pins 1, 3	USB-C or USB-B, with ESD protection at the connector
E1/E2 LEDs	HD1 pins 14, 16	Front-panel LEDs through a 470 Ω resistor
UART TX/RX	HD1 pins 76, 78	3-pin header or a DB9

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6.6 LAYOUT CHECKLIST

Item	Requirement	Priority
HD1 and HD2 footprints	Apply the Hirose DF40 land pattern without deviation	Mandatory
EtherCAT impedance	50 Ω single-ended, 100 Ω differential	Mandatory
Ground split	1206 capacitor between chassis and circuit ground near the magnetics	Mandatory
+5V_Ext decoupling	100 nF ceramic at the HD1 connector; ~100 µF bulk recommended, not required if the 5 V line is stable	Recommended
Feedback routing	Route feedback traces away from power traces; no parallel runs	Mandatory
Encoder ESD	TVS diode array on the encoder signal pins	Recommended
CAN isolation	ISO1042 or equivalent where the bus exits the enclosure	Recommended
USB ESD	USB ESD protection device at the connector	Recommended
Differential encoder termination	120 Ω across each RS-422 pair	Recommended

6.7 GROUNDING AND SIGNAL INTEGRITY

Clean grounding is the single biggest factor in obtaining accurate current and position feedback in a switching drive. Apply these principles on the interface board:

- **Single-point (star) ground to the power electronics.** The SOLO SOM is non-isolated: all of its GND pins form the system's low-voltage signal ground. Connect this module ground to the power-electronics ground (the gate-driver returns, the shunt power side, and the bus-capacitor return) at **one single star point only.** Do not bond the two grounds together at more than one place. A single connection stops the high-di/dt power-return currents from circulating through the module's ground and corrupting the measurements.
- **Partition power and analog returns.** Keep the high-current, high-di/dt power returns (gate drivers, shunts, bus capacitors) in their own region, and the quiet analog references (the 1.65 V bias, the current- and voltage-sense signals, and the ADC references) in a separate quiet region. The two meet only at the single star point above.

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- **Keep sensor grounds clean and avoid ground loops.** For the position sensors and other feedback devices, provide a clean ground reference and **avoid ground loops**: ground each cable shield at one end only (see Section 6.4) and do not create a second ground path between the sensor and the module. A ground loop drives circulating current and switching noise straight into the feedback, degrading both position and current accuracy.

Together with the feedback-routing and chassis/circuit-ground items in the Section 6.6 checklist, these rules keep the switching noise of the power stage out of the module's measurements.

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7. TECHNICAL SPECIFICATIONS

The following tables specify the values required to design the interface board and to verify operation within the rated limits. Where additional explanation is warranted, it is given in the accompanying text.

7.1 POWER

Description	Units	Value
DC supply voltage (continuous)	VDC	5
Module input current — idle	mA	≈ 200
Module input current — maximum	mA	1000
Maximum continuous output power (5 V line)	mW	500

The module operates from a single 5 V input and generates the internal 3.3 V logic and 1.2 V DSP core rails on board. It draws about 200 mA from the 5 V input at idle, rising to as much as 1000 mA at full load when it is simultaneously supplying multiple encoders and peripherals. Size the 5 V supply for at least 1 A to cover this worst case. The 500 mW figure is the power the 5 V line makes available to general external loads such as sensors. It is not the motor output power. A bulk capacitance of around **100 µF** at the module's 5 V input helps stabilise the rail and absorb transient current demand, but it is **not mandatory if the 5 V line is already stable**.

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7.2 CONTROL AND TIMING

Description	Units	Value
Analog speed/torque command	VDC	0–5 V analog, or a PWM input above 5 kHz
Digital direction control	VDC	0–3.3 / 5 V
Modes of operation	—	Torque, speed, position
Motors supported	—	DC brushed, BLDC, PMSM, EC coreless
Firmware protections	—	Bus over-voltage, bus over-current, motor phase over-current
Current (torque) loop sample time	µs	Synchronized to PWM frequency (1 µs minimum)
Current (torque) loop execution time	µs	1
Speed loop sample rate	kHz	4 (250 µs period)
Speed loop execution time	µs	75
Position loop sample rate	kHz	4 (250 µs period)
Position loop execution time	µs	75
Maximum encoder frequency — incremental	MHz	10
Encoder clock frequency — absolute (BiSS-C)	MHz	2 (min) to 8 (max)
Current measurement resolution	bit	12 (default); 16 optional for phase currents (on request)

The loop timing reflects the nested structure of Section 3.4: the torque loop samples as fast as every 1 µs, synchronized to the PWM frequency, while the speed and position loops run at 4 kHz (a 250 µs period). The supported encoder frequency depends on the encoder type: incremental encoders are supported up to 10 MHz, while the BiSS-C absolute interface operates with a clock frequency between 2 MHz (minimum) and 8 MHz (maximum). This BiSS-C range applies to both the primary and the secondary channel.

The SOLO SOM provides no hardware protection for motor control. The bus over-voltage, bus over-current, and motor phase over-current protections are implemented in firmware, acting on the measured bus voltage, bus current, and phase currents supplied by the interface-board sensing circuits. Because these protections depend on firmware execution and on the

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accuracy of the interface-board sensing, the interface board must also provide independent hardware protection (for example, fuses, a desaturation-detecting gate driver, or a hardware over-current comparator) appropriate to the power stage.

7.3 THERMAL & ENVIRONMENTAL

Description	Units	Value
Operating (board) temperature	°C	–20 to +120
Storage temperature	°C	–40 to +85
Operating humidity	% RH	5 to 95, non-condensing
Storage humidity	% RH	5 to 95, non-condensing
Operating altitude	m	up to 2000 (higher on request)
Vibration (recommended limit)	—	2 g, 10–500 Hz sinusoidal
Shock (recommended limit)	—	15 g, 11 ms half-sine
ESD immunity (device I/O pins)	kV	±2 (HBM, ANSI/ESDA/JEDEC JS-001)
Ingress protection (IP)	—	None — open board-level module
Conformal coating	—	Available on request
Cooling	—	Natural convection
MTBF	—	Available on request

The SOLO SOM has no heatsink and needs none. It is designed for natural-convection cooling and tolerates a board temperature up to 120 °C. It is an open board-level assembly with no ingress protection, so provide environmental protection at the enclosure level as the application requires. The operating altitude is rated to **2000 m** without derating; **on request, SOLO can evaluate qualifying the module for higher altitudes.** The vibration and shock figures are **recommended design limits**. Because all components and both board-to-board connectors are surface-mounted, secure the module firmly through its mounting provisions so the connectors stay supported, and validate the complete assembly for the shock and vibration of the target application.

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7.4 MECHANICAL

Description	Units	Value
Size (H × W × D)	mm	40 × 40 × 7
Weight	g	35
Board-to-board mated stack height	mm	4.0
Form factor	—	Wall mount

The board-to-board mated stack height of 4.0 mm is set by the mated DF40 connector pair (the "4.0" in the DF40HC(4.0)-80DS part number). Confirm it against the Hirose DF40-series datasheet for the exact assembled separation between the module and the interface board.

7.5 ABSOLUTE MAXIMUM VOLTAGE RATINGS

This table specifies, for each pin group, the maximum voltage that may be applied.

Two columns require careful interpretation. **Typical Max** is the maximum continuous voltage permitted at the pin in normal operation. Design to this value. **Absolute Max** is a short-transient limit that bounds voltage spikes and switching noise lasting microseconds. It is not a level to be applied intentionally. Designing to the Absolute Max value will result in eventual damage to the module.

> ⚠ **WARNING:** Design the interface board against the **Typical Max** column. The **Absolute Max** column bounds brief transients only. Continuously exceeding Typical Max will permanently damage the module.

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Section	Pin / Signal	Dir	Units	Min	Typical Max	Absolute Max
Supply input	+5V_Ext	Input	VDC	0	+5.5	+5.6
HD1	LED (E1/E2)	Input	VDC	0	+5.5	+5.6
HD2	Hall (HA/HB/HC)	Input	VDC	0	+5.5	+5.6
HD1	GPIO (GPI/O1–8)	Out/In	VDC	0	+5.0	+5.2
HD1	ENC single-ended	Input	VDC	0	+5.0	+5.2
HD1	PT1000-IN (PTC+/-)	Input	VDC	0	+3.3	+3.75
HD2	EtherCAT TD+/TD-	Input	VDC	0	+3.3	+3.75
HD2	EtherCAT RD+/RD-	Input	VDC	0	+3.3	+3.75
HD1	DFU1 (forced-boot) / DFU2	Input	VDC	0	+5	+5.25
HD2	+5V_OUT_P / +5V_OUT_S	Output	VDC	+4.95	+5.0	+5.05
HD2	ENC differential — incremental & BiSS-C	Input	VDC	0	+5.5	+6.0
HD2	Analog input (AI1 / AI2)	Input	VDC	0	+5.0	+5.2
HD1	UART_RX	Input	VDC	-0.5	—	+5.2
HD1	UART_TX	Output	VDC	-0.5	—	+5.2
HD1	CAN-H	—	VDC	-2	—	+7
HD1	CAN-L	—	VDC	-2	—	+7
HD2	GPO1	Output	VDC	0	+5.0	+5.2
HD2	GPI1	Input	VDC	0	+5.0	+5.2

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7.6 PROCESSING AND MEMORY

Parameter	Value	Notes
DSP	TMS320F28388D (ZWT package)	Dual-core C28x with two CLAs
CPU1 / CPU2 clock	200 MHz each	—
CLA clock	200 MHz	One CLA per core
SDRAM	16 MB / 128 Mbit (AS4C8M16SA)	On the module, used internally
PWM switching frequency	8 kHz to 150 kHz	Dependent on the motor and the required resolution
ADC sample rate	Up to 3.5 MSPS	Simultaneous sampling
EtherCAT cycle time	≥ 125 µs	Dependent on network configuration
IPC latency (CPU1 ↔ CPU2)	< 1 µs	Through shared RAM
SPI (SPID) max clock	50 MHz	User Core
CAN data rate	Up to 1 Mbit/s	Classical CAN; hardware is CAN FD capable
EtherCAT PHY data rate	100 Mbit/s	DP83822, 100BASE-TX

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8. MECHANICAL INTEGRATION

8.1 MODULE AND MOUNTING

The SOLO SOM is a double-sided board measuring 40 × 40 × 7 mm with a mass of 35 g. The two high-density connectors, HD1 and HD2, are present on **both** faces of the module with identical pinouts. The module can therefore be mated to the interface board from either face, as required by the enclosure, without any change to the signal assignment.

Each connector position uses a female socket on the top face and a male header on the bottom face. The on-board JTAG header and the USB-C port are available for commissioning and debugging. Figure 19 shows the top view with its dimensions, and Figure 20 the bottom view.

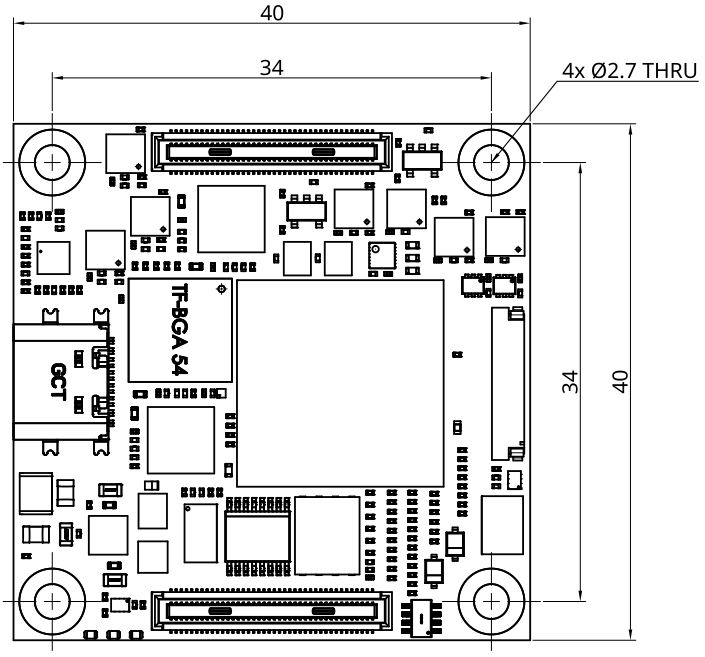

Figure 19. Top view of the SOLO SOM — all dimensions in millimetres.

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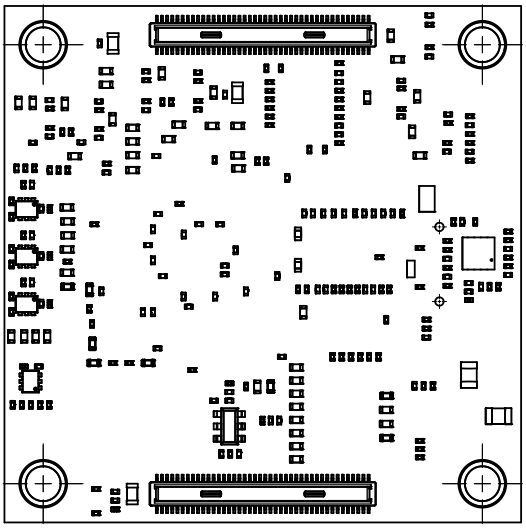

Figure 20. Bottom view of the SOLO SOM.

8.2 CONNECTOR SPECIFICATIONS

Connector	Part Number	Type	Pitch	Manufacturer
HD1 top	DF40HC(4.0)-80DS-0.4V(58)	Female socket, SMD	0.4 mm	Hirose
HD1 bottom	DF40C-80DP-0.4V(58)	Male header, SMD	0.4 mm	Hirose
HD2 top	DF40HC(4.0)-80DS-0.4V(58)	Female socket, SMD	0.4 mm	Hirose
HD2 bottom	DF40C-80DP-0.4V(58)	Male header, SMD	0.4 mm	Hirose
JTAG	SM12B-SURS-TF	12-pin single-row header, SMD	1.0 mm	JST
USB	USB Type-C receptacle	SMD	—	—

ℹ NOTE: The top and bottom pins of a given connector are connected one-to-one: HD1 top pin 1 is the same net as HD1 bottom pin 1, and likewise for HD2. The signal on a given pin number is therefore identical whichever face the interface board mates to; what changes between the two

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> faces is the mating connector's gender: male for top-side interfacing, female for bottom-side (see Section 8.3).

8.3 MATING FOOTPRINT DESIGN

On the interface board, the mating connector's gender is the **opposite** of the module face it mates against, because each module face already presents one gender (Section 8.2): the module's top face carries the female sockets and its bottom face the male headers. The connector to fit on the interface board therefore depends on which face of the module it mates to, and the same rule applies to both HD1 and HD2:

- **Top-side interfacing** (interface board mating the module's **top** face): fit the **male** connector, **DF40C-80DP-0.4V(58)** (Figure 22).
- **Bottom-side interfacing** (interface board mating the module's **bottom** face): fit the **female** connector, **DF40HC(4.0)-80DS-0.4V(58)** (Figure 21).

Apply the land pattern from the Hirose DF40-series datasheet without deviation. At a 0.4 mm pitch the alignment tolerance is small, and a footprint error produces defective solder joints or bridges.

The land pattern the interface board must provide for each mating face is shown in Figure 21 (bottom side) and Figure 22 (top side). **Lay out this footprint to better than 0.05 mm positional accuracy.** At the connectors' 0.4 mm pad pitch, a larger error prevents the high-density connectors from mating reliably.

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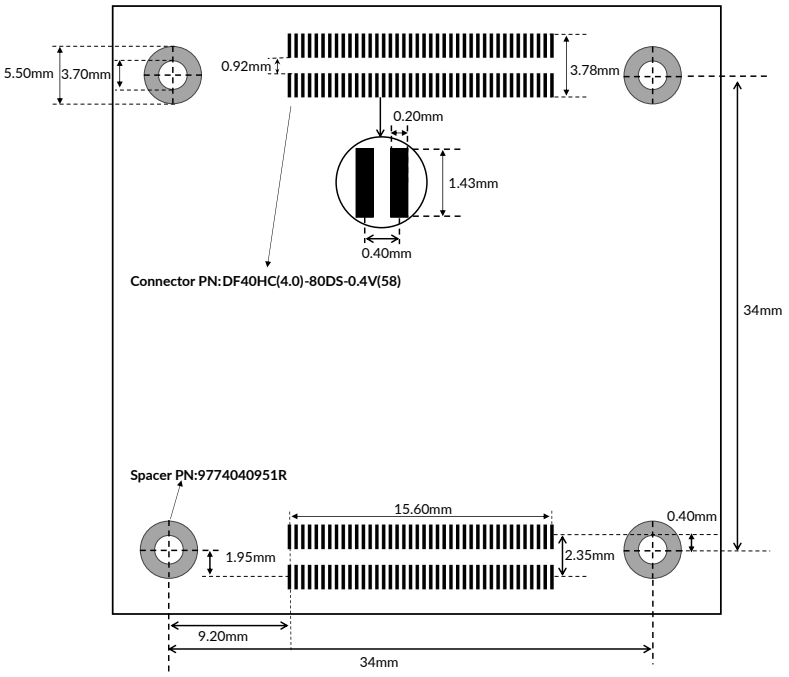

Figure 21. Bottom-side interfacing footprint: the interface-board land pattern (connector pads and mounting holes) for the bottom face of the SOLO SOM; dimensions in millimetres.

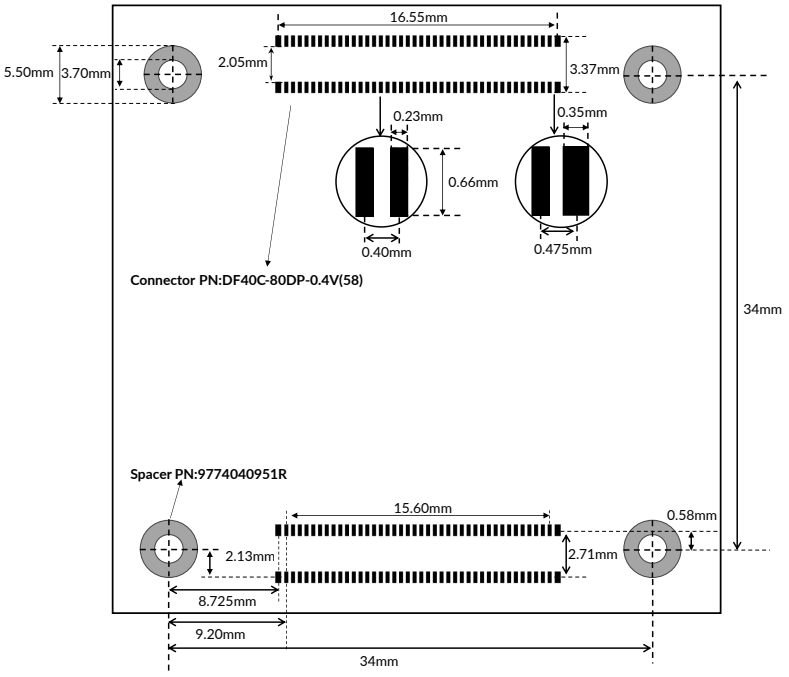

Figure 22. Top-side interfacing footprint: the interface-board land pattern (connector pads and mounting holes) for the top face of the SOLO SOM; dimensions in millimetres.

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Apply the following routing practices:

- Route the EtherCAT lines as controlled-impedance traces: 50 Ω single-ended and 100 Ω differential (see Section 10.1).
- Place a 1206 capacitor between chassis ground and circuit ground near the Ethernet magnetics.
- Provide a dedicated quiet analog ground region for the current-sense and Sin/Cos signals, separated from the switching currents of the power stage.
- Provide ESD protection on every pin routed to a user-accessible connector.
- Route feedback signals away from power signals. Routing a low-level sensor signal parallel to a switching power trace couples noise into the control loops.

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9. CONNECTOR PINOUT & SIGNAL DESCRIPTIONS

9.1 CONNECTOR ORGANIZATION

This chapter is the primary reference for interface-board wiring. The connector layout is described first, followed by the detailed pin tables.

The module routes its signals through **two** 80-pin connectors, a debug header, and a USB port:

Connector	Signal content
HD1 (80-pin)	Power and ground, single-ended incremental encoders, motor voltage feedback, current sensing, motor PWM outputs, GPIO, User Core PWM/SPI/ADC, analog outputs (AO1–AO3), Sin/Cos, PT1000 input, UART, and CAN
HD2 (80-pin)	USB data lines, differential incremental encoder, Hall sensors, both EtherCAT ports, the 0–5 V analog inputs, additional general-purpose ADC channels, the primary and secondary BiSS-C encoders with their switched 5 V supplies, and spare DSP GPIO
JTAG (12-pin)	User Core debug interface
USB-C	USB 2.0 Full-Speed, for configuration and firmware updates

HD1 carries the motor and power-stage signals together with the User Core analog and digital resources; HD2 carries the communication and position-sensing signals. Both are normally routed.

In the tables below, each pin is listed on its own row in numerical order (1 through 80), with its signal name and an individual description. On the connector itself, the odd-numbered and even-numbered pins form the two physical rows.

Figure 23 shows the complete pin assignment of both high-density connectors at a glance, alongside the USB and JTAG ports. The detailed per-pin tables follow.

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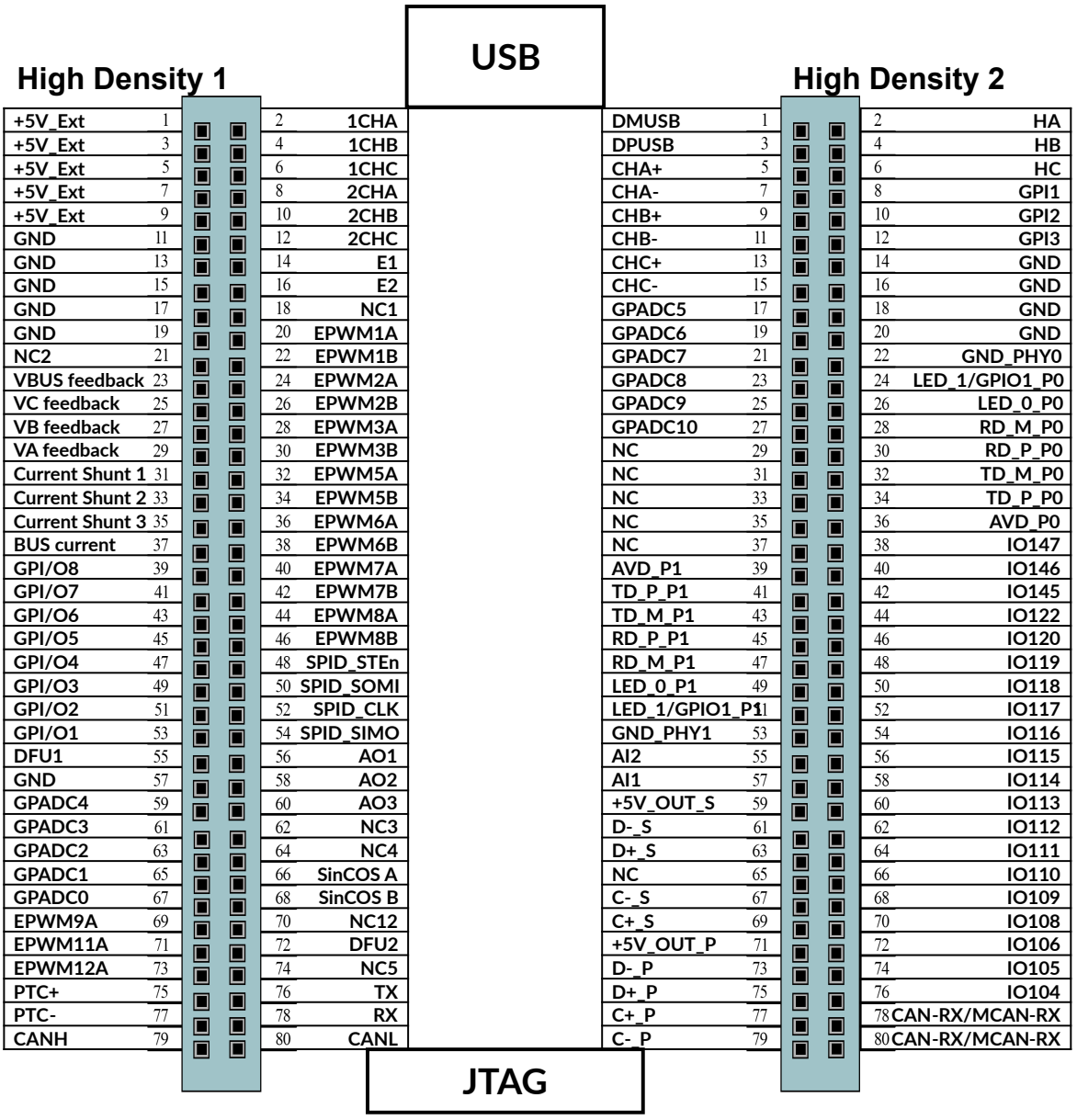

Figure 23. Pin assignment map for both high-density connectors (HD1 and HD2), with the USB and JTAG ports.

9.2 HD1 — HIGH-DENSITY CONNECTOR 1 (80-PIN)

Pin	Signal	Description
1	+5V_Ext	+5 V supply input
2	Enc 1CHA	Single-ended encoder 1, channel A
3	+5V_Ext	+5 V supply input

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Pin	Signal	Description
4	Enc 1CHB	Single-ended encoder 1, channel B
5	+5V_Ext	+5 V supply input
6	Enc 1CHC	Single-ended encoder 1, index (C)
7	+5V_Ext	+5 V supply input
8	Enc 2CHA	Single-ended encoder 2, channel A
9	+5V_Ext	+5 V supply input
10	Enc 2CHB	Single-ended encoder 2, channel B
11	GND	Ground
12	Enc 2CHC	Single-ended encoder 2, index (C)
13	GND	Ground
14	E1 (Error LED)	Error indicator output
15	GND	Ground
16	E2 (Heartbeat LED)	Heartbeat indicator output
17	GND	Ground
18	NC	Not connected
19	GND	Ground
20	EPWM1A	Phase A high-side PWM
21	NC	Not connected
22	EPWM1B	Phase A low-side PWM
23	VBUS_feedback	DC bus voltage sense (0–3.3 V)
24	EPWM2A	Phase B high-side PWM
25	VC_feedback	Motor phase C voltage (0–3.3 V)
26	EPWM2B	Phase B low-side PWM
27	VB_feedback	Motor phase B voltage (0–3.3 V)
28	EPWM3A	Phase C high-side PWM
29	VA_feedback	Motor phase A voltage (0–3.3 V)
30	EPWM3B	Phase C low-side PWM

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Pin	Signal	Description
31	Motor Current 1	Phase 1 current shunt (0–3.3 V)
32	EPWM5A	User Core PWM5 A
33	Motor Current 2	Phase 2 current shunt (0–3.3 V)
34	EPWM5B	User Core PWM5 B
35	Motor Current 3	Phase 3 current shunt (0–3.3 V)
36	EPWM6A	User Core PWM6 A
37	BUS_current	DC bus current shunt (0–3.3 V)
38	EPWM6B	User Core PWM6 B
39	GPI/O8	General-purpose I/O 8
40	EPWM7A	User Core PWM7 A
41	GPI/O7	General-purpose I/O 7
42	EPWM7B	User Core PWM7 B
43	GPI/O6	General-purpose I/O 6
44	EPWM8A	Auxiliary PWM8 A
45	GPI/O5	General-purpose I/O 5
46	EPWM8B	Auxiliary PWM8 B
47	GPI/O4	General-purpose I/O 4
48	SPID_STEn	SPI chip-select (active low)
49	GPI/O3	General-purpose I/O 3
50	SPID_SOMI	SPI master-in / slave-out
51	GPI/O2	General-purpose I/O 2
52	SPID_CLK	SPI clock (max 50 MHz)
53	GPI/O1	General-purpose I/O 1
54	SPID_SIMO	SPI master-out / slave-in
55	DFU1	Forced-boot input (active-high: hold at 3.3 V to force boot — see Section 13.4)
56	AO1	Analog output 1 (0–5 V)
57	GND	Ground

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Pin	Signal	Description
58	AO2	Analog output 2 (0–5 V)
59	GPADC4	General-purpose ADC 4 (0–3.3 V)
60	AO3	Analog output 3 (0–5 V)
61	GPADC3	General-purpose ADC 3 (0–3.3 V)
62	NC	Not connected
63	GPADC2	General-purpose ADC 2 (0–3.3 V)
64	NC	Not connected
65	GPADC1	General-purpose ADC 1 (0–3.3 V)
66	SinCOS_A	Sin/Cos encoder, Sin
67	GPADC0	General-purpose ADC 0 (0–3.3 V)
68	SinCOS_B	Sin/Cos encoder, Cos
69	EPWM9A	Auxiliary PWM9 A
70	NC	Not connected
71	EPWM11A	Auxiliary PWM11 A
72	DFU2	Reserved (forced boot uses DFU1; see Section 13.4)
73	EPWM12A	Auxiliary PWM12 A
74	NC	Not connected
75	PTC+	PT1000 sensor +
76	TX (UART)	UART transmit
77	PTC–	PT1000 sensor –
78	RX (UART)	UART receive
79	CAN_H	CAN bus high
80	CAN_L	CAN bus low

The five +5V_Ext pins and the adjacent grounds carry the module supply current. Connect all of them so the current is distributed across multiple contacts rather than a single pin. The motor voltage and current-sense signals on odd pins 23–37 all require a 0–3.3 V range, so the interface board must scale the motor voltages and shunt voltages into that range before they reach the module (see Section 6.3).

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ℹ NOTE: The current-sense and motor-voltage pins connect directly to the DSP ADC. Condition and attenuate the power-stage signals to 0–3.3 V on the interface board. Do not connect a motor terminal or a raw shunt directly to these pins.

ℹ NOTE: DFU1 (pin 55) is the forced-boot input and is **active-high**: holding it at 3.3 V before a power cycle forces the module into the bootloader, while ground or no connection has no effect. DFU2 (pin 72) is reserved. The forced-boot pin is not needed for normal operation; see Section 13.4.

9.3 HD2 — HIGH-DENSITY CONNECTOR 2 (80-PIN)

Pin	Signal	Description
1	DMUSB	USB D-
2	HA	Hall sensor A
3	DPUSB	USB D+
4	HB	Hall sensor B
5	CHA+	Differential encoder A+
6	HC	Hall sensor C
7	CHA-	Differential encoder A-
8	GPI1	General-purpose digital input 1 (max 5.2 V)
9	CHB+	Differential encoder B+
10	GPI2	General-purpose digital input 2
11	CHB-	Differential encoder B-
12	GPI3	General-purpose digital input 3
13	CHC+	Differential encoder index C+
14	GND	Ground
15	CHC-	Differential encoder index C-
16	GND	Ground
17	GPADC5	General-purpose ADC 5 (0–3.3 V)
18	GND	Ground
19	GPADC6	General-purpose ADC 6 (0–3.3 V)
20	GND	Ground

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Pin	Signal	Description
21	GPADC7	General-purpose ADC 7 (0–3.3 V)
22	GND_PHY0	EtherCAT PHY0 ground
23	GPADC8	General-purpose ADC 8 (0–3.3 V)
24	LED_1/GPIO1_P0	EtherCAT port 0 activity LED
25	GPADC9	General-purpose ADC 9 (0–3.3 V)
26	LED_0_P0	EtherCAT port 0 link LED
27	GPADC10	General-purpose ADC 10 (0–3.3 V)
28	RD_M_P0	EtherCAT port 0 receive –
29	NC	Not connected
30	RD_P_P0	EtherCAT port 0 receive +
31	NC	Not connected
32	TD_M_P0	EtherCAT port 0 transmit –
33	NC	Not connected
34	TD_P_P0	EtherCAT port 0 transmit +
35	NC	Not connected
36	AVD_P0	EtherCAT port 0 analog supply (+3.3 V)
37	NC	Not connected
38	IO147	Spare DSP GPIO147
39	AVD_P1	EtherCAT port 1 analog supply (+3.3 V)
40	IO146	Spare DSP GPIO146
41	TD_P_P1	EtherCAT port 1 transmit +
42	IO145	Spare DSP GPIO145
43	TD_M_P1	EtherCAT port 1 transmit –
44	IO122	Spare DSP GPIO122
45	RD_P_P1	EtherCAT port 1 receive +
46	IO120	Spare DSP GPIO120
47	RD_M_P1	EtherCAT port 1 receive –

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Pin	Signal	Description
48	IO119	Spare DSP GPIO119
49	LED_0_P1	EtherCAT port 1 link LED
50	IO118	Spare DSP GPIO118
51	LED_1/GPIO1_P1	EtherCAT port 1 activity LED
52	IO117	Spare DSP GPIO117
53	GND_PHY1	EtherCAT PHY1 ground
54	IO116	Spare DSP GPIO116
55	AI2	Analog input 2 (0–5 V)
56	IO115	Spare DSP GPIO115
57	AI1	Analog input 1 (0–5 V)
58	IO114	Spare DSP GPIO114
59	+5V_OUT_S	Switched 5 V for the secondary encoder
60	IO113	Spare DSP GPIO113
61	D-_S	Secondary BiSS-C data -
62	IO112	Spare DSP GPIO112
63	D+_S	Secondary BiSS-C data +
64	IO111	Spare DSP GPIO111
65	NC	Not connected
66	IO110	Spare DSP GPIO110
67	C-_S	Secondary BiSS-C clock -
68	IO109	Spare DSP GPIO109
69	C+_S	Secondary BiSS-C clock +
70	IO108	Spare DSP GPIO108
71	+5V_OUT_P	Switched 5 V for the primary encoder
72	IO106	Spare DSP GPIO106
73	D-_P	Primary BiSS-C data -
74	IO105	Spare DSP GPIO105

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Pin	Signal	Description
75	D+_P	Primary BiSS-C data +
76	IO104	Spare DSP GPIO104
77	C+_P	Primary BiSS-C clock +
78	CAN-RX	CAN receive (before the transceiver)
79	C-_P	Primary BiSS-C clock -
80	CAN-TX	CAN transmit (before the transceiver)

Even-numbered pins 38 through 60 form a block of spare DSP GPIO (IO104 through IO147). These are not used by the standard firmware and are routed out for advanced or custom builds. Leave them unconnected unless a specific function has been confirmed with SOLO.

> ⚠ **CAUTION:** GPI1 (pin 8) is rated to 5.2 V maximum. Do not exceed it. The general-purpose output GPO1 can source a maximum of 5 mA. For higher loads, use GPO1 to switch a transistor rather than driving the load directly.
>
> **i NOTE:** AVD_P0 (pin 36) and AVD_P1 (pin 39) are the 3.3 V analog supplies for the two Ethernet PHYs. Decouple each with a 100 nF ceramic capacitor placed close to the RJ45 magnetics centre-tap on the interface board (see Section 10.1).

9.4 JTAG CONNECTOR — USER CORE DEBUG (12-PIN)

This 12-pin single-row connector (SM12B-SURS-TF, JST, 1.0 mm pitch) provides a standard TI debug probe with direct access to the DSP for loading and debugging User Core code. The on-board JTAG connector is shown in Figure 24.

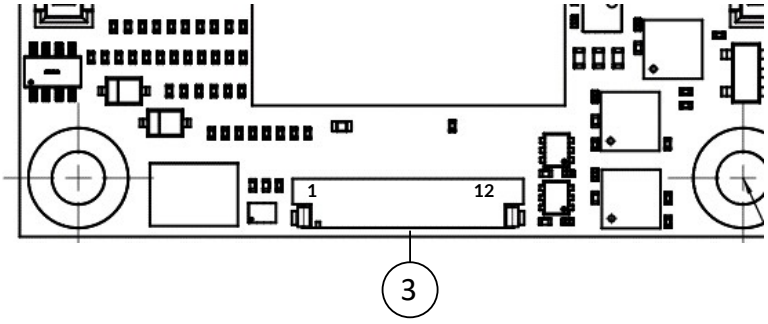

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Figure 24. On-board JTAG connector (SM12B-SURS-TF).

Pin	Signal	Dir	Description
1	+5V	—	5 V reference
2	+3.3V	—	3.3 V reference
3	TDI	Input	Test data in
4	TMS	Input	Test mode select
5	TRST	Input	Test reset (active low)
6	TDO	Output	Test data out
7	TCK	Input	Test clock
8	XRS	Input	External DSP reset
9	GPIO59	Input	DSP GPIO59
10	GPIO84	Input	DSP GPIO84
11	GND	—	Ground
12	GND	—	Ground

The five core JTAG signals (TDI, TDO, TMS, TCK, TRSTn) plus the device reset XRS come directly from the corresponding pins of the TMS320F28388D. The header is compatible with the TI XDS100V2, XDS110, and XDS200 debug probes. For users who want a ready-made solution and faster bring-up, SOLO also offers a general-purpose JTAG programmer for the SOLO SOM.

CONNECTING JTAG TO AN EXTERNAL PROBE

The JTAG port is a free, fully exposed standard IEEE 1149.1 interface, so the user can bring it out to any location and connect any compatible JTAG device. All of the signals required are present on the connector: TDI, TDO, TMS, TCK, the test reset TRST, and the device reset XRS, together with the 3.3 V and 5 V references and ground. A minimal connection needs only TDI, TDO, TMS, TCK, GND, and the 3.3 V reference; TRST and XRS are recommended for reliable reset control.

The on-module connector is a **JST SM12B-SURS-TF** (SUR series: 12-pin, single-row, 1.0 mm pitch, surface-mount, side-entry). To wire the port out, mate it with the corresponding JST SUR-series receptacle housing and crimp contacts on a cable or adapter, and route the signals to the external connector of choice. A common approach is to land these pins on a

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standard TI 14-pin or 20-pin debug header on the interface board, so that any XDS-class probe (XDS100V2, XDS110, XDS200) or the SOLO general-purpose JTAG programmer can be plugged in directly. Figure 25 shows the JTAG port wired out to an external probe.

> **ℹ NOTE:** Pins 1 (+5 V) and 2 (+3.3 V) are voltage references for the probe's level detection, not power inputs to the module. Use the 3.3 V reference to set the probe's I/O voltage. Do not back-feed the module from the probe.

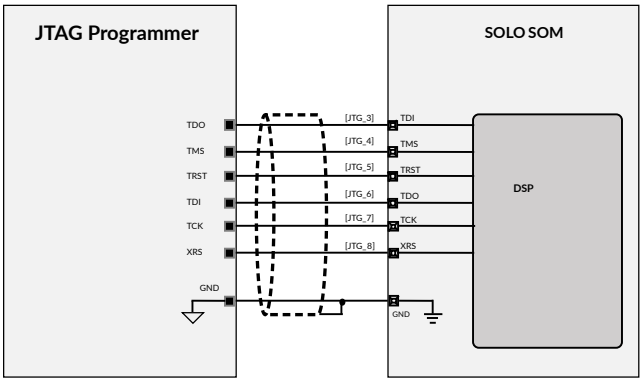

Figure 25. Wiring the JTAG port out to an external debug probe.

9.5 USB TYPE-C PORT

Parameter	Value
USB standard	USB 2.0 Full-Speed (12 Mbit/s)
Connector	USB Type-C (reversible orientation)
Modes	Virtual COM Port for the SOLO Motion Terminal; DFU for firmware updates
Maximum cable length	5 m
Power	The USB cable does not power the module; the external 5 V supply is always required

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10. NETWORKING & COMMUNICATIONS

Both EtherCAT PHYs and the CAN transceiver are integrated on the module. The interface board carries the signals to the connectors. No external transceiver circuitry is required.

10.1 ETHERCAT

EtherCAT is a high-speed industrial bus used to connect a controller (the master, typically a PLC or industrial PC) to a series of drives. Its principal characteristic is deterministic timing: every node is updated within the same cycle, which keeps multiple axes synchronized.

The module carries two **DP83822IRHBR** 100BASE-TX PHYs connected to the EtherCAT Slave Controller within the DSP. The two ports (P0 and P1) enable drives to be daisy-chained: data enters one port, passes through, and exits the other to the next node, with no external switch required.

The Ethernet signals are high-speed differential pairs and must be treated as controlled-impedance transmission lines. Otherwise the data is corrupted between the module and the connector. When routing them on the interface board:

- Route the transmit and receive pairs (TD+/TD–, RD+/RD–) as **100 Ω differential** pairs, with each trace **50 Ω single-ended** to ground.
- Do not overlap the circuit ground and chassis ground planes beneath the PHY traces. Overlap couples noise across the isolation barrier.
- Place a 1206 capacitor between chassis ground and circuit ground, close to the Ethernet magnetics, to provide a high-frequency path to chassis without a DC connection.
- Connect the magnetics centre-tap to the PHY analog supply (AVD, HD2 pins 36 and 39) and decouple it with a 100 nF capacitor at the transformer.
- Provide galvanic isolation between the EtherCAT cabling and the module by placing an isolating LAN transformer in each port's signal path. This isolation is mandatory: it protects the module from cable-borne surges and breaks ground loops between nodes operating at different ground potentials.
- **Standard RJ45 interface.** Use a discrete isolating LAN transformer such as the Würth Elektronik **7499011448** between the PHY signals and the RJ45 jack, or use an RJ45 connector with the isolation magnetics already integrated.

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- **Heavily embedded or space-constrained designs.** Where a panel RJ45 jack is not used, provide the isolation with a compact LAN magnetics module such as the Abracon **ALANL100X1-DE12DT**, routing the isolated signals directly to the board-to-board or M12 connector of choice.
- Keep each EtherCAT segment within the 100 m limit of 100BASE-TX.

WIRING DIAGRAM

Figure 26 shows how the EtherCAT PHY signals are routed from the module to the interface board, and Figure 27 shows the wiring through the isolating LAN transformer to the RJ45 connector.

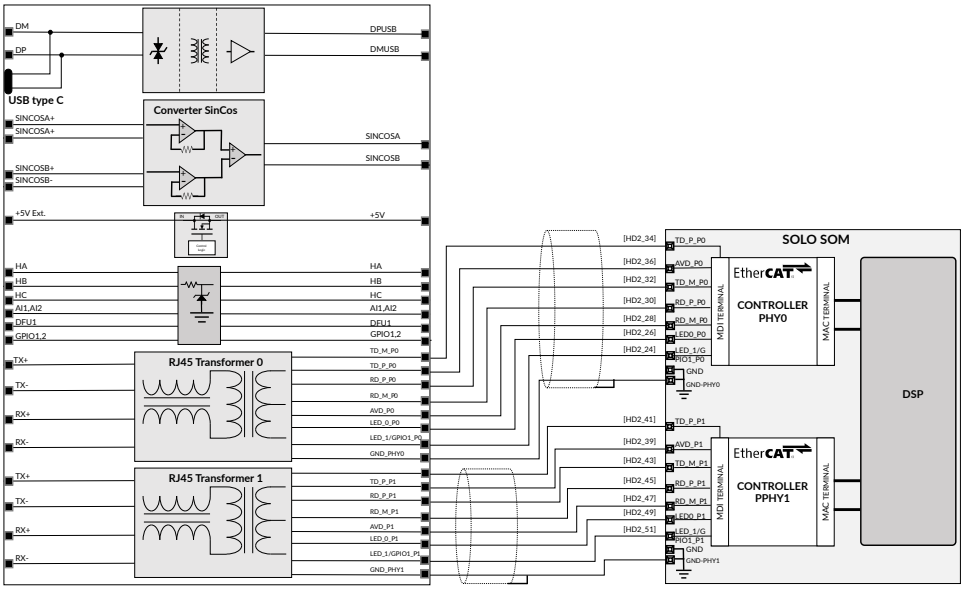

Figure 26. Routing the EtherCAT PHY signals from the module out to the interface board.

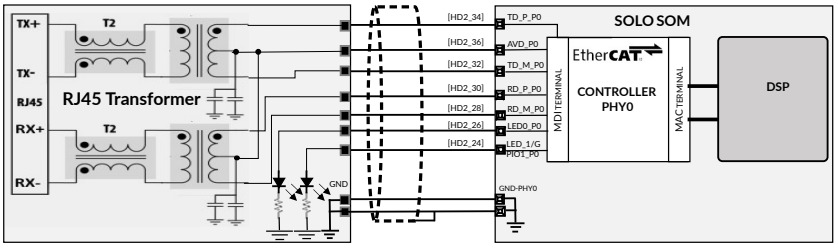

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Figure 27. EtherCAT wiring through the isolating LAN transformer to the RJ45 / network connector.

10.2 CANOPEN (DS402)

CAN is a robust, lower-speed bus common in vehicles and in simpler industrial systems. The SOLO SOM implements CANopen with the DS402 motion profile, which is the standard method for commanding a drive over CAN. The on-board **TCAN332DCNR** transceiver performs the physical signalling, so in the simplest interface board only CAN_H and CAN_L (HD1 pins 79 and 80) are routed to a connector.

In addition, the logic-level CAN signals ahead of the transceiver, **CANTX (HD2 pin 80)** and **CANRX (HD2 pin 78)**, are brought out to the connectors. Routing them out gives the designer an easy path to galvanic isolation: a digital isolator (for example the ISO1042 or a plain digital isolator feeding an external transceiver) can be inserted directly on CANTX/CANRX, isolating the CAN interface at the logic level without disturbing the module. The signals are there whenever isolation is wanted; if it is not, simply leave them unconnected and use CAN_H/CAN_L from the on-board transceiver.

Design considerations:

- The firmware uses classical CAN at up to 1 Mbit/s. The hardware is CAN FD capable, but the standard firmware stack runs classical CAN.
- A CAN bus must be terminated with a 120 Ω resistor at each of its two physical ends, and nowhere else. Fit a terminator on the interface board only if the drive is the last node on the bus.
- Set the node address and bit rate from the SOLO Motion Terminal or over the bus using CANopen LSS.
- The on-board transceiver is not isolated. Where galvanic isolation between the drive and the CAN network is required, as it commonly is when nodes sit at different ground potentials, add isolation on the interface board. The easiest route is to isolate the logic-level CANTX/CANRX lines (HD2 pins 80 and 78) with an isolated transceiver such as the ISO1042; alternatively, an isolator can be placed on the CAN_H/CAN_L bus lines.

WIRING DIAGRAM

The CAN bus wiring (CAN_H / CAN_L to the network connector) is shown in Figure 28.

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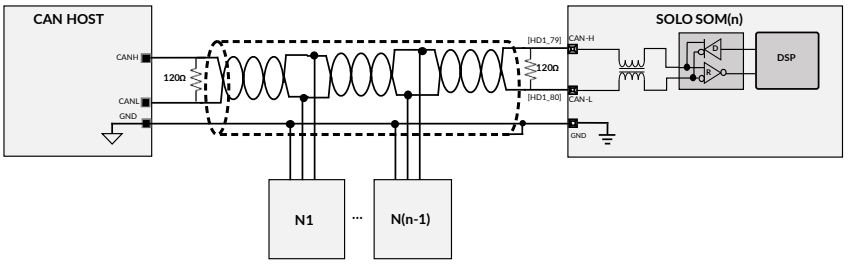

Figure 28. CAN bus wiring (CAN_H / CAN_L to the network connector).

10.3 USB

The USB Type-C port, or the same data lines on HD2 pins 1 and 3, provides the connection to a PC during configuration. The module enumerates as a virtual COM port, and the SOLO Motion Terminal uses it to configure the drive, tune the loops, and monitor live signals.

The USB data lines (USB_DM / USB_DP, HD2 pins 1 and 3) are **extendable**, so the port can be relocated from the module to a connector elsewhere on the interface board or on the enclosure. USB 2.0 signal quality falls off with distance. Where the routed length (PCB traces plus cabling) exceeds about **1.5 m**, it is recommended to fit a **USB redriver** (such as the **TUSB211AIRWBR**) close to the connector. The redriver restores the edges of the differential pair and keeps enumeration reliable over the longer run.

Because the USB lines are brought out rather than tied to the on-module connector alone, the same extendability lets the designer **galvanically isolate** the USB interface where it is needed, to break a ground loop between the PC and the drive, say, or to protect the host during bring-up of a high-voltage stage. Insert a full-speed USB isolator (such as the Analog Devices ADuM3160 / ADuM4160) in the USB_DM / USB_DP path on the interface board.

USB is intended for configuration and monitoring, not for real-time motor control. Use EtherCAT or CANopen for closed-loop control during operation.

WIRING DIAGRAM

The USB connection (USB_DM / USB_DP to the USB connector) is shown in Figure 29.

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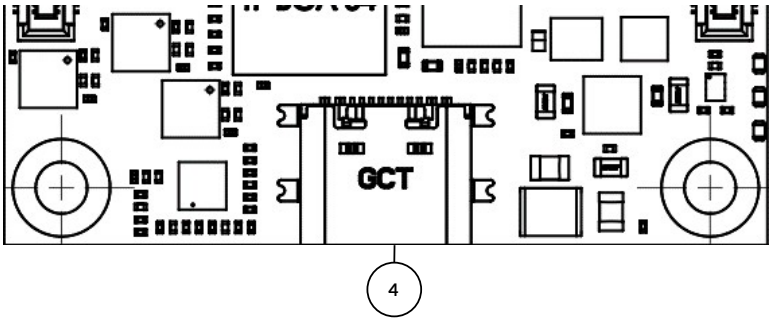

Figure 29. USB connection (USB_DM / USB_DP to the USB connector).

10.4 UART

An asynchronous serial port (UART) is available on HD1 pins 76 (TX) and 78 (RX) at 3.3 V levels. It provides a simple link to another microcontroller or to a host that does not support EtherCAT or CAN. To interface with a 5 V system or a true RS-232 port, add a level shifter or an RS-232 transceiver on the interface board.

WIRING DIAGRAM

The UART (TX / RX) wiring to an external host is shown in Figure 30.

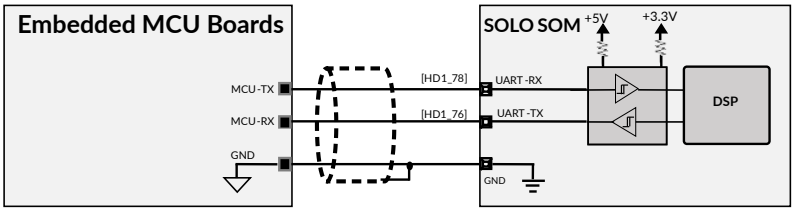

Figure 30. UART (TX / RX) wiring to an external host.

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10.5 CONNECTOR PLACEMENT

Because the module routes the PHY and transceiver signals to the connector, the physical placement of the EtherCAT, CAN, USB, and UART connectors on the interface board is determined by the designer. This permits the enclosure to be designed around the drive rather than around the module, and every module function can be controlled over these digital links.

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11. POSITION SENSING

Accurate control of motor position or speed requires knowledge of the rotor position. This information is provided by a position sensor (an encoder, or a set of Hall sensors) mounted on the motor. The SOLO SOM supports a range of sensor types so that the sensor can be matched to the required accuracy, cost, and robustness.

The module provides **two** sensing channels. The **primary** channel is used by the control loops to run the motor. The **secondary** channel is independent and is intended for monitoring: the load-side position in a safety system, for example, or a second independent position reading for cross-checking.

> ℹ **NOTE:** A position sensor is not always required. The SOLO SOM also supports **sensorless** control, including the High-Speed Observer (HSO) method for high-speed motors. See Section 3.4.3.

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11.1 PRIMARY ENCODER TYPES

11.1.1 BISS-C ABSOLUTE ENCODER (UP TO 48-BIT)

An absolute encoder reports the exact shaft angle at power-up, with no requirement to move the motor to a reference position first. BiSS-C is an open digital standard for absolute encoders. On the primary channel the SOLO SOM operates as a full BiSS-C **master**: it generates the clock, reads back the position data, and can both read from and write to the encoder's internal registers. Register write access supports operations such as configuring the encoder or clearing its error and warning flags.

Parameter	Value
Role	BiSS-C master (full protocol: read and write encoder registers)
Data width	Up to 48 bits
Clock frequency	2 MHz (minimum) to 8 MHz (maximum)
Signalling	RS-422/RS-485 differential
Encoder supply	+5V_OUT_P (HD2 pin 71); 500 mA continuous, e-fuse-protected (TPS2001EDBVR) above ≈ 2 A

The clock and data each use a differential pair (two conductors carrying opposite-polarity versions of the same signal). Differential signalling rejects noise: interference coupled into the cable affects both conductors nearly equally, and the receiver, which responds only to the difference between them, cancels it. To obtain this benefit, route each pair as a twisted pair and ground the cable shield at one end only.

The encoder connections are C+_P / C-_P (clock) on HD2 pins 77 and 79, and D+_P / D-_P (data) on pins 75 and 73. The wiring is shown in Figure 31.

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WIRING DIAGRAM

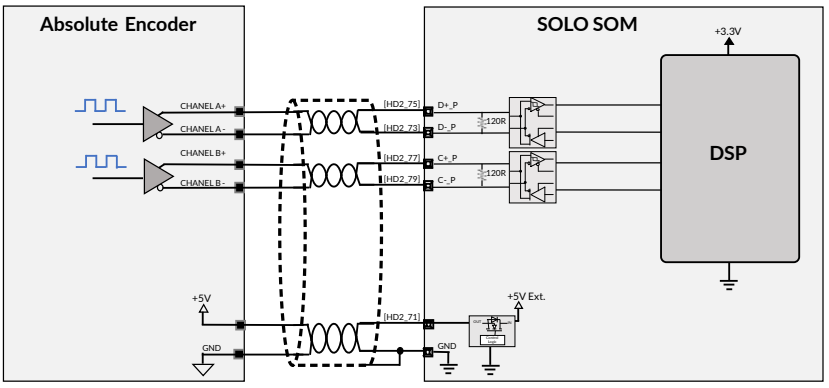

Figure 31. Primary BiSS-C absolute encoder wiring (clock and data differential pairs, switched 5 V supply).

11.1.2 SIN/COS ABSOLUTE ENCODER

A Sin/Cos encoder outputs two analog signals, a sine and a cosine, as the shaft rotates. Measuring both allows the drive to interpolate the angle finely between the coarse counts. These signals connect to HD1 pins 66 (Sin) and 68 (Cos). Because they drive the DSP analog inputs, the interface board must scale and bias them into the 0–3.3 V ADC range.

WIRING DIAGRAM

Figure 32 shows the Sin/Cos encoder wiring, with the Sin and Cos signals conditioned for the DSP analog inputs.

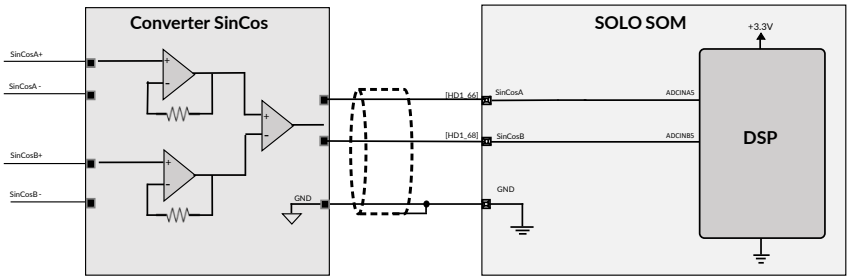

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Figure 32. Sin/Cos absolute encoder wiring (Sin / Cos analog signals conditioned for the DSP analog inputs).

The interface board must present each Sin/Cos channel to the DSP as a clean sine and cosine **centred on the 1.65 V mid-rail**, with the minimum and maximum kept inside the **0–3.3 V** ADC window (Figure 33). The waveform does not have to use the full 0–3.3 V span: any swing that stays within those rails is acceptable, even a reduced range such as 0.5 V to 2.8 V, provided it remains centred on 1.65 V. The firmware adapts to whatever amplitude is presented, so centring on 1.65 V and staying inside 0–3.3 V are the only hard requirements; because a larger amplitude gives the angle interpolation more resolution, use as much of the 0–3.3 V range as the signal chain allows for the best position accuracy.

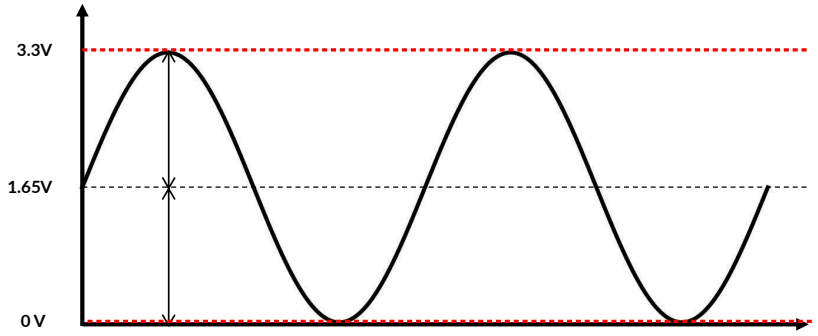

Figure 33. Sin/Cos input to the DSP: sine and cosine centred on 1.65 V with the swing kept within the 0–3.3 V ADC range. The full range need not be used (e.g. 0.5–2.8 V is acceptable) as long as the signals stay centred on 1.65 V. A larger amplitude yields finer interpolation resolution.

11.1.3 INCREMENTAL ENCODER — DIFFERENTIAL (RS-422)

An incremental encoder does not report absolute position. It emits a pulse train on two channels (A and B) as the shaft rotates, plus an index pulse (C) once per revolution. By counting the pulses and detecting which channel leads, the drive tracks the displacement and direction of the shaft. The differential version transmits each channel as an RS-422 pair, which provides noise immunity over long or electrically noisy cable runs.

The pairs connect on HD2: CHA+/– (pins 5, 7), CHB+/– (pins 9, 11), and CHC+/– (pins 13, 15). Fit a 120 Ω termination resistor across each pair on the interface board to match the cable impedance and suppress reflections.

> **i NOTE:** For a three-phase motor, the index pulse (channel C) is required. The firmware uses it during the one-time encoder calibration that aligns the encoder count with the rotor magnetic

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position. A DC brushed motor does not require the index pulse.

WIRING DIAGRAM

The differential (RS-422) incremental encoder wiring, with the CHA/CHB/CHC pairs and their 120 Ω terminations, is shown in Figure 34.

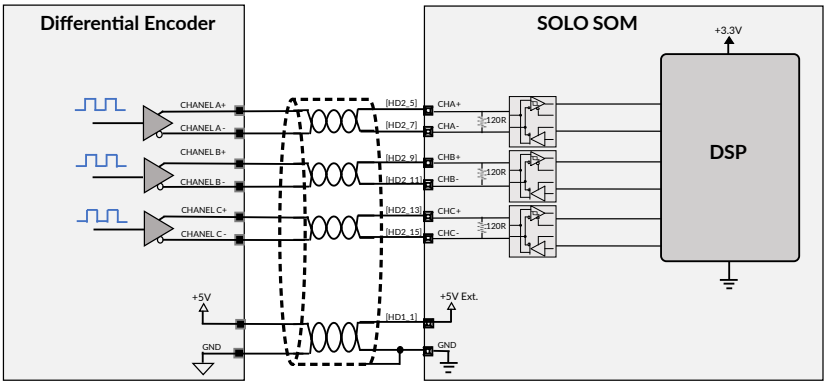

Figure 34. Differential (RS-422) incremental encoder wiring (CHA/CHB/CHC pairs with 120 Ω terminations).

11.1.4 INCREMENTAL ENCODER — SINGLE-ENDED

A single-ended incremental encoder transmits each channel on a single conductor referenced to ground, rather than as a differential pair. This is lower in cost but more susceptible to noise, and is therefore suited to short cable runs in low-noise environments. The primary single-ended channel uses 1CHA, 1CHB, and 1CHC on HD1 (pins 2, 4, 6). These inputs tolerate up to 5.2 V. A second single-ended channel set, 2CHA/2CHB/2CHC, is reserved as the secondary input and is described in Section 11.2.2.

WIRING DIAGRAM

Figure 35 shows the primary single-ended incremental encoder wiring (1CHA / 1CHB / 1CHC).

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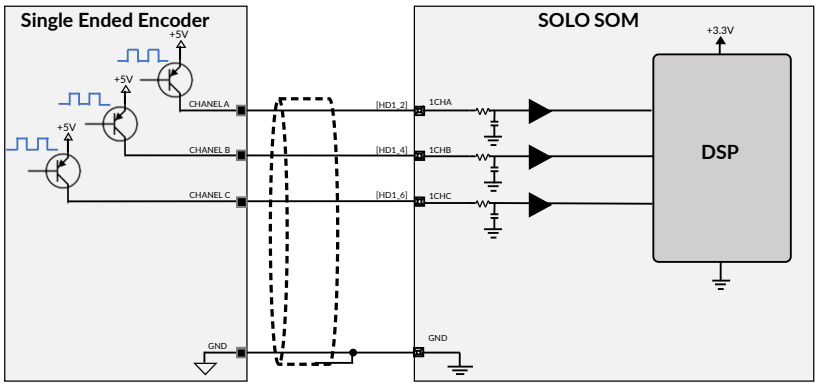

Figure 35. Single-ended incremental encoder wiring (primary channel: 1CHA / 1CHB / 1CHC).

11.1.5 DIGITAL HALL SENSORS

Hall sensors provide coarse position feedback through three digital signals (HA, HB, HC) that change state as the rotor magnets pass them. This is sufficient for six-step commutation or a coarse speed estimate. They connect on HD2 pins 2, 4, and 6 and tolerate up to 5.5 V.

> **i NOTE:** As with the encoders, Hall-based operation requires a one-time setup and calibration before running the motor. The SOLO Motion Terminal provides this procedure.

WIRING DIAGRAM

Figure 36 shows the digital Hall sensor wiring (HA / HB / HC).

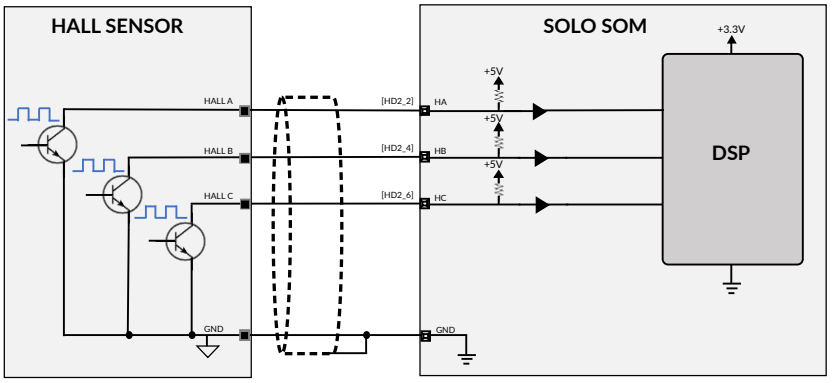

Figure 36. Digital Hall sensor wiring (HA / HB / HC).

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11.1.6 ENDAT 2.2 (BETA)

EnDAT 2.2, the Heidenhain absolute-encoder protocol, is supported in beta firmware. Where a design depends on it, confirm the current status with SOLO Motor Controllers before committing.

WIRING DIAGRAM

Wiring diagram to be added in a future revision.

11.2 SECONDARY ENCODER TYPES

11.2.1 BISS-C ABSOLUTE (READ-ONLY)

On the secondary channel the SOLO SOM still generates and drives the clock to the encoder, but it does not implement the full BiSS-C master protocol. It can only **read** the encoder's position data. It **cannot write** to the encoder's internal registers. The secondary channel is therefore a read-only absolute position input, suited to monitoring: reading a load-side or second motor-side position independently of the primary control loop, for example. As on the primary channel, the BiSS-C clock frequency ranges from 2 MHz (minimum) to 8 MHz (maximum). The connections are C+_S / C-_S (clock, pins 69, 67) and D+_S / D-_S (data, pins 63, 61) on HD2.

> **i NOTE:** Full BiSS-C master operation, including writing to the encoder registers, is available only on the primary channel (Section 11.1.1). If the application requires register writes, to configure an encoder or clear its flags, connect that encoder to the primary channel.

WIRING DIAGRAM

Figure 37 shows the secondary BiSS-C absolute encoder wiring, which uses the same differential clock and data connections as the primary channel.

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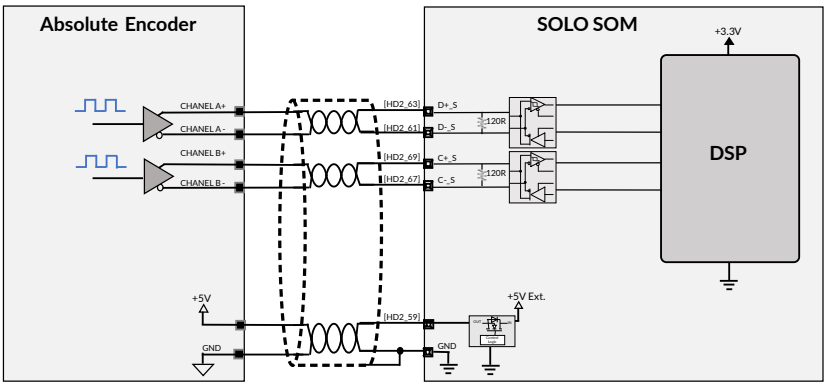

Figure 37. Secondary BiSS-C absolute encoder wiring (read-only; same differential clock/data connections as the primary channel).

11.2.2 INCREMENTAL — SINGLE-ENDED

The secondary channel provides one single-ended incremental encoder input, using 2CHA, 2CHB, and 2CHC on HD1 (pins 8, 10, 12). It is intended for monitoring: reading a load-side encoder while the primary channel reads the motor-side encoder, so that a slipped coupling or a broken belt can be detected. Only this single channel set is available on the secondary side.

WIRING DIAGRAM

Figure 38 shows the secondary single-ended incremental encoder wiring (2CHA / 2CHB / 2CHC).

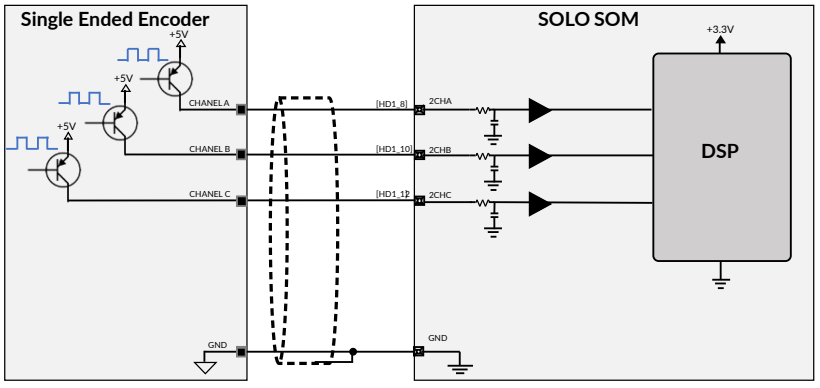

Figure 38. Secondary single-ended incremental encoder wiring (2CHA / 2CHB / 2CHC).

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11.3 PT1000 TEMPERATURE SENSOR

A PT1000 is a platinum resistance thermometer whose resistance increases predictably with temperature (1000 Ω at 0 °C). Mounting one on the motor windings or on a heatsink allows the drive to monitor for over-temperature and reduce output before damage occurs. Connect it across PTC+ (HD1 pin 75) and PTC– (HD1 pin 77).

Parameter	Value
Sensor type	PT1000 RTD (1000 Ω at 0 °C)
PTC+ pin	HD1 pin 75
PTC– pin	HD1 pin 77
Input range	0–3.3 V (+3.75 V absolute maximum)

> ⚠ **CAUTION:** The PT1000 input pins are limited to 3.3 V in normal operation. Exceeding the 3.75 V absolute maximum can permanently damage the module.

WIRING DIAGRAM

Figure 39 shows the PT1000 temperature-sensor wiring (PTC+ / PTC–), and Figure 40 shows its resistance-versus-temperature characteristic.

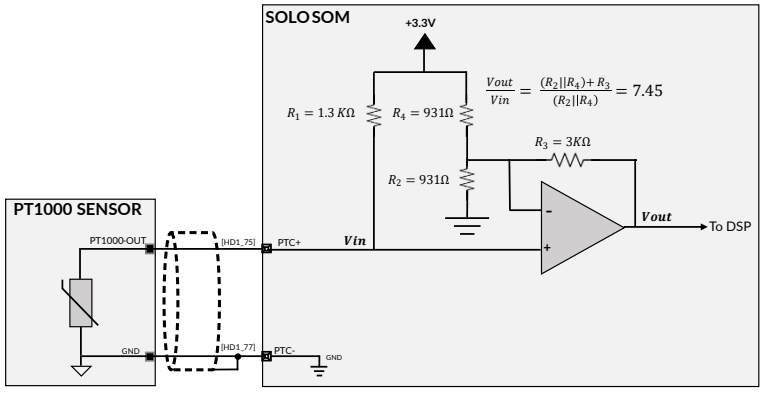

Figure 39. PT1000 temperature-sensor wiring (PTC+ / PTC–).

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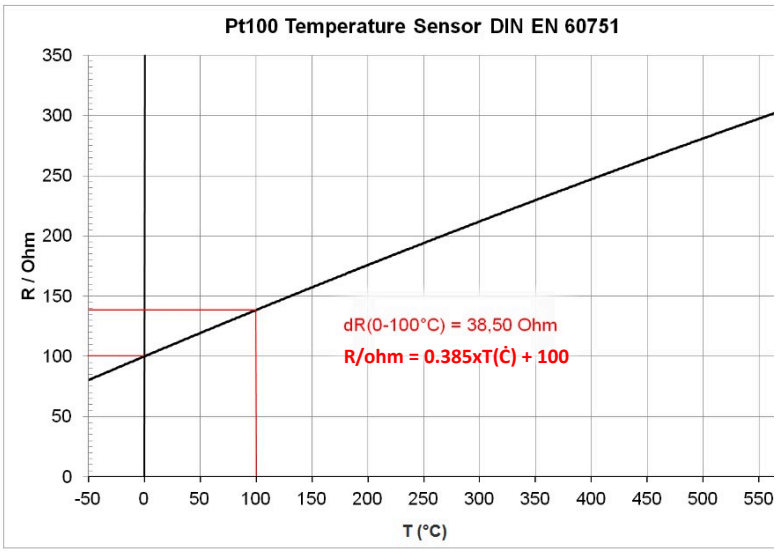

Figure 40. PT1000 resistance-versus-temperature characteristic.

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12. LED INDICATORS

The module has three LEDs that indicate its operating state:

LED	Indicates	Behaviour	Notes
A1	Power	On continuously whenever the 5 V supply is present (4.5–5 V)	Fixed on-board indicator
E2	Heartbeat	Blinks continuously once the firmware has booted successfully	Also available on HD1 pin 16
E1	Error	Blinks when a fault is active: over-voltage, over-current, or over-temperature	Also available on HD1 pin 14

In summary: A1 indicates that the board has power, E2 indicates that the firmware is running, and E1 indicates a fault. A correctly operating drive shows A1 on, E2 blinking, and E1 off.

The E1 and E2 signals are routed to HD1 (pins 14 and 16), allowing them to be mirrored to LEDs on the enclosure front panel. Drive each panel LED through a current-limiting resistor; 470 Ω provides 3 mA at 3.3 V.

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13. GETTING STARTED / INITIAL SETUP

13.1 REQUIRED EQUIPMENT

Commissioning the module for the first time requires:

1. The SOLO SOM module (SLSG0XZ011).
2. An interface board that supplies 5 V. A USB connector on the interface board is not required, because the SOLO SOM has its own USB Type-C port on the module. The interface board only needs a USB connector if the user chooses to re-route USB through it, to relocate the port to a more convenient position on the enclosure (see Section 10.3).
3. A USB Type-C cable, up to 5 m.
4. A PC running Windows 10/11 or Linux.
5. The SOLO Motion Terminal software, available from solomotorcontrollers.com.

13.2 FIRST POWER-UP

Perform these steps in order to confirm the module is operating correctly before connecting the motor power stage.

1. Verify that the 5 V supply is between 4.5 and 5.5 V before connecting it.
2. Confirm that every ground connection is secure.
3. Connect the USB cable between the module USB-C port and the PC.
4. Apply power. The **A1** LED lights immediately, confirming the supply.
5. Within approximately two seconds, the **E2** heartbeat LED begins blinking, confirming that the firmware has booted.
6. If the **E1** error LED is blinking, stop and check the supply voltage, the encoder wiring, and the motor connections before proceeding.
7. Open the SOLO Motion Terminal. The module appears automatically as a virtual COM port.

13.3 SOLO MOTION TERMINAL — INITIAL CONFIGURATION

The Motion Terminal is used to configure the drive for the connected motor and to tune it. It communicates with the module over USB, and optionally over CANopen.

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1. Download and install the software from solomotorcontrollers.com/SOLO-motion-terminal.
2. With the module powered and connected, open the software.
3. Select the module COM port from the list and click **Connect**.
4. Open **Motor Setup** and enter the motor parameters: type, pole-pair count, and rated current.

From this point, follow the online guides at solomotorcontrollers.com to learn how to tune and calibrate the motor using the Motion Terminal. The full tuning and calibration procedure is maintained online and is outside the scope of this manual.

13.4 FIRMWARE UPDATE (DFU) AND FORCED BOOT

Updating the module firmware (Device Firmware Update, DFU) is **primarily a software procedure**. The on-module bootloader starts on its own at every power-up, with no external connection and no pin asserted, so the standard update path is fully driven from the host: connect the module over USB, open the SOLO Motion Terminal, and load the new firmware image. In normal operation this software DFU is all that is needed. No jumper, button, or wiring is involved.

Forced boot is the emergency fallback. It exists for the rare case in which the resident firmware is corrupted or a fault prevents the module from booting far enough for the host to reach the software bootloader. The **DFU1** pin (HD1 pin 55) is the forced-boot input: it drives the module straight into the bootloader on the next power-up, independently of the application firmware, so a device that no longer enumerates normally can still be recovered and re-flashed.

The forced-boot input is **active-high**:

- Hold **DFU1** (HD1 pin 55) at **3.3 V**, then power-cycle the module. On the next power-up the module is forced into the bootloader. The wiring is shown in Figure 41.
- Held at ground, or left unconnected, the pin has no effect and the module boots normally.

> **i NOTE:** Mind the polarity: a high level (3.3 V) forces the boot, not a low level. DFU1 is the forced-boot pin.

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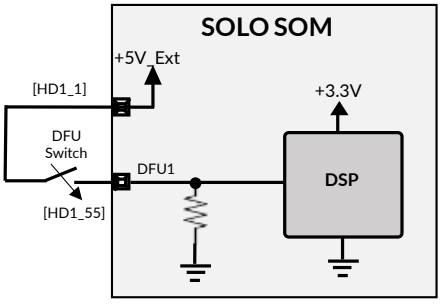

Figure 41. Forced-boot wiring: DFU1 pulled to 3.3 V to enter the bootloader on the next power-up.

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14. EVALUATION BOARDS

To make it fast and low-risk to start designing with the SOLO SOM, SOLO offers a family of **evaluation boards**. They expose the module's full capability and let you bring up a complete motor drive before committing to a custom interface board.

14.1 OPEN-SOURCE EVALUATION BOARD

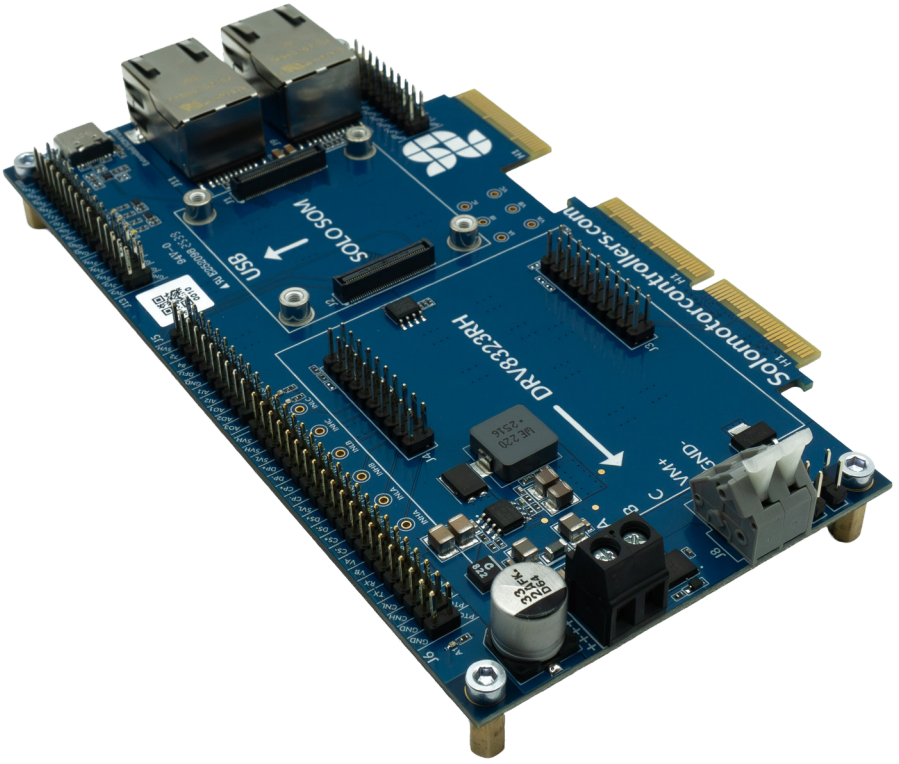

Figure 42. The SOLO SOM open-source evaluation board.

The open-source evaluation board built for the SOLO SOM (Figure 42) gives you full access to every communication interface and all digital and analog I/Os. This platform accelerates the development and testing of your next-generation motor controller, scaling easily across any power, voltage, or current level. Schematics for the SOLO SOM evaluation board, as well as all compatible evaluation boards, are fully available.

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14.2 LOW-VOLTAGE DRIVE EVALUATION

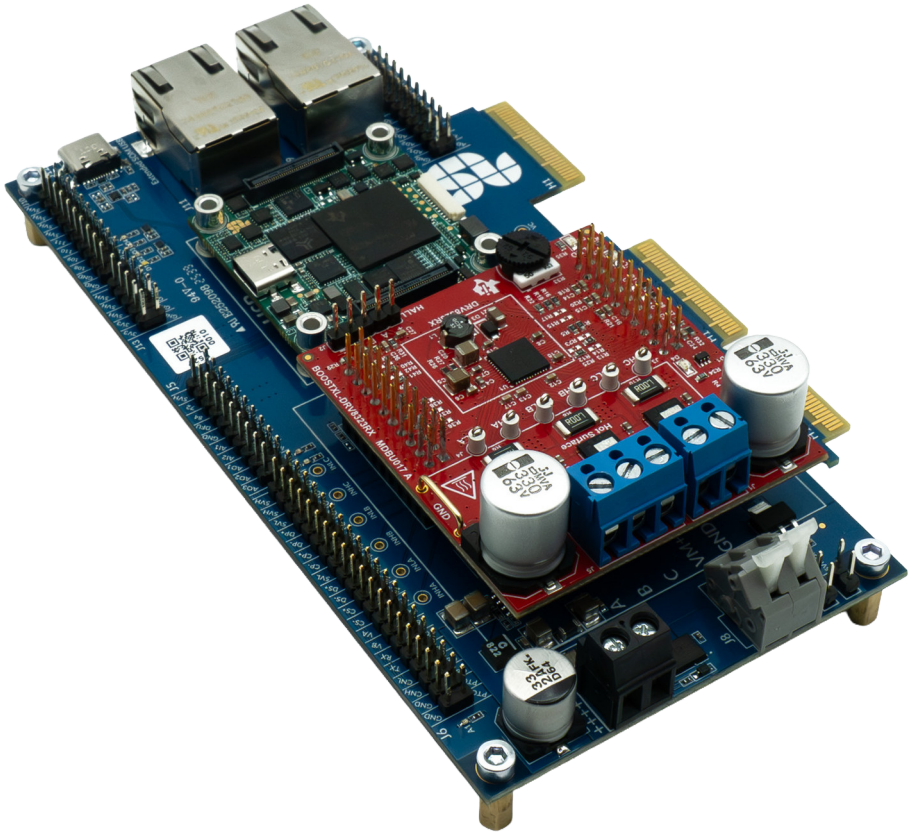

Figure 43. Evaluation board interfaced to the TI BOOSTXL-DRV8323RH for low-voltage drives.

For low-voltage work, the evaluation board provides a direct interface to the Texas Instruments **BOOSTXL-DRV8323RH** (Figure 43). That connection is a quick way to prototype a general-purpose low-voltage motor drive and control system for applications below 60 V.

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14.3 HIGH-VOLTAGE DRIVE EVALUATION

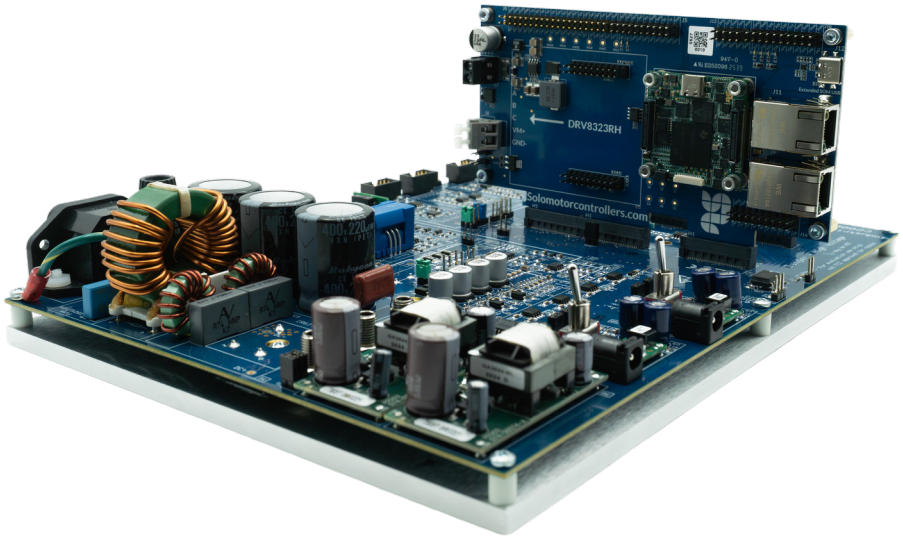

Figure 44. Evaluation board interfaced to the TMDXIDK379D 400 V inverter for high-voltage drives.

The evaluation board also enables seamless interfacing with the **TMDXIDK379D** (Figure 44), a 400 V-rated motor inverter. Leverage this capability to design your high-voltage drives around the SOLO SOM, drastically cutting down your development time.

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15. REGULATORY COMPLIANCE & APPROVALS

The compliance status below applies to the SOLO SOM module. Compliance of the complete drive depends on the interface board, the power stage, and the enclosure. System-level certification is the responsibility of the integrator.

Standard	Status
CE	Compliant
RoHS (2011/65/EU)	Compliant

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16. REVISION HISTORY

Rev	Date	Firmware	Author	Change Description
V1.0.0	31/05/2023	0x0000B00F	SOLO Motor Controllers	First release
01	2026-06-24	—	SOLO Motor Controllers	Expanded hardware manual

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