a module solution provider

WG3221-00

WLAN Dual-Band 1x1 802.11ac + Bluetooth 5.0
M.2 Type 1216, Wireless Module

Qualcomm QCA9377-3 Solution

Datasheet

Draft 0.5

Prepared By	Reviewed By	Approved By
HsinWei Wang 2019.07.19	Victor Lee 2019/07/19	2019/05/22

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1. OVERVIEW

The WG3221-00 is a wireless local area network (WLAN) and Bluetooth (BT) combination module to support 1×1 IEEE 802.11a/b/g/n/ac WLAN standards and BT5.0, enabling seamless integration of WLAN/BT and low-energy technology. This module is based on Qualcomm QCA9377-3 single-die chip.

1.1. General Features

- Supports a low-power SDIO 3.0 interface for WLAN and a UART/PCM interface for BT
- Provides a highly integrated WLAN module for 5 GHz 802.11ac, or 2.4 GHz/5 GHz 802.11n WLAN applications
- Supports BT 5.0, BLE, and ANT+ and backward compatibility with BT 1.x and BT 2.x + Enhanced Data Rate.
- Supports a single-ended RF port for cleaner and lower cost design.
- Supports 20 MHz/40 MHz at 2.4 GHz and supports 20 MHz, 40 MHz, or 80 MHz at 5 GHz
- Supports multi-user MIMO
- Supports BT-WLAN coexistence and ISM-LTE coexistence
- Operates on one 3.3-volt power supply and an I/O supply of 3.3 V or 1.8 V. Both WLAN and BT power management use advanced power-saving techniques such as:
  - Gating clocks to idle or inactive blocks
  - Voltage scaling to specific blocks in certain states
  - Fast start and settling circuits to reduce Tx
  - Active duty cycles
  - Processor frequency scaling
  - Other techniques to optimize power consumption across all operating states
- Includes additional features such as:
  - Low-density parity check (LDPC)
  - 1.5 KB of on-chip one-time programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost
  - Supports BT for class 1 and class 2 power-level transmissions without requiring an external PA
  - Available in a M.2 type 1216 package
  - Uses an internal PA and internal LNA to support the datasheet specifications.
- Dimension 16mm(L) x 12mm(W) x 2.1mm(H)
- RoHS Compliance

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram

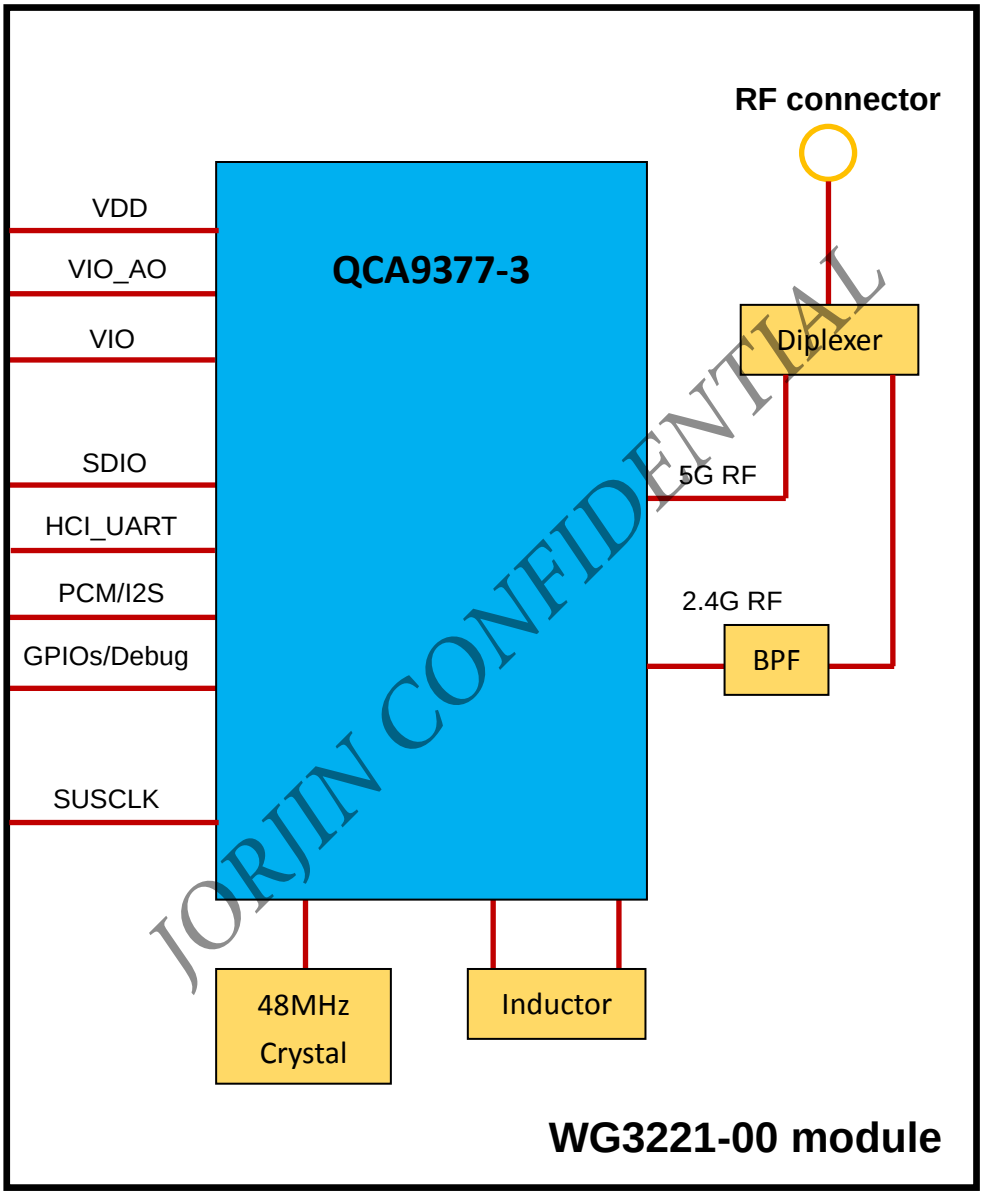


Figure 2-1. WG3221-00 Block Diagram

3. MODULE OUTLINE

3.1. Signal Layout (Top View)

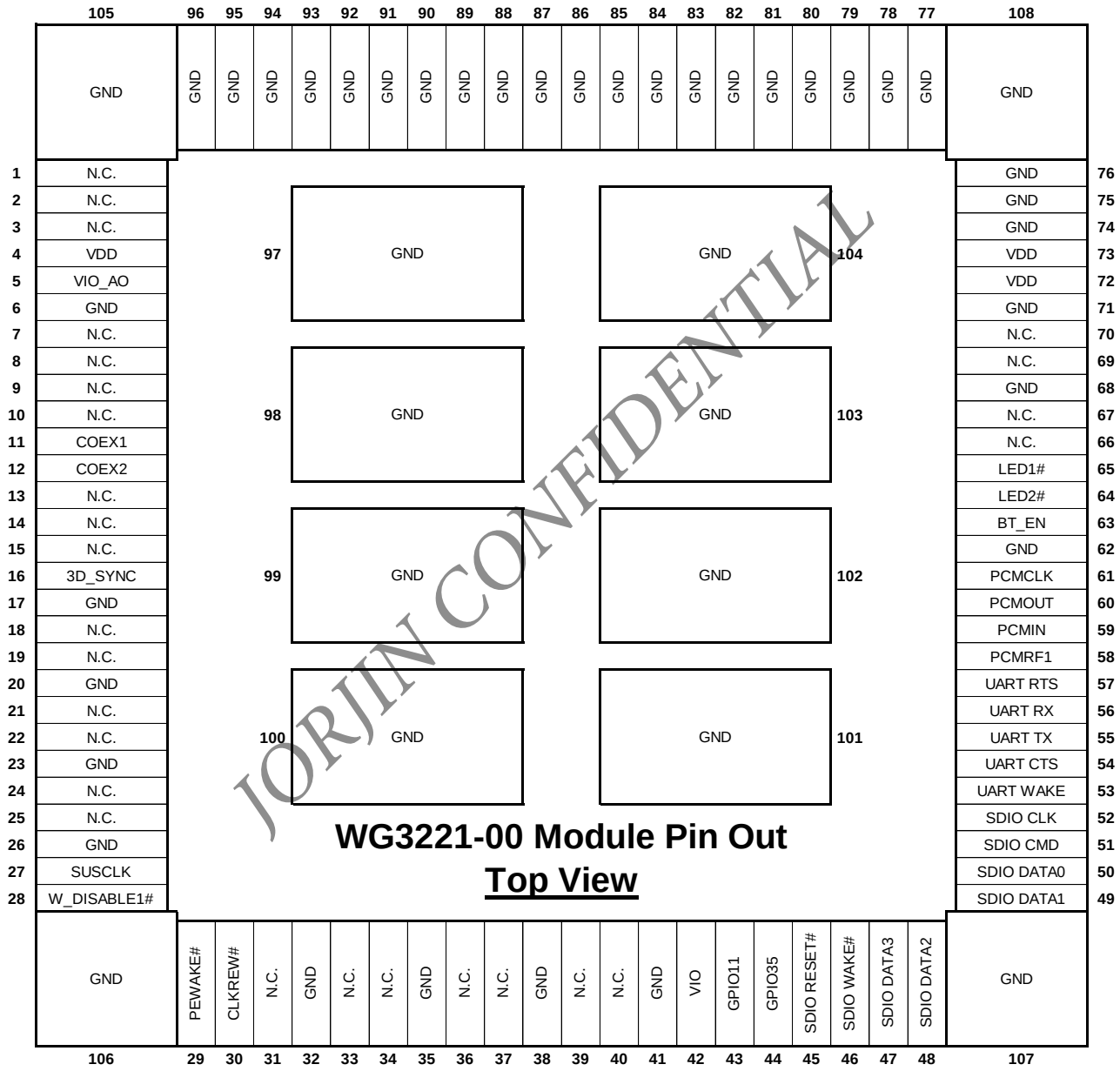


Figure 3-1. Module Pin Out (Top View)

3.2. Pin Description

Table 3-1. Pin Description

Pin No.	Pin Name	Type(1)	Description
1	NC	NC	No connection.
2	NC	NC	No connection.
3	NC	NC	No connection.
4	VDD	Power	3.3V main power supply
5	VIO_AO	Power	Always–on I/O supply for power management and real–time clock. 1.8V or 3.3V supply.
6	GND	GND	Ground
7	NC	NC	No connection.
8	NC	NC	No connection.
9	NC	NC	No connection.
10	NC	NC	No connection.
11	COEX1	PU	LTE coexistence signal. LTE_UART_RXD or LTE_FS.
12	COEX2	DO	LTE coexistence signal. LTE_UART_TXD or LTE_PRI.
13	NC	NC	No connection.
14	NC	NC	No connection.
15	NC	NC	No connection.
16	3D_SYNC	PD	Frame sync signal from TV to sync with 3D glass via Bluetooth.
17	GND	GND	Ground
18	NC	NC	No connection.
19	NC	NC	No connection.
20	GND	GND	Ground
21	NC	NC	No connection.
22	NC	NC	No connection.
23	GND	GND	Ground
24	NC	NC	No connection.
25	NC	NC	No connection.
26	GND	GND	Ground
27	SUSCLK	PD	External low–power 32.768 kHz clock input

28	W_DISABLE1#	PU	Turn off WLAN RF analog and front–end. Active low.
29	PEWAKE#	OD	PCI Express host wakeup function to wake up the host on WLAN activity. Not used, leave N.C.
30	CLKREW#	OD	PCI Express clock request signal. Not used, leave N.C.
31	NC	NC	No connection.
32	GND	GND	Ground
33	NC	NC	No connection.
34	NC	NC	No connection.
35	GND	GND	Ground
36	NC	NC	No connection.
37	NC	NC	No connection.
38	GND	GND	Ground
39	NC	NC	No connection.
40	NC	NC	No connection.
41	GND	GND	Ground
42	VIO	Power	I/O voltage supply. 1.8V or 3.3V supply.
43	GPIO11	DO	Clock request output. Not used, leave N.C.
44	GPIO35	OD	This signal can be used to enable for external Wireless charging UART circuit. Not used, leave N.C.
45	SDIO RESET#	PD	WLAN enable. Active high
46	SDIO WAKE#	DO	WLAN SDIO interrupt signal.
47	SDIO DATA3	B	WLAN SDIO data bus D3
48	SDIO DATA2	B	This pin is a boot strap signal. It must keep high for normal operation during power on reset. WLAN SDIO data bus D2
49	SDIO DATA1	B	WLAN SDIO data bus D1
50	SDIO DATA0	B	WLAN SDIO data bus D0
51	SDIO CMD	DI	WLAN SDIO CMD line signal
52	SDIO CLK	OD	WLAN SDIO clock signal.
53	UART WAKE	OD	Bluetooth wakeup host. Active high. Shared for BT LED.
54	UART CTS	DI	Bluetooth HCI UART CTS signal
55	UART TX	DO	Bluetooth HCI UART TXD signal

56	UART RX	DI	Bluetooth HCI UART RXD signal
57	UART RTS	DO	Bluetooth HCI UART RTS signal
58	PCMRF1	B	Bluetooth PCM_SYNC signal
59	PCMIN	OD	Bluetooth PCM_IN signal
60	PCMOUT	DO	Bluetooth PCM_OUT signal
61	PCMCLK	PD	Bluetooth PCM_CLK signal
62	GND	GND	Ground
63	BT_EN	PD	Bluetooth enable. Active high
64	LED2#	OD	Connected internally to pin 53 (UART WAKE)
65	LED1#	OD	Connected internally to pin 30 (CLKREW#)
66	NC	NC	No connection.
67	NC	NC	No connection.
68	GND	GND	Ground
69	NC	NC	No connection.
70	NC	NC	No connection.
71	GND	GND	Ground
72	VDD	Power	3.3V main power supply
73	VDD	Power	3.3V main power supply
74~108	GND	GND	Ground

(1) Power: Voltage supply

GND: Ground

NC: No connection

PU: Input signals with weak internal pull-up, to prevent signals from floating when left open

PD: Input signals with weak internal pull-down, to prevent signals from floating when left open

B: Bidirectional digital with CMOS input

DI: Digital input (CMOS)

DO: Digital output signal

OD: A digital output signal with open drain

4. MODULE SPECIFICATIONS

We reserve the right to amend the design and/or specifications of our products without notice.

4.1. Absolute Maximum Ratings(1)(2)

Over operating free-air temperature range (unless otherwise noted)

Table 4-1. Absolute Maximum Ratings

Parameter	Conditions	MIN	MAX	Unit
Supply voltage, VDD		-0.3	3.65	V
Supply voltage, VIO		-0.3	4.0	
3.3 V I/O VIH MAX 1.8 V I/O VIH MAX	Maximum digital I/O input voltage for 3.3V I/O supply Maximum digital I/O input voltage for 1.8V I/O supply		VIO + 0.3 VIO + 0.2	
VIH MIN	Minimum digital I/O input voltage for 3.3V or 1.8V I/O supply	-0.3		
Input RF level	Maximum RF input		+10	dBm
ESD	Electrostatic discharge tolerance	2000		V
Storage temperature range		-40	+85	°C

4.2. Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Parameter	Conditions	MIN	Typ..	MAX	Unit
Ambient temperature range		-30	-	85	°C
Operating supply voltage (VDD)	3.3V supply	3.135	3.3	3.465	V
Operating supply voltage (VIO)	1.8V or 3.3V supply	1.71 3.14	1.8 3.3	3.46	

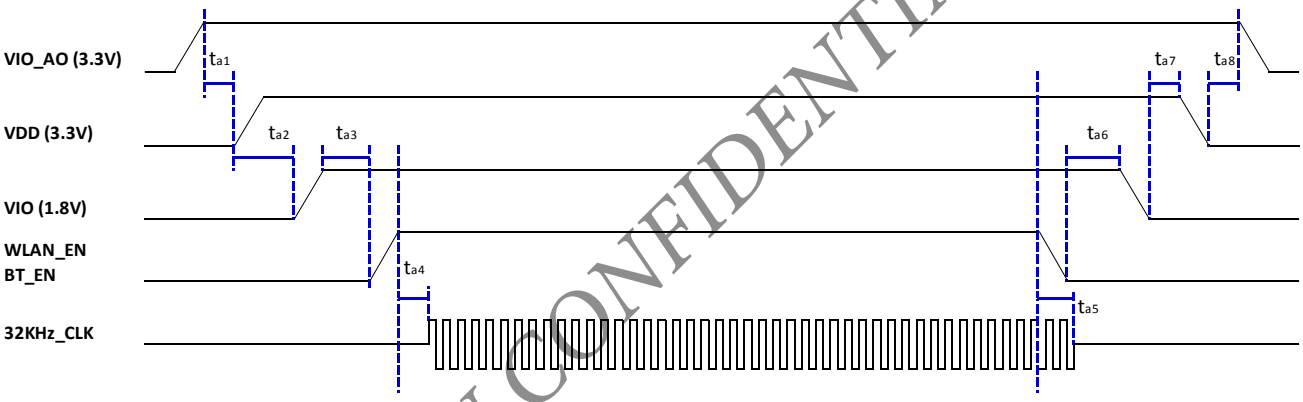
4.3. Power Sequencing:

Case-1: 3.3V power down after 1.8V

If the battery source can be removed from the end user device (battery removed, AC/DC plugged in), this is the recommended power sequence. It will avoid violating the power off sequence by allowing the 3.3 V rail to shut down after the 1.8 V rail.

Notes:

1. The module VIO voltage should match VIO voltage from the host.
2. In this case, both WLAN_EN and BT_EN of WG3221 are at 3.3 V due to using the VIO_AO power rail. If the host VIO voltage is 1.8 V, it must have level shifters to interface with host.
3. All host interface signals must stay floating or low before valid power on sequence (WLAN_EN and BT_EN goes high).



Symbol	Parameter	Min	Max	Units
t_{a1}	No requirement if VIO_AO connected to 3.3 V	0	-	μs
t_{a2}	90% of 3.3 V to 10% of 1.8 V	0	0-	
t_{a3}	90% of VIO to 0.7 V of both WLAN_EN and BT_EN	10	-	
t_{a4}	WLAN_EN valid to SUSCLK input	0	-	
t_{a5}	WLAN_EN de-assert (“low”) to SUSCLK de-assert (tristate or low)	0	-	
t_{a6}	Both WLAN_EN = low and BT_EN = low to 90% of 1.8 V	10	-	
t_{a7}	3.3 V always higher than 1.8 V during operation, with power off by removing battery or unplugging AC/DC	0		
t_{a8}	VIO_AO should be connected to 3.3 V power rail	0		

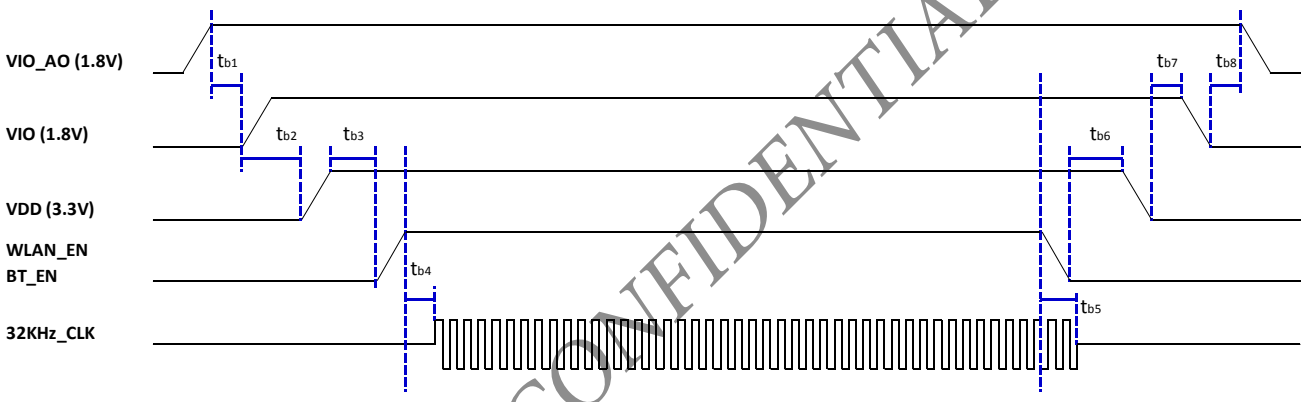
Figure 4-1. Power Sequence (3.3V power down after 1.8V)

Case-2: 1.8V power down after 3.3V

If the battery source cannot be removed from the end user device, this is the recommended power sequence for this application. This sequence allows the software to control the power on/off sequence.

Notes:

1. The module VIO voltage should match VIO voltage from the host.
2. Both WLAN_EN and BT_EN of WG3221 are 1.8 V. If host VIO voltage is 1.8 V, it does not need level shifter to interface with host.
3. All host interface signals must stay floating or low before WLAN_EN/BT_EN =high, and after WLAN_EN/BT_EN = Low.



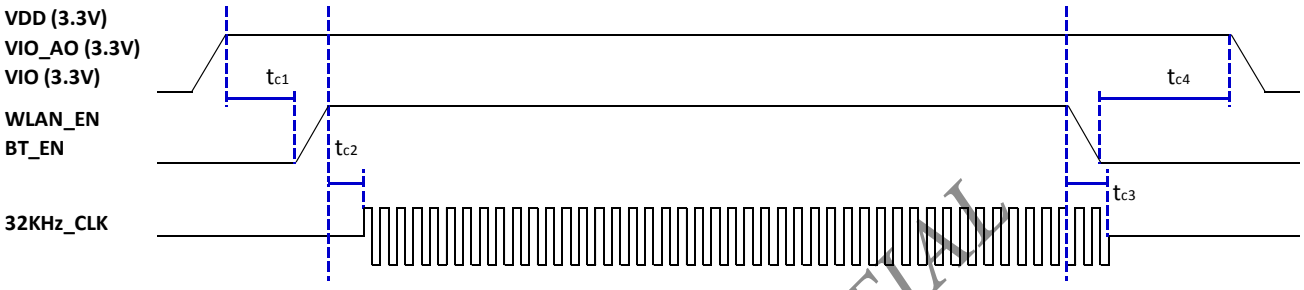
Symbol	Parameter	Min	Max	Units
t_{b1}	No requirement if VIO_AO connected to 1.8 V	0	-	µs
t_{b2}	90% of 1.8 V to 10% of 3.3 V	0	-	
t_{b3}	90% of 3.3 V to 0.7 V of both WLAN_EN and BT_EN	10	-	
t_{b4}	WLAN_EN valid to SUSCLK input	0	-	
t_{b5}	WLAN_EN de-assert (“low”) to SUSCLK de-assert (tristate or low)	0	-	
t_{b6}	Both WLAN_EN = low and BT_EN = low to 90% of 3.3 V	10	-	
t_{b7}	10% of 3.3 V to 90% of 1.8 V	0	-	
t_{b8}	VIO_AO should be connected to 1.8 V power rail	0		

Figure 4-2. Power Sequence (1.8V power down after 3.3V)

Case-3: All power rails supplied 3.3V

All power pins are connected to 3.3 V only include VDD、VIO_AO and VIO.

Notes: All host signals are either GND or floating before WLAN_EN/BT_EN =high, and after WLAN_EN/BT_EN = Low.



Symbol	Parameter	Min	Max	Units
t_{c1}	90% of 3.3 V to 0.7 V of both WLAN_EN and BT_EN	0	-	µs
t_{c2}	WLAN_EN valid to SUSCLK input	0	-	
t_{c3}	WLAN_EN de-assert (“low”) to SUSCLK de-assert (tristate or low)	0	-	
t_{c4}	Both WLAN_EN = low and BT_EN = low to 90% of 3.3 V	10	-	

Figure 4-3. Power Sequence (All power rails supplied 3.3V)

4.4. Digital Logic Characteristics

General DC electrical characteristics (for VDD=3.3V, I/O operation). Tc = 25°C

Table 4-3. Digital Logic Characteristics

Symbol	Parameter	Comments		Min	Typ.	Max	Units
VIH	High-level input voltage			0.7 x VIO	-	VIO + 0.3	V
VIL	Low-level input voltage			-0.3		0.3 x VIO	V
IIL	Input low leakage current	VIN = 0 V, Supply = VIO max		-5.0	-	5.0	µA
RPULL	Input pull resistor	Up or down	1.8V VIO 3.3V VIO	- -	120 70	- -	kΩ
VOH	High-level output voltage			0.9 x VIO	-	VIO	V
VOL	Low-level output voltage			0	-	0.1 x VIO	V
IOH	High-level output current			3	-	-	mA
IOL	Low-level output current			-	-	-11	mA
CIN	Input capacitance			-	-	3	pF

4.5. External 32.768KHz clock

The 32.768kHz clock is used in low-power modes such as IEEE power-save and sleep. It serves as a timer to determine when to wake up to receive beacons in various power-save schemes and to maintain basic logic operations when in sleep.

The WG3221 module does not require an external 32 kHz clock. By default, the module utilizes its internal 200 kHz clock shared with the WLAN and BT subsystem.

If the end application has a more accurate 32 kHz clock, then it can be supplied externally via the SUSCLK pin. The SUSCLK pin must be grounded when using the default internal clock mode. If an external 32 kHz clock is used, the requirements are:

Symbol	Parameter	Min	Typ.	Max	Units
CK1	Clock rate	-	32.768	-	KHz
CK2	Fail time	1	-	100	Ns
CK3	Rise time	1	-	100	Ns
CK4	Duty cycle (high to los ratio)	15	-	85	%
CK5	Frequency stability	-200	-	200	Ppm
CK6	Input high voltage	0.8xVIO	-	VIO+0.2	V
CK7	Input low voltage	-0.3	-		V

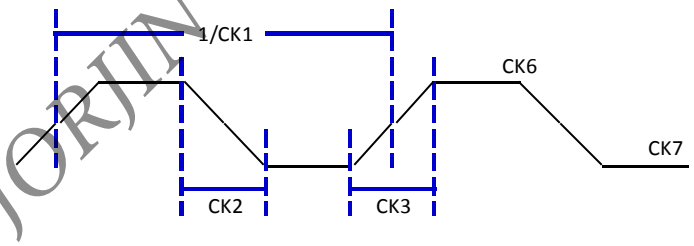


Figure 4-4. External 32.768KHz clock information

4.6. WLAN RF Characteristics

Transmit power at 2.4 GHz:

Transmit power with IEEE 802.11 EVM and spectral mask compliance at 25°C

Standard	Modulation	Data rates	MIN	Typ.	MAX	Unit
802.11b	BPSK	1 Mbps	-	18	-	dBm
	QPSK	2 Mbps	-	18	-	
	CCK	5.5 Mbps	-	18	-	
	CCK	11 Mbps	-	18	-	
802.11g	BPSK	6 Mbps	-	17	-	
	BPSK	9 Mbps	-	17	-	
	QPSK	12 Mbps	-	17	-	
	QPSK	18 Mbps	-	17	-	
	16 QAM	24 Mbps	-	17	-	
	16 QAM	36 Mbps	-	17	-	
	64 QAM	48 Mbps	-	16	-	
	64 QAM	54 Mbps	-	16	-	

Standard	Modulation	Data rates	20 MHz			40MHz			Unit
			MIN	Typ.	MAX	MIN	Typ.	MAX	
802.11n	BPSK	MCS0	-	17	-	-	16	-	dBm
	QPSK	MCS1	-	17	-	-	16	-	
	QPSK	MCS2	-	17	-	-	16	-	
	16 QAM	MCS3	-	17	-	-	16	-	
	16 QAM	MCS4	-	17	-	-	16	-	
	64 QAM	MCS5	-	16	-	-	15	-	
	64 QAM	MCS6	-	16	-	-	15	-	
	64 QAM	MCS7	-	15	-	-	14	-	

Transmit power at 5 GHz:

Transmit power with IEEE 802.11 EVM and spectral mask compliance at 25°C

Standard	Modulation	Data rates	MIN	Typ.	MAX	Unit
802.11a	BPSK	6 Mbps	-	15	-	dBm
	BPSK	9 Mbps	-	15	-	
	QPSK	12 Mbps	-	15	-	
	QPSK	18 Mbps	-	15	-	
	16 QAM	24 Mbps	-	15	-	
	16 QAM	36 Mbps	-	14	-	
	64 QAM	48 Mbps	-	13	-	
	64 QAM	54 Mbps	-	12	-	

Standard	Modulation	Data rates	20 MHz			40MHz			Unit
			MIN	Typ.	MAX	MIN	Typ.	MAX	
802.11n	BPSK	MCS0	-	15	-	-	14	-	dBm
	QPSK	MCS1	-	15	-	-	14	-	
	QPSK	MCS2	-	15	-	-	14	-	
	16 QAM	MCS3	-	14	-	-	13	-	
	16 QAM	MCS4	-	14	-	-	13	-	
	64 QAM	MCS5	-	13	-	-	12	-	
	64 QAM	MCS6	-	12	-	-	11	-	
	64 QAM	MCS7	-	11	-	-	10	-	

Standard	Modulation	Data Rates	20 MHz			40MHz			80MHz			Unit
			Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
802.11ac	BPSK	MCS0	-	15	-	-	14	-	-	13	-	dBm
	QPSK	MCS1	-	15	-	-	14	-	-	13	-	
	QPSK	MCS2	-	15	-	-	14	-	-	13	-	
	16 QAM	MCS3	-	14	-	-	13	-	-	12	-	
	16 QAM	MCS4	-	14	-	-	13	-	-	12	-	
	64 QAM	MCS5	-	13	-	-	12	-	-	11	-	
	64 QAM	MCS6	-	12	-	-	11	-	-	10	-	
	64 QAM	MCS7	-	11	-	-	10	-	-	9	-	
	256 QAM	MCS8	-	11	-	-	10	-	-	9	-	
	256 QAM	MCS9	-	-	-	-	9	-	-	8	-	

Receive minimum input level sensitivity at 2.4 GHz:

Standard	Modulation	Data rates	Typ.	Max	Unit
802.11b	BPSK	1 Mbps	-94	-	dBm
	CCK	11 Mbps	-87	-	
802.11g	BPSK	6 Mbps	-89	-	
	64 QAM	54 Mbps	-72	-	

Standard	Modulation	Data rates	20 MHz		40MHz		Unit
			Typ.	Max	Typ.	Max	
802.11n	BPSK	MCS0	-88.5	-	-86.5	-	dBm
	64 QAM	MCS7	-69	-	-67.5	-	

Receive minimum input level sensitivity at 5 GHz:

Standard	Modulation	Data rates	Typ.	Max	Unit
802.11a	BPSK	6 Mbps	-88.5	-	dBm
	64 QAM	54 Mbps	-72	-	

Standard	Modulation	Data rates	20 MHz		40MHz		Unit
			Typ.	Max	Typ.	Max	
802.11n	BPSK	MCS0	-88.5	-	-85.5	-	dBm
	64 QAM	MCS7	-69	-	-67	-	

Standard	Modulation	Data rates	20 MHz		40MHz		80MHz		Unit
			Typ.	Max	Typ.	Max	Typ.	Max	
802.11ac	BPSK	MCS0	-88	-	-85.5	-	-83	-	dBm
	256 QAM	MCS8	-65	-	-62.5	-	-60	-	
	256 QAM	MCS9	-	-	-60.5	-	-57.5	-	

4.7. BT RF Characteristics

Bluetooth and Low-Energy Transmit power:

Parameter	Min	Typ.	Max	Units
BR output power	-	10.5	-	dBm
EDR output power	-	7.5	-	
BLE output power	-	6	8.5	

Bluetooth and Low-Energy Receive sensitivity:

Parameter	Condition	Typ.	Max	Units
BT BR, EDR sensitivity Dirty TX on	BR, BER = 0.1%	-92	-	dBm
	EDR2, BER = 0.1%	-92	-	
	EDR3, BER = 0.1%	-86	-	
BLE sensitivity	1M bps, PER = 30.8%	-95	-	

4.8. Typical Power Consumption

All measurements are performed with VDD、VIO_AO and VIO=3.3V. Temperature at 25°C.

Power consumption for continuous **Rx 2.4 GHz.**

Data rates	Typ	Unit
11b, 1 Mbps	57	mA
11b, 11 Mbps	58	
11g, 6 Mbps	58	
11g, 54 Mbps	59	
MCS0, HT20	58	
MCS7, HT20	60	
MCS0, HT40	63	
MCS7, HT40	67	

Power consumption for continuous **Tx 2.4 GHz**

Data rates	Typ	Unit
11b, 1 Mbps at 18 dBm	348	mA
11b, 11 Mbps at 18 dBm	326	
11g, 6 Mbps at 17 dBm	314	
11g, 54 Mbps at 16 dBm	228	
MCS0, HT20 at 17 dBm	308	
MCS7, HT20 at 15 dBm	214	
MCS0, HT40 at 16 dBm	279	
MCS7, HT40 at 14 dBm	179	

Power consumption for continuous **Rx 5 GHz.**

Data rates	Typ	Unit
MCS0, HT20	80	mA
MCS7, HT20	82	
MCS0, VHT20	81	
MCS8, VHT20	83	
MCS0, VHT40	86	
MCS9, VHT40	90	
MCS0, VHT80	94	
MCS9, VHT80	97	

Power consumption for continuous **Tx 5 GHz**

Data rates	Typ	Unit
MCS0, HT20 at 15 dBm	388	mA
MCS7, HT20 at 11 dBm	265	
MCS0, VHT20 at 15 dBm	393	
MCS8, VHT20 at 11 dBm	258	
MCS0, VHT40 at 14 dBm	366	
MCS9, VHT40 at 9 dBm	216	
MCS0, VHT80 at 13 dBm	332	
MCS9, VHT80 at 8 dBm	193	

Power consumption for **Bluetooth**.

Mode	Typ	Unit
Continuous Rx DH5	26	mA
Continuous Tx DH5 at 10.5 dBm	59	

5. DESIGN RECOMMENDATIONS

5.1. Reference Schematic

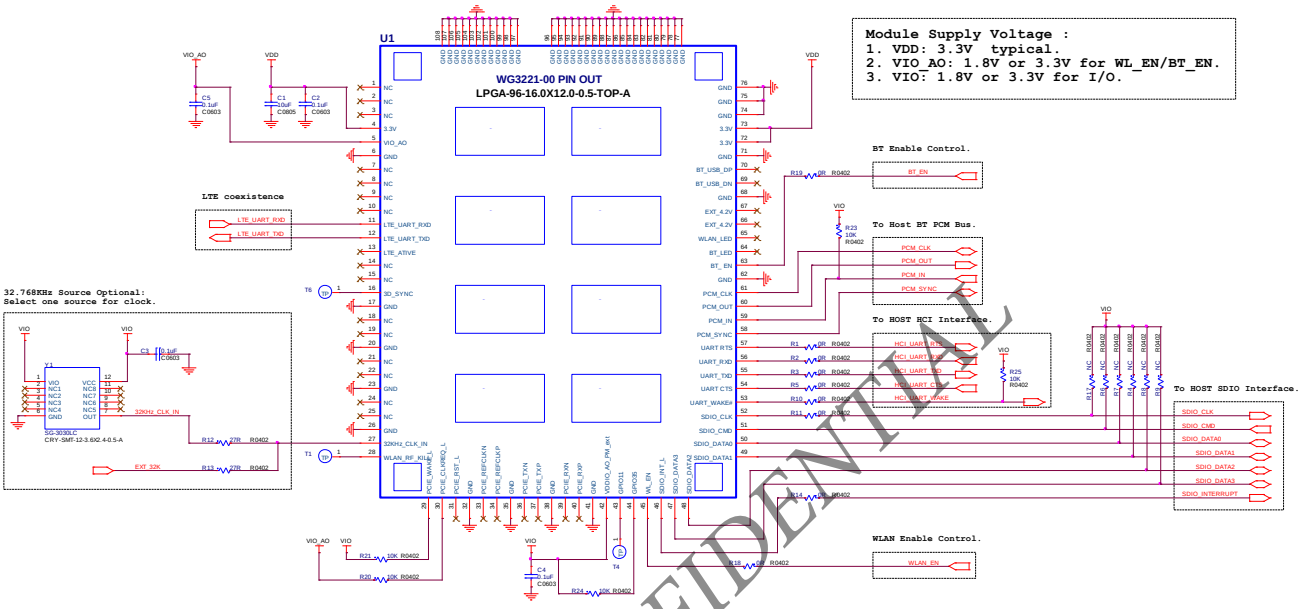
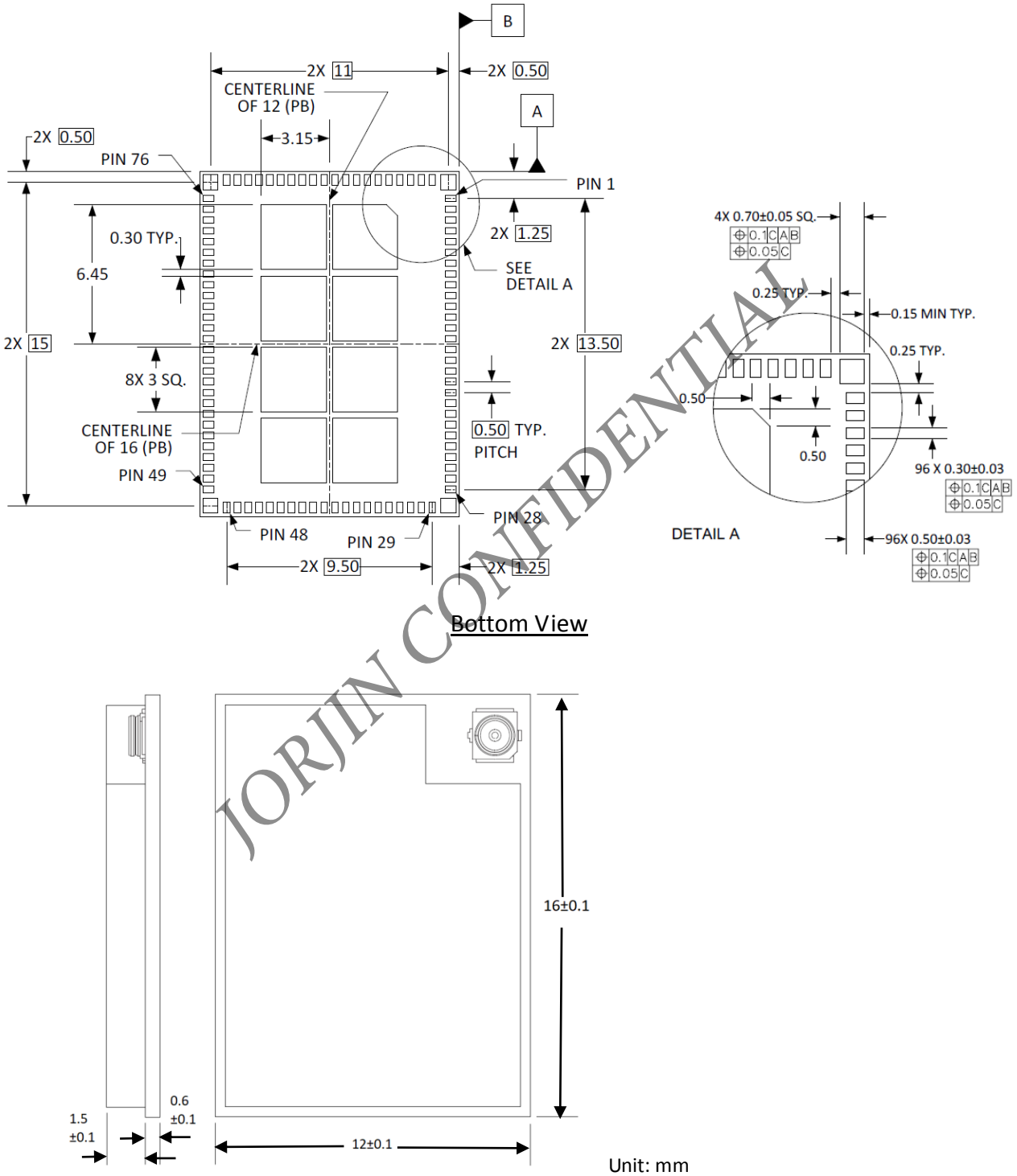


Figure 5-1. WG3221-00 module reference circuit

6. PACKAGE INFORMATION

6.1. Module Mechanical Outline



Bottom View

Top View

Figure 6-1 WG3221-00 Mechanical Outline Drawing

6.2. Recommended Land Pattern

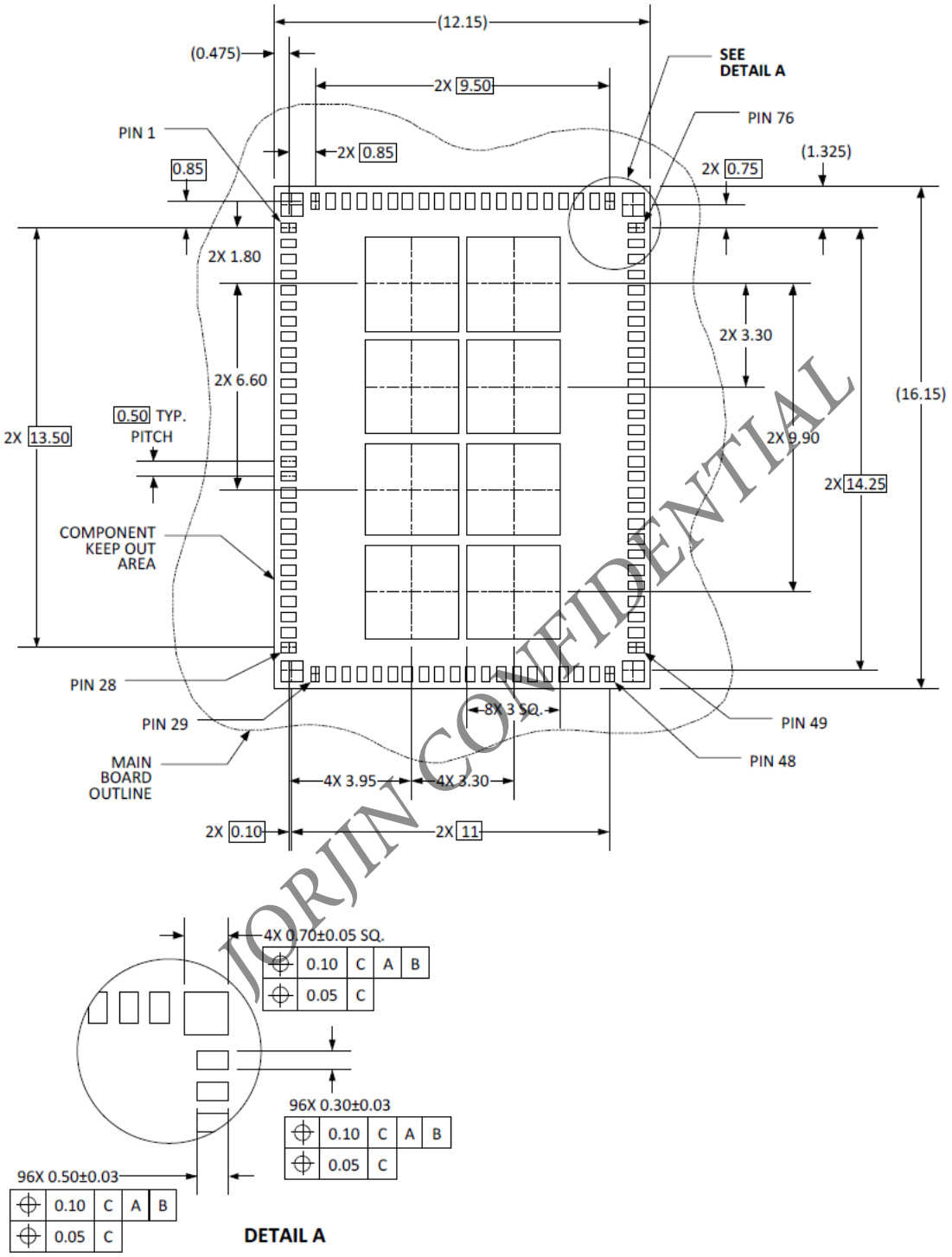
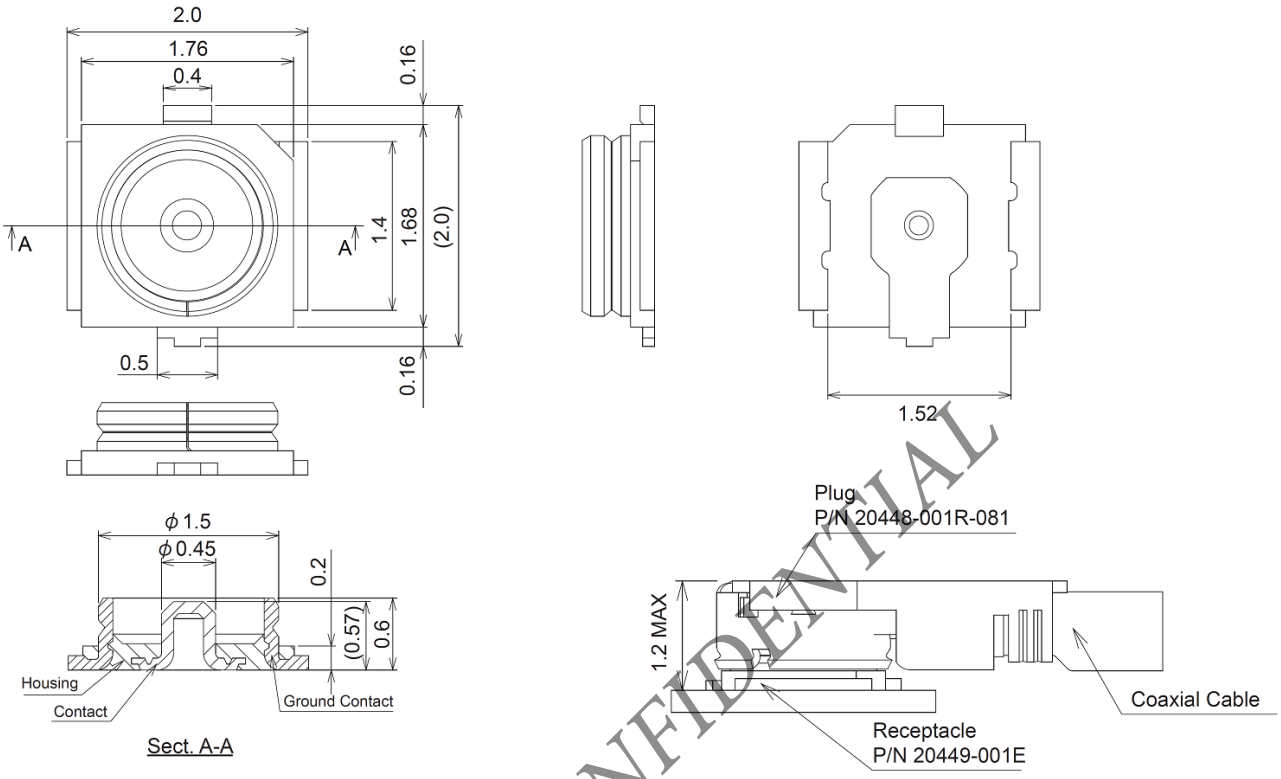


Figure 6-2 Recommended Land Pattern for Module Type 1216

6.3. RF Connector



※ P/N : 20449-001E (MHF4 series) from I-PEX

Figure 6-3 RF Connect drawing

6.4. Ordering Information

Order Number	Package
WG3221-00	M.2 type 1216

6.5. Package Marking

Marking	Description
JORJIN	Brand name
WG3221-00	Model name
YYWWSSFB	Lot Trace Code: YYWWSSFB YY = Digit of the year, ex: 2019=19 WW = Week (01~52) SS = Serial number from 01~98 match to MFG's lot number, or 99 to repair control code. F = Reverse for internal use. B = Module version.

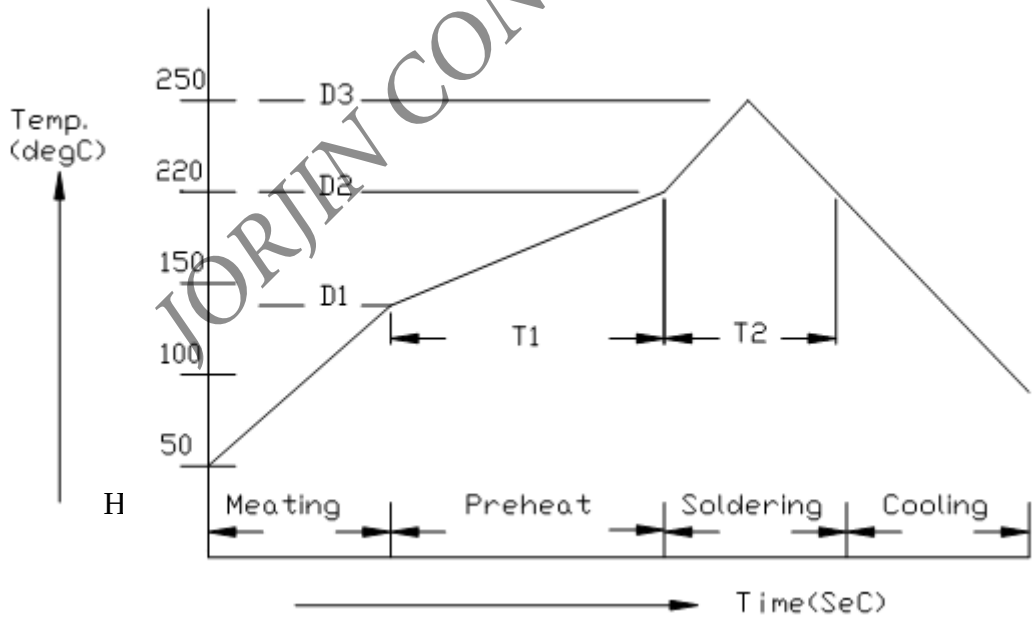
7. SMT AND BAKING RECOMMENDATION

7.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
    b) Stored at <10% RH.
  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%
  - If baking is required, Devices may be baked for 8 hrs at 125 °C.

7.2. SMT Recommendation

- Recommended Reflow profile：



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.

(2) Add Nitrogen while Reflow process：SMT solder ability will be better.

- **Stencil thickness**： 0.1~ 0.13 mm (Recommended)
- **Soldering paste (without Pb)**：Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

8. HISTORY CHANGE

Revision	Date	Description
D01	2019.01.19	Initial Released.
D02	2019.03.06	Add power consumption, RF characteristics
D03	2019.05.08	1. Update module pin out drawing in Section 3.1 2. Add power sequence in Section 4.3 3. Update RF Characteristics in Section 4.5 and 4.6. 4. Update Reference Schematic in Section 5.1. 5. Add RF connector information in Section 6.3.
D04	2019.05.22	1. Update Block Diagram in Section 2.1. 2. Update Module **Pin-5** define and description in Section 3.1 and 3.2. 3. Update power sequence in Section 4.3. 4. Add External 32.768KHz clock info in Section 4.5. 5. Update 2.4GHz RF Characteristics in Section 4.6. 6. Update Reference Schematic in Section 5.1.
D05	2019.07.19	1. Update the RF Characteristics in Section 4.5~4.7. 2. Update Power Consumption in Section 4.8.