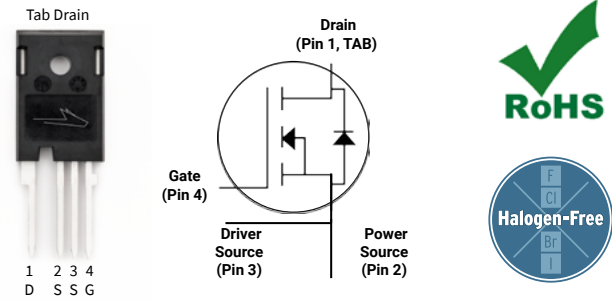


# C3M0040120K

1200V 40mohm Silicon Carbide Power MOSFET  
N-Channel Enhancement Mode

## Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant



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Part Number	Package	Marking
C3M0040120K	TO-247-4	C3M0040120K

## Applications

- Solar inverters
- EV motor drive
- High voltage DC/DC converters
- Switched mode power supplies
- Load switch

## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Maximum Ratings ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit	Test Conditions	Note
Drain-Source Voltage	$V_{DS\ max}$	1200	V	$V_{GS} = 0\ \text{V}, I_D = 100\ \mu\text{A}$	
Gate-Source Voltage (dynamic) <sup>1</sup>	$V_{GS\ max}$	-8/+19		AC ( $f > 1\ \text{Hz}$ )	Note 1
Gate - Source Voltage (static) <sup>2</sup>	$V_{GSop}$	-4/+15		Static	
Continuous Drain Current	$I_D$	66	A	$V_{GS} = 15\ \text{V}, T_c = 25^\circ\text{C}$	Fig. 19
		48		$V_{GS} = 15\ \text{V}, T_c = 100^\circ\text{C}$	Note 2
Pulsed Drain Current	$I_{DM}$	223		Pulse width $t_p$ limited by $T_{j\ max}$	Fig. 22 Note 2
Power Dissipation <sup>2</sup>	$P_D$	326	W	$T_c = 25^\circ\text{C}, T_j = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-40 to +175	°C		
Solder Temperature	$T_S$	260		According to JEDEC J-STD-020	
Mounting Torque	$M_S$	1	N-m	(M3 or 6-32 screw)	
		8.8	lbf-in		

Note:

<sup>1</sup> Recommended turn-off/turn on gate voltage  $V_{GS\ max} = -4V...0V/+15V$

<sup>2</sup> Verified by design



## Electrical Characteristics ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—		$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.7	3.6	V	$V_{DS} = V_{GS}, I_D = 9.2\ \text{mA}, T_J = 25^\circ\text{C}$	Fig. 11
Gate Threshold Voltage		—	2.2	—		$V_{DS} = V_{GS}, I_D = 9.2\ \text{mA}, T_J = 175^\circ\text{C}$	Fig. 11
Zero Gate Voltage Drain Current	$I_{DSS}$	—	1	50	$\mu\text{A}$	$V_{DS} = 1200\ \text{V}, V_{GS} = 0\ \text{V}$	
Gate-Source Leakage Current	$I_{GSS}$	—	10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	40	53.5	m $\Omega$	$V_{GS} = 15\ \text{V}, I_D = 33.3\ \text{A}$	Fig. 4, 5, 6
		—	68	—		$V_{GS} = 15\ \text{V}, I_D = 33.3\ \text{A}, T_J = 175^\circ\text{C}$	
Transconductance	$g_{fs}$	—	21	—	S	$V_{DS} = 20\ \text{V}, I_{DS} = 33.3\ \text{A}$	Fig. 7
		—	20	—		$V_{DS} = 20\ \text{V}, I_{DS} = 33.3\ \text{A}, T_J = 175^\circ\text{C}$	
Input Capacitance	$C_{iss}$	—	2900	—	pF	$V_{GS} = 0\ \text{V}, V_{DS} = 1000\ \text{V}$ $f = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
Output Capacitance	$C_{oss}$	—	103	—			
Reverse Transfer Capacitance	$C_{riss}$	—	5	—			
$C_{oss}$ Stored Energy	$E_{oss}$	—	60	—	$\mu\text{J}$		Fig. 16
Turn-On Switching Energy (SiC Diode FWD)	$E_{on}$	—	243	—	$\mu\text{J}$	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V},$ $I_D = 33.3\ \text{A}, R_{G(ext)} = 2.5\ \Omega,$ $L = 99\ \mu\text{H}, T_J = 175^\circ\text{C}$	Fig. 26
Turn Off Switching Energy (SiC Diode FWD)	$E_{off}$	—	104	—			
Turn-On Switching Energy (Body Diode FWD)	$E_{on}$	—	611	—			
Turn-Off Switching Energy (Body Diode FWD)	$E_{off}$	—	99	—			
Turn-On Delay Time	$t_{d(on)}$	—	13	—	ns	$V_{DD} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 33.3\ \text{A}, R_{G(ext)} = 2.5\ \Omega,$ $L = 99\ \mu\text{H}$ Timing relative to $V_{DS}$ Inductive load	Fig. 27
Rise Time	$t_r$	—	17	—			
Turn-Off Delay Time	$t_{d(off)}$	—	23	—			
Fall Time	$t_f$	—	9	—			
Internal Gate Resistance	$R_{G(int)}$	—	3.5	—	$\Omega$	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Effective Output Capacitance (Energy Related)	$C_{O(er)}$	—	127	—	pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0 \dots 800\ \text{V}$	Note 3
Effective Output Capacitance (Time Related)	$C_{O(tr)}$	—	197	—			
Gate to Source Charge	$Q_{GS}$	—	34	—	nC	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 33.3\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	$Q_{gd}$	—	28	—			
Total Gate Charge	$Q_g$	—	99	—			

### Note:

<sup>3</sup>  $C_{O(er)}$ , a lumped capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V

$C_{O(tr)}$ , a lumped capacitance that gives the same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V



### Reverse Diode Characteristics ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	$V_{SD}$	5.5	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.9	—		$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	$I_S$	—	51	A	$V_{GS} = -4\text{ V}, T_J = 25^\circ\text{C}$	
Diode Pulse Current	$I_{SM}$	—	223		$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{Jmax}$	
Reverse Recovery Time	$t_{rr}$	17	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.3\text{ A}, V_R = 800\text{ V}$ $T_J = 175^\circ\text{C}, di_p/dt = 7725\text{ A}/\mu\text{s}$ , $T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	850	—	nC		
Peak Reverse Recovery Current	$I_{RRM}$	79	—	A		
Reverse Recovery Time	$t_{rr}$	33	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.3\text{ A}, V_R = 800\text{ V}$ $T_J = 175^\circ\text{C}, di_p/dt = 2325\text{ A}/\mu\text{s}$ , $T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	691	—	nC		
Peak Reverse Recovery Current	$I_{RRM}$	30	—	A		

### Thermal Characteristics

Parameter	Symbol	Typ	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.46	$^\circ\text{C}/\text{W}$	Fig. 21



Typical Performance

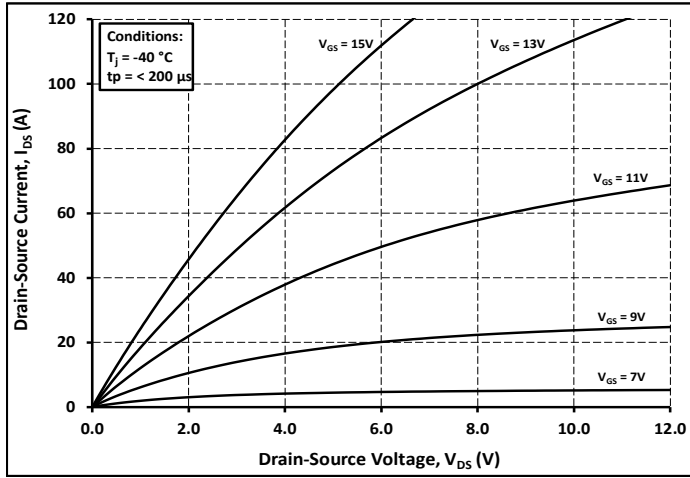


Figure 1. Output Characteristics  $T_j = -40^\circ\text{C}$

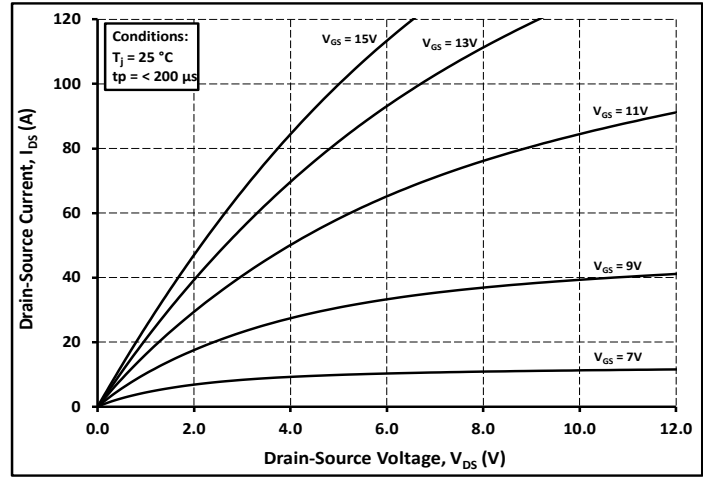


Figure 2. Output Characteristics  $T_j = 25^\circ\text{C}$

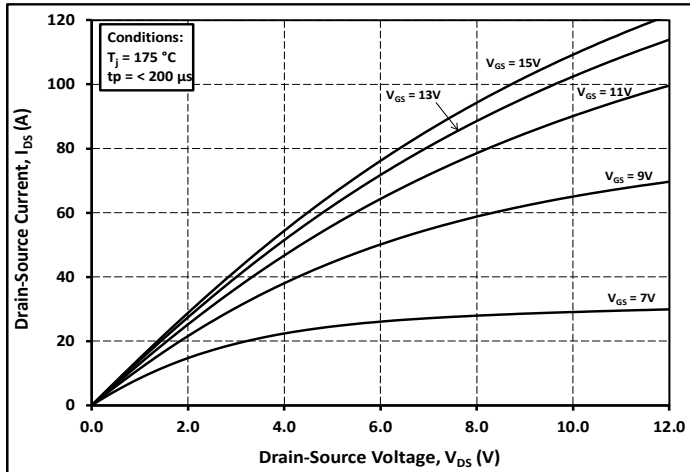


Figure 3. Output Characteristics  $T_j = 175^\circ\text{C}$

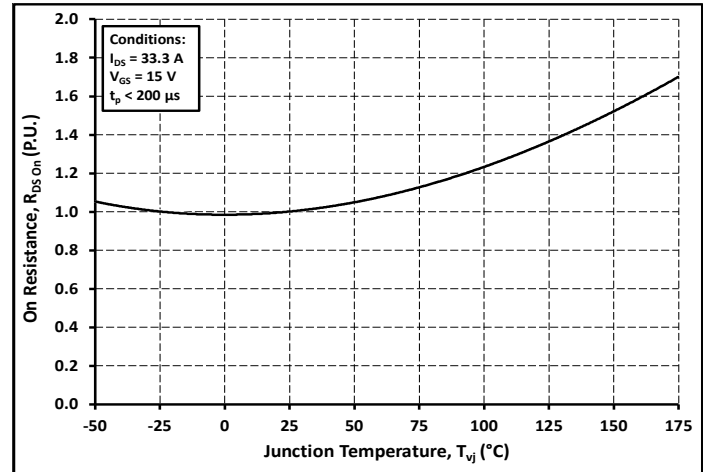


Figure 4. Normalized On-Resistance vs. Temperature

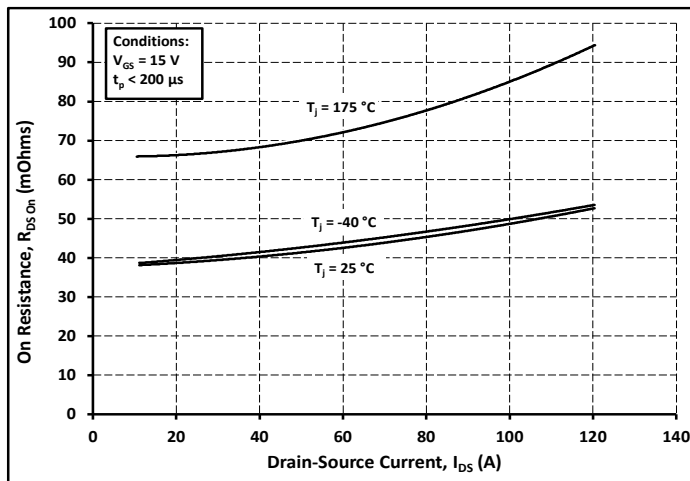


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

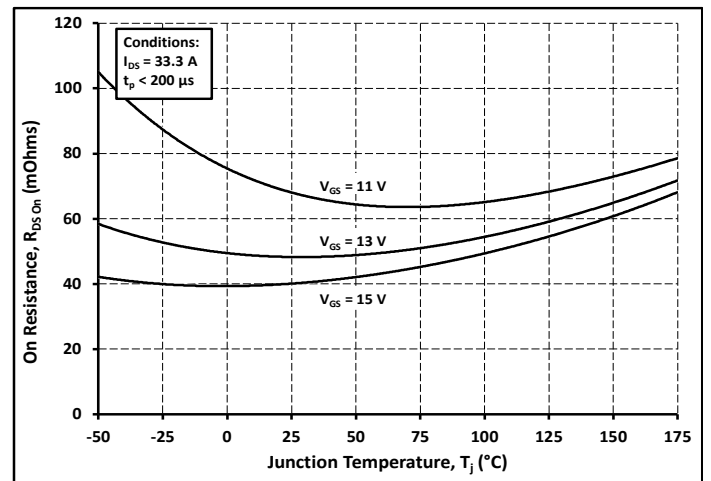


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

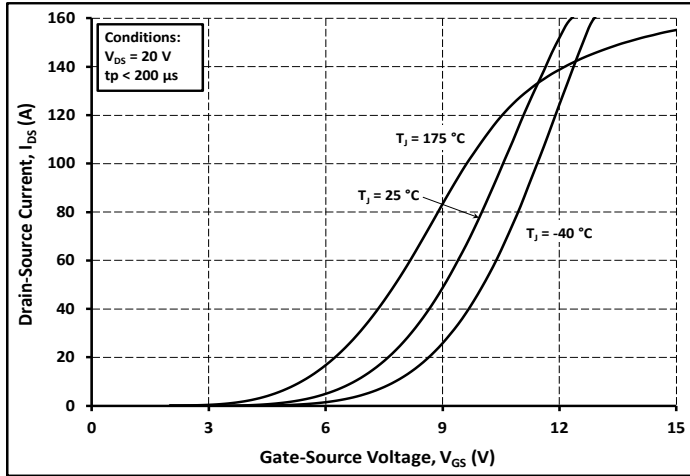


Figure 7. Transfer Characteristic for Various Junction Temperatures

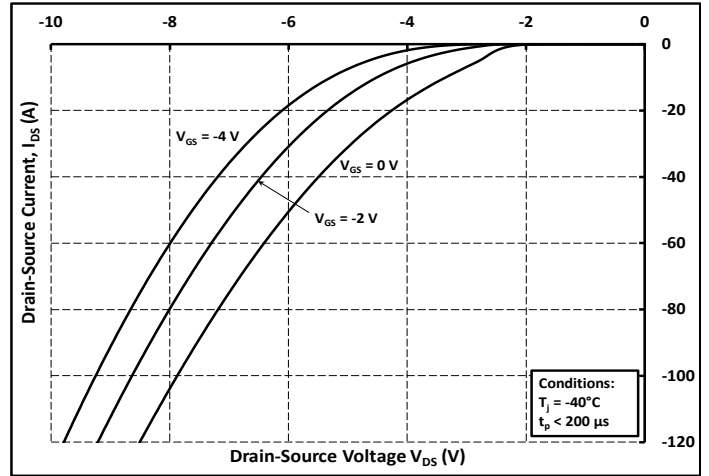


Figure 8. Body Diode Characteristic at -40°C

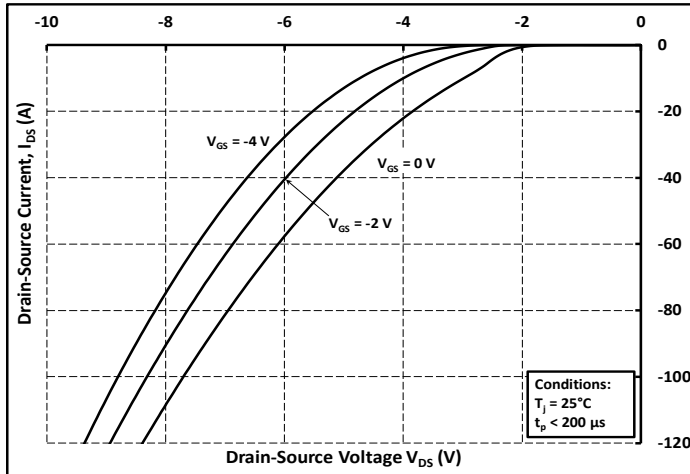


Figure 9. Body Diode Characteristic at 25°C

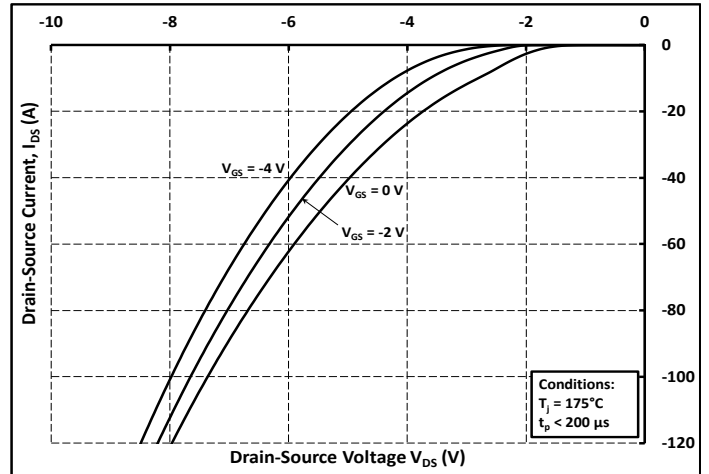


Figure 10. Body Diode Characteristic at 175°C

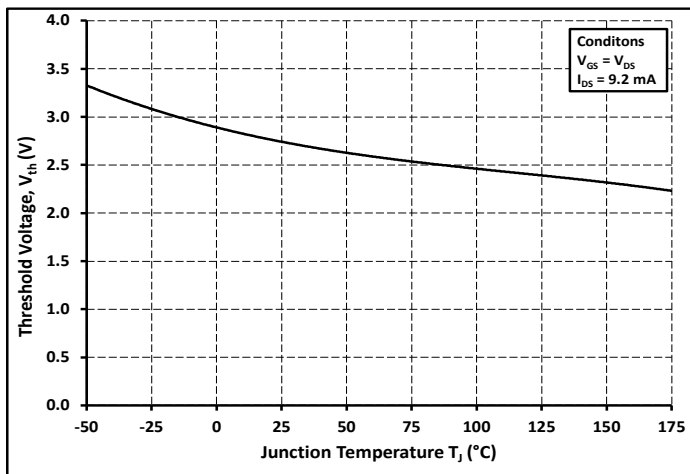


Figure 11. Threshold Voltage vs. Temperature

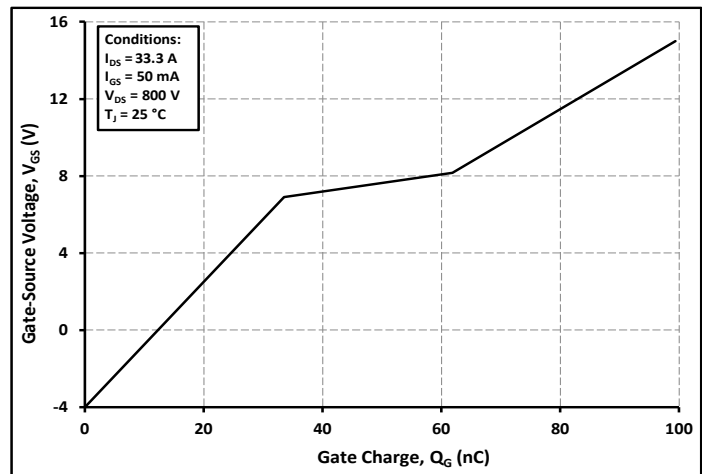


Figure 12. Gate Charge Characteristics



Typical Performance

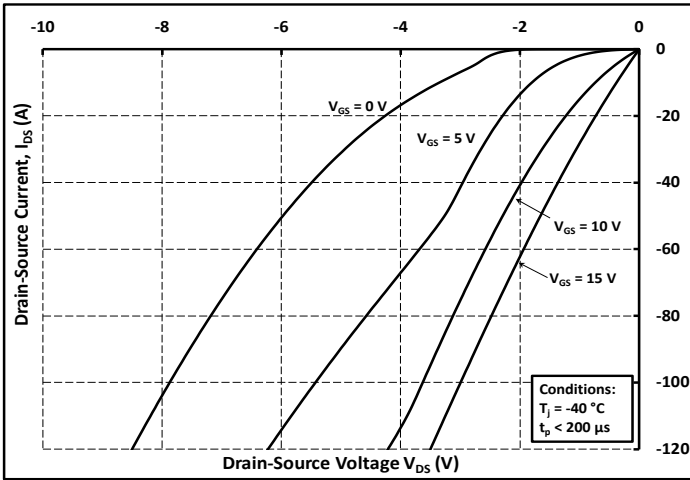


Figure 13. 3rd Quadrant Characteristic at  $-40^\circ\text{C}$

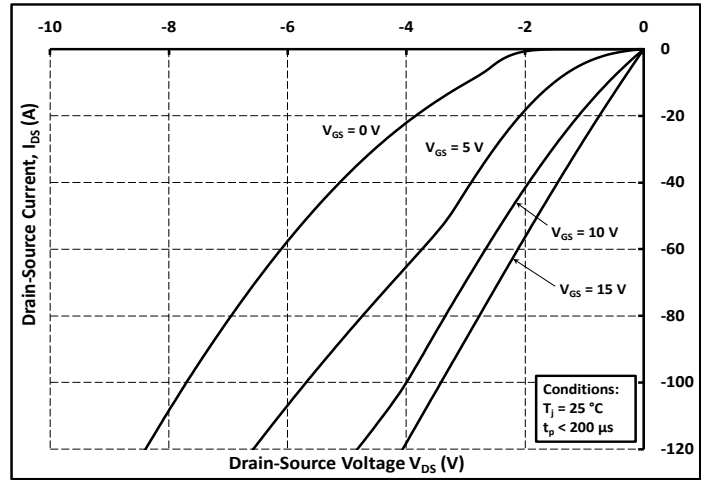


Figure 14. 3rd Quadrant Characteristic at  $25^\circ\text{C}$

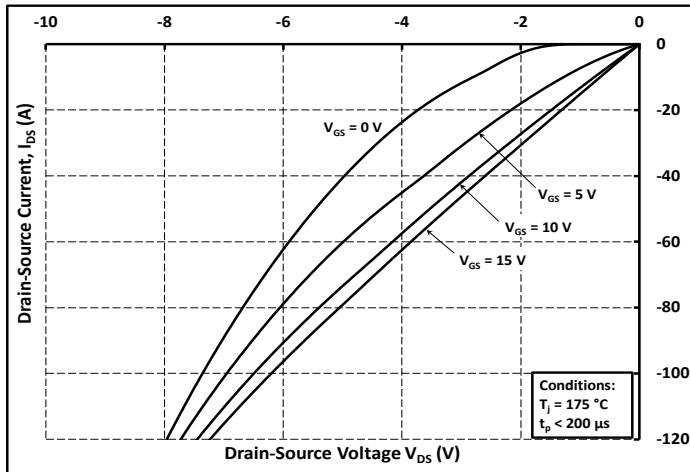


Figure 15. 3rd Quadrant Characteristic at  $175^\circ\text{C}$

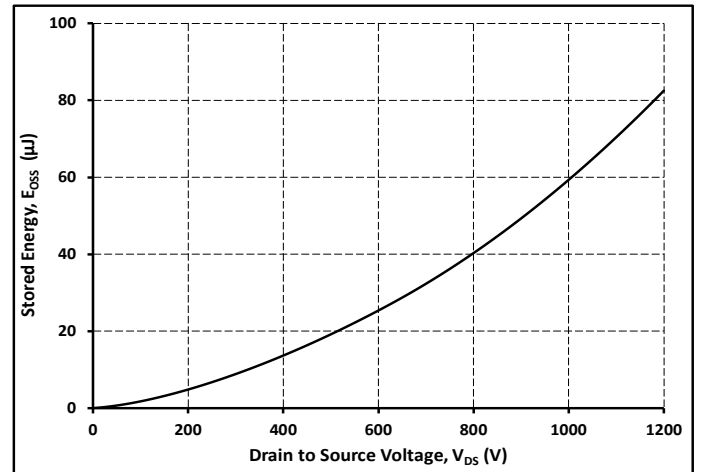


Figure 16. Output Capacitor Stored Energy

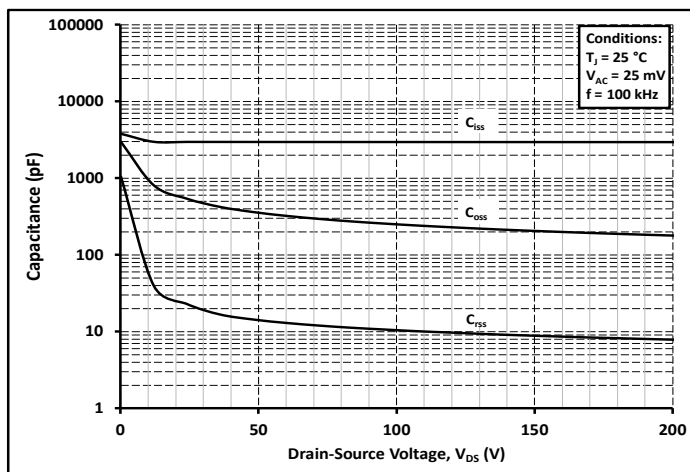


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

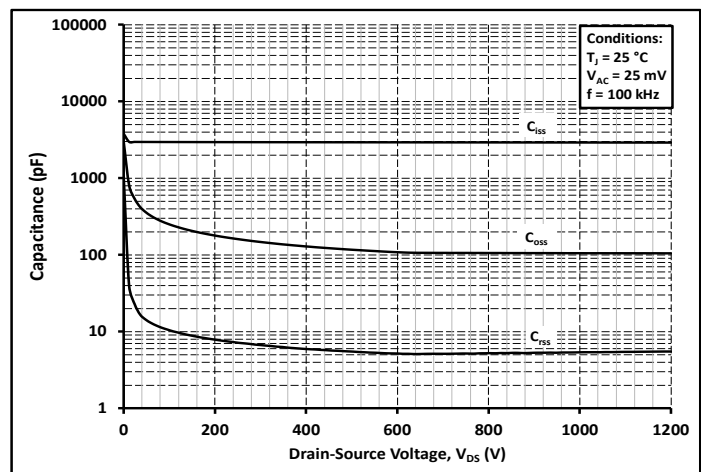


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)



Typical Performance

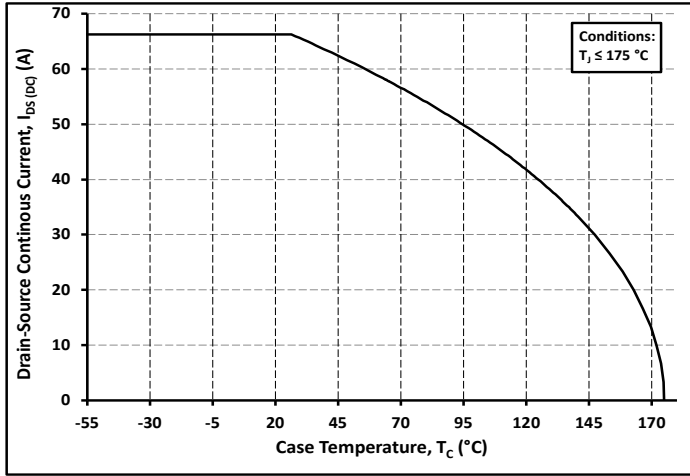


Figure 19. Continuous Drain Current Derating vs. Case Temperature

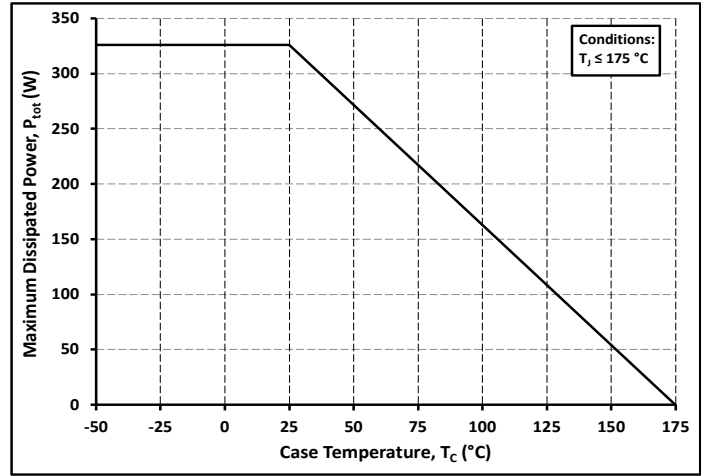


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

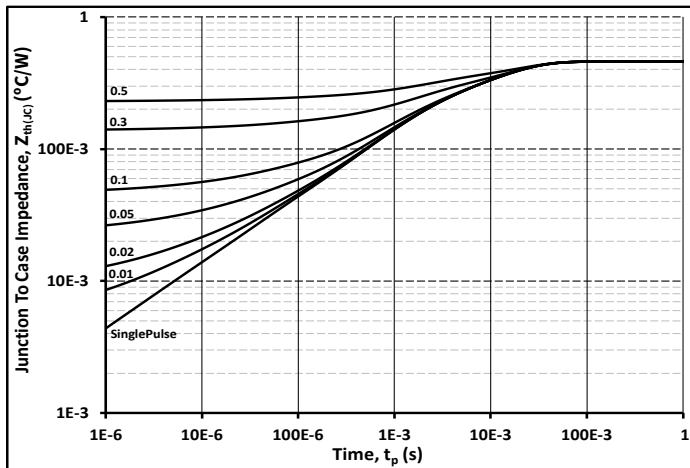


Figure 21. Transient Thermal Impedance (Junction - Case)

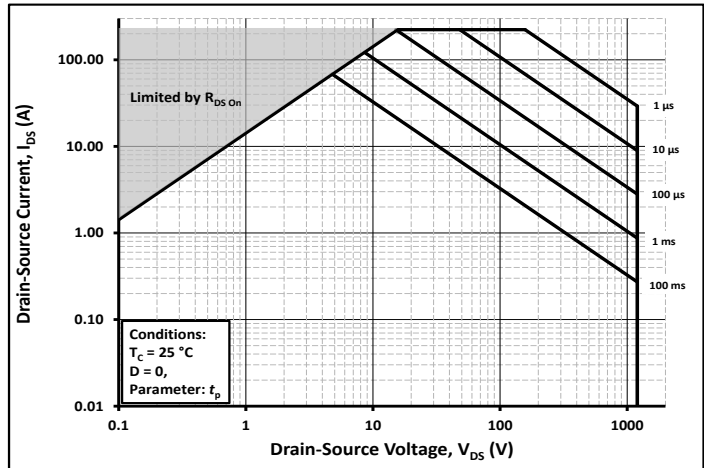


Figure 22. Safe Operating Area

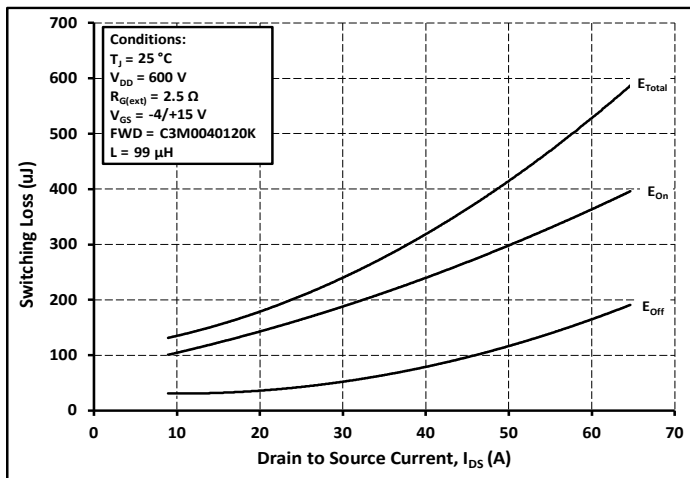


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600\text{ V}$ )

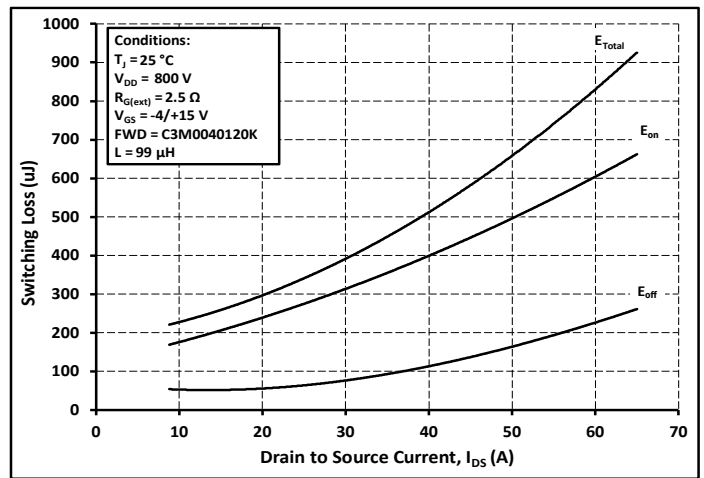


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800\text{ V}$ )



Typical Performance

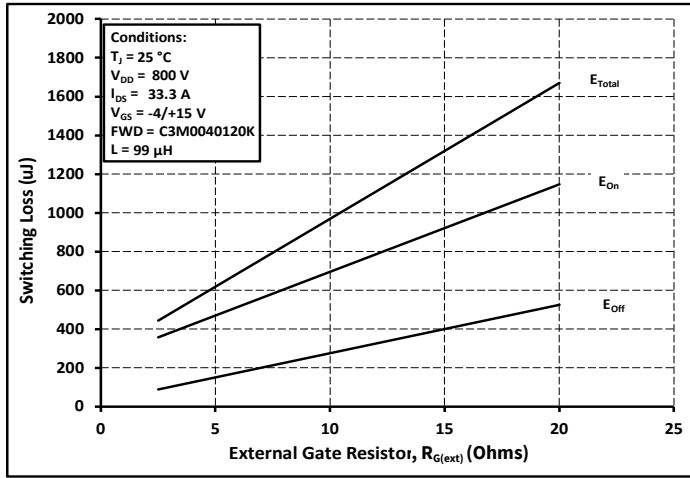


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

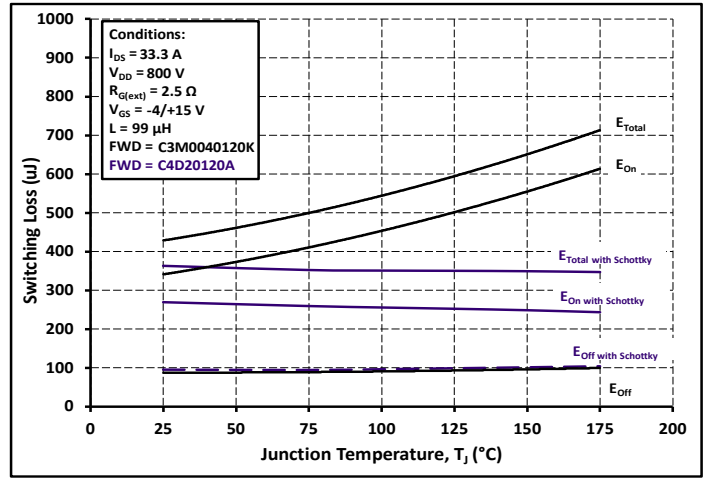


Figure 26. Clamped Inductive Switching Energy vs. Temperature

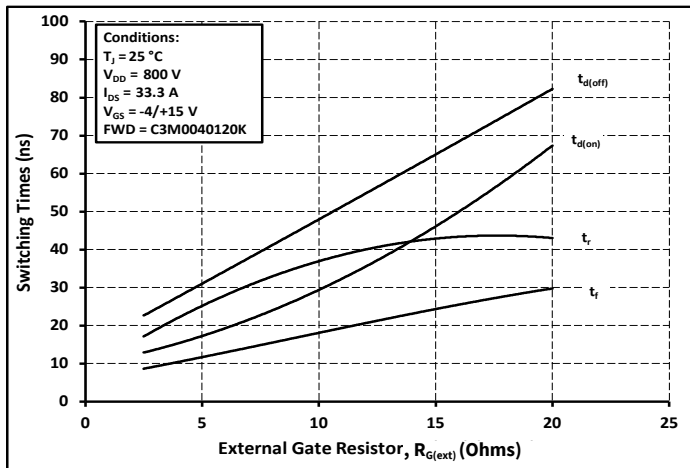


Figure 27. Switching Times vs.  $R_{G(ext)}$

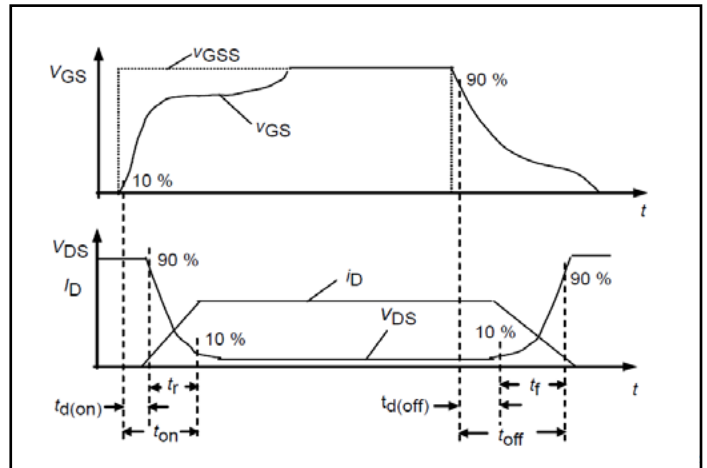
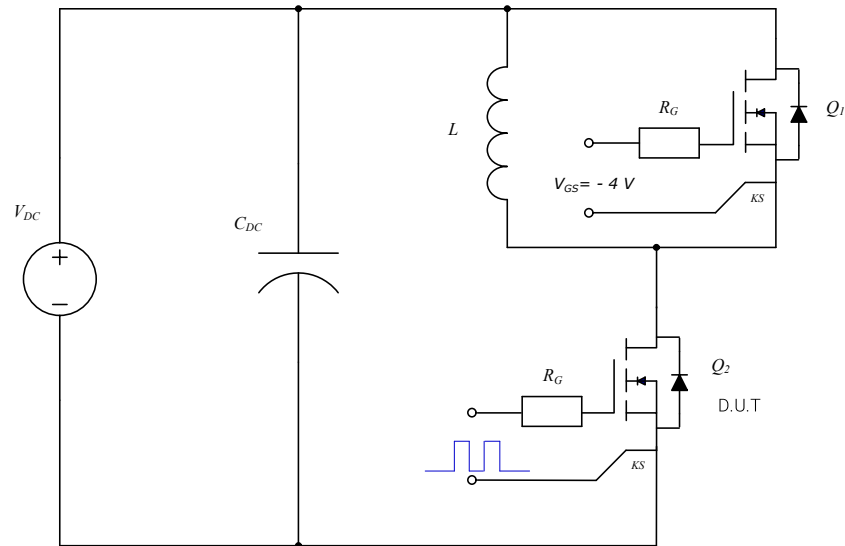


Figure 28. Switching Times Definition



## Test Circuit Schematic

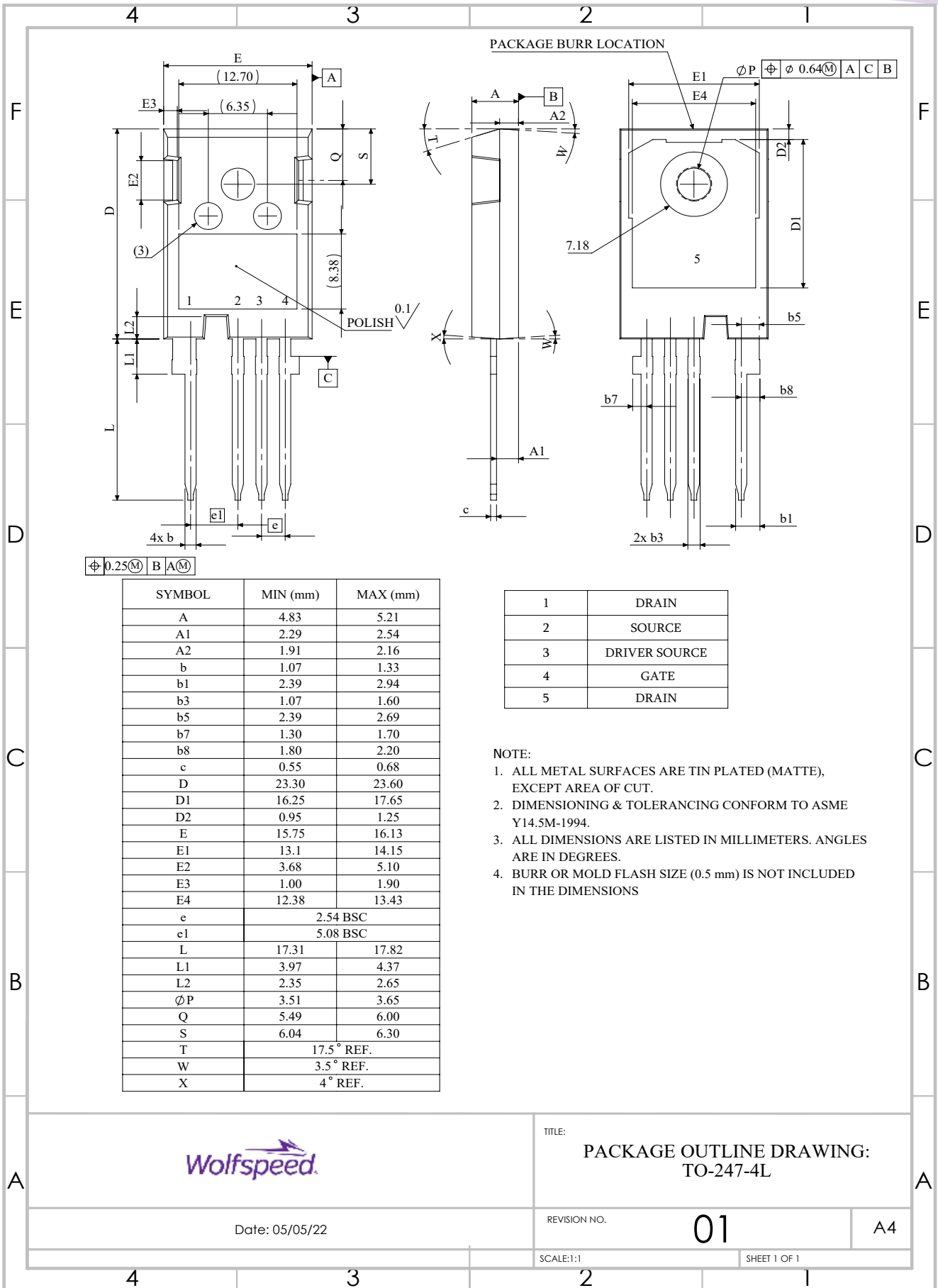


**Figure 29.** Clamped Inductive Switching Waveform Test Circuit

**Note:**

Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions – Package TO-247-4L



TITLE: PACKAGE OUTLINE DRAWING: TO-247-4L

Date: 05/05/22

REVISION NO.

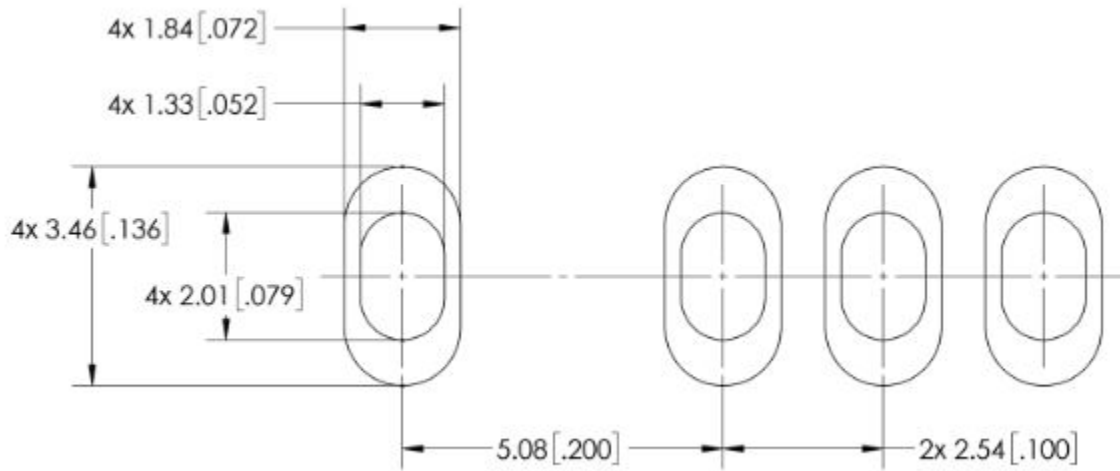
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SCALE:1:1

SHEET 1 OF 1

### Recommended Solder Pad Layout





## Related Links

- [SPICE Models](#)
- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)

## Revision History

Document Version	Date of Release	Description of Changes
1	October-2020	Initial Release
2	August-2023	ID Pulse test conditions Updated Package Drawing Updated Landing Pad



## Notes & Disclaimer

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The Silicon Carbide MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

### RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of [www.wolfspeed.com](http://www.wolfspeed.com).

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### Contact info:

4600 Silicon Drive  
Durham, NC 27703 USA  
Tel: +1.919.313.5300  
[www.wolfspeed.com/power](http://www.wolfspeed.com/power)